2015 European Conference on Circuit Theory and Design (ECCTD)

# Compensation Circuit with Additional Junction Sensor to Enhance Latchup Immunity for CMOS Integrated Circuits

Hui-Wen Tsai and Ming-Dou Ker
*Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan*

***Abstract*— A circuit solution to generate compensation current that can decrease the perturbation induced by the external latchup trigger was proposed. The robustness against latchup can be improved by supporting compensation current at the pad under latch-up current test. By inserting additional junctions to sense the latchup trigger current, the injected latchup trigger current can be detected, and then the I/O or ESD-protection devices are used to generate the compensation current that decrease the perturbation to the internal circuits. The proposed design has been successfully verified in a 0.5-μm BCD process to improve latchup immunity.**

***Keywords- Latchup, electrostatic discharge (ESD) protection, guard ring.***

## I. Introduction

Latchup problems, a parasitic pnpn path between the PMOS and NMOS, should be aware in the circuit design and implementation stages [1]-[3]. When such parasitic pnpn path was triggered on by the unexpected noises during the normal circuit operations with power supply, the chip would be often burned out to cause serious damage to IC products. Therefore, IC products to pass the required level of latchup test guided in JEDEC standards has become a must. The specifications of latchup trigger current characterization for the previous and updated JEDEC standards are summarized in Table I [4] and Table II [5], respectively. The maximum specification of trigger current that applied to the I/O pin of IC products has been increased from +/- 100mA to +/- 200mA, as specified in the updated latchup test standard [5]. Therefore, the method to improve latchup immunity should be strongly demanded by IC industry.

To achieve sufficient latch-up immunity, the parasitic devices and the triggering paths formed in the I/O cells with output driver and/or ESD devices are needed to be concerned. Fig. 1 shows an input buffer with ESD protection devices to provide general ESD protection [6]. With ESD-protection transistors, the guard rings are typically surrounding the whole devices, as that shown in the cell layout of Fig. 2, to decrease the susceptibility of latchup in both the input buffer and the internal circuits [7]-[8]. The occurrence of latchup will happen in the I/O cells and also in the internal circuits, where there are pnpn paths between the VDD-connected PMOS and GND-connected NMOS.

TABLE I
LATCHUP TRIGGER CURRENT CHARACTERIZATION IN THE PREVIOUS JEDEC STANDARD [4]

| Latchup I-test | Specification |
|---|---|
| Positive I-test | +100 mA |
| Negative I-test | -100 mA |

TABLE II
LATCHUP TRIGGER CURRENT CHARACTERIZATION IN THE UP-TO-DATED JEDEC STANDARD [5]

| Latchup I-test | | Specification |
|---|---|---|
| Positive I-test | I | < 50 mA |
| | II | 50 mA to < 100 mA |
| | III | 100 to 150 mA |
| | IV | 150 to 200 mA |
| | V | >= 200 mA |
| Negative I-test | I | > -50 mA |
| | II | -50 mA to > -100 mA |
| | III | -100 mA to > -150 mA |
| | IV | -150 mA to >-200 mA |
| | V | <= -200 mA |

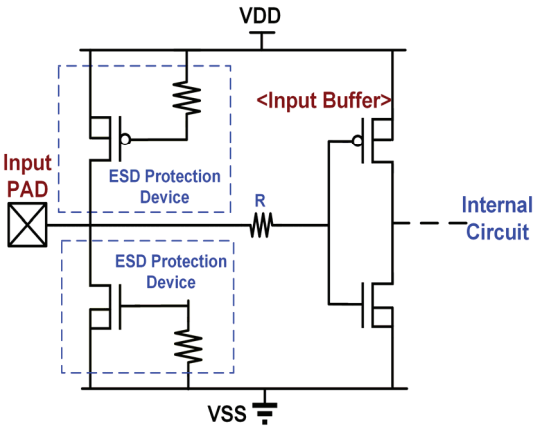


Fig. 1. Typical input buffer with ESD protection devices for the input pad.

In this work, a circuit solution to generate compensation current that can decrease the perturbation induced by the external latchup trigger current was proposed. The robustness

978-1-4799-9877-7/15/$31.00 ©2015 IEEE

against latchup can be improved by supporting compensation current at the pad under latch-up current test (I-test). By inserting additional junctions to sense the latchup trigger current, the injected latchup trigger current can be detected, and then the ESD-protection devices are used to generate compensation current that decrease the perturbation to the internal circuits.

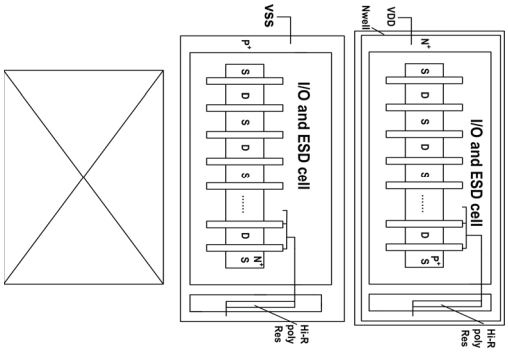


Fig. 2. The typical layout of I/O cell with single guard ring surrounding the PMOS and NMOS devices.

## II. Traditional Metchods for Latchup Prevention

Guard rings are the typical method used to prevent latchup issue. Fig.3 shows the typical layout implementation for latchup prevention with the specified design rules provided by foundry. The parasitic pnpn path inside a CMOS inverter that causes latchup issue is shown in Fig. 4(a). The trigger and holding voltage of the parasitic pnpn path inside the I/O or ESD devices are also needed to be greater than the supply voltage VDD in order to achieve latchup-free design, as depicted in Fig. 4(b).

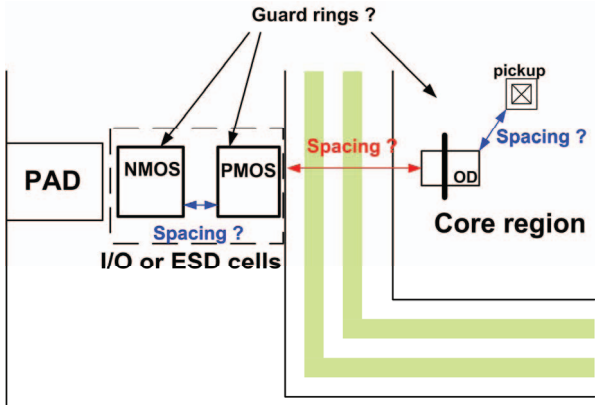


Fig. 3. Typical latchup prevention rules in layout implementation.

The I/O and/or ESD devices should be surrounded by some guard rings. The internal circuits are requested to add some pickups in layout that connected to the n-well with VDD bias or the p-well/p-sub. with GND bias. Besides, the additional guard rings are requested to be added between the I/O cells and the internal circuits, which are used to absorb the injected latchup trigger current from the I/O cell toward the internal circuits during the latchup I-test. Some testchips should be fabricated in silicon to investigate/decide above layout rules for meeting the requested latchup specification [9]. With a higher latchup test current of +/- 200mA, the widths of guard-ring diffusions, the spacing between the PMOS and NMOS, and the clearance between the I/O cell and internal circuits, should be also enlarged to improve latchup immunity.

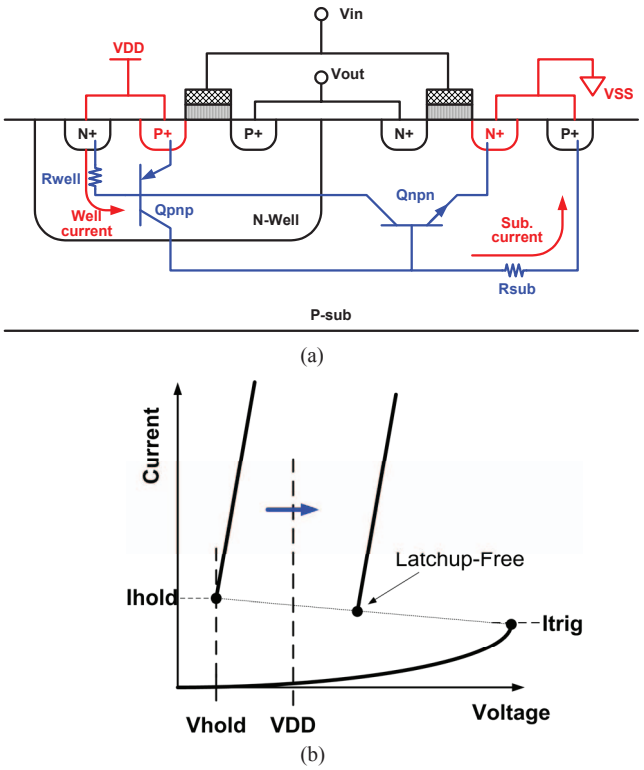


Fig. 4. (a) The parasitic pnpn path inside a CMOS inverter that cause latchup issue. (b) I-V characteristics to show latchup-free design.

## III. Proposed Compensation Circuit to Suppress External Latch-up Trigger Current

To increase the latch-up robustness against the external current triggers, a simpler alternative is designed with the schematic circuit and the layout structure shown in Fig. 5(a) and (b), respectively. Besides of the single guard ring, the proposed design adopts additional junctions to form effective BJTs (Qn1 and Qp1) and connect to the gate terminals. The Qn1 detects the latchup perturbations and then pulls low the gate of the Mp1 while sufficient negative trigger current is applied at the input pad. The external trigger current is approximately equal to the summation of the source-to-drain current of Mp1, the sensing current of Qn1, the drain to bulk current of the Mn1, and the substrate perturbation current that injected to the internal circuits. Thus, once the compensation current produced by the source-to-drain current of Mp1 is increased, the substrate perturbation current flowing to the internal circuits can be decreased during the latchup negative I-test. Therefore, the robustness of the proposed design against latchup can be enhanced. During the positive latchup triggers, the operation of the proposed work is quite similar as that in the negative I-test, but the sensor and the current provider are replaced by the Qp1 and Mn1, respectively.

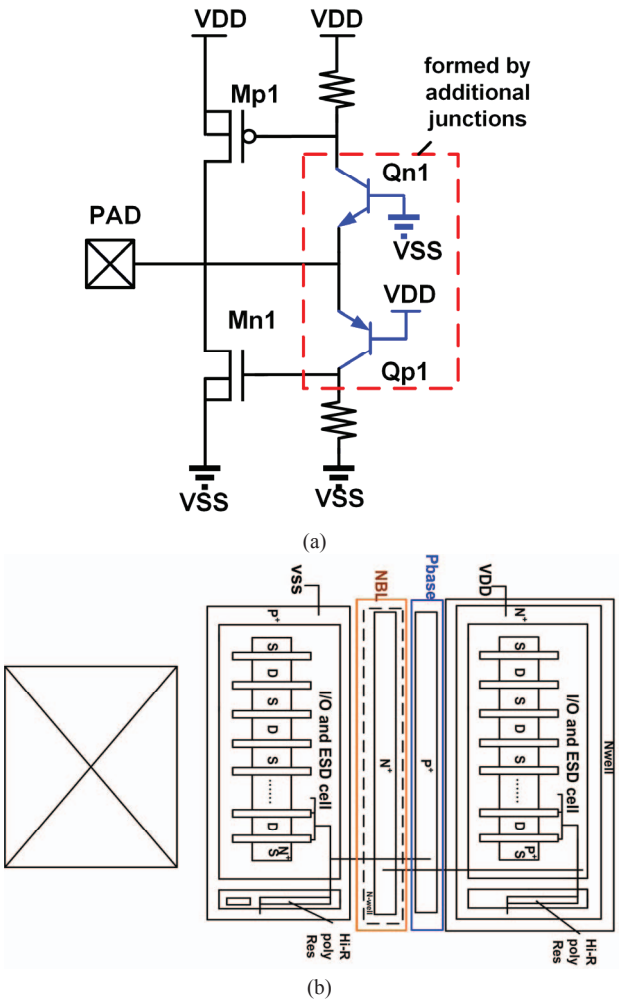


Fig. 5. (a) Schematic circuit, and (b) layout structure, of the proposed design with additional junctions to sense the injected current during latchup I-test.

While the sufficient positive trigger current is applied at the input pad, the rising voltage differences generate certain amount of emitter-to-collector current in Qp1 to turn on Mn1. With increased drain-to-source current in Mn1 to share the effect bringing by the external positive trigger current, the substrate perturbation current flowing to the internal circuits is also decreased to improve the immunity against latchup positive I-test. The planned layout structure is shown in Fig. 5(b). To increase the sensibility of Qp1 and Qn1, the n-well layer is added under the n+ diffusion region with NBL at beneath layers as well. Besides, pbase layers are adopted with p+ diffusion region. Since the process used for implementation is the 0.5-μm 5V/15V/25V/40V BCD process, the NBL and pbase layers are already embedded and can be used directly. The additional junctions located between the guard ring of Mp1 and Mn1 are used as the effective collector terminals of Qn1 and Qp1. The emitter of Qn1 and Qp1 are realized with the existing drain terminals of the Mn1 and Mp1, respectively. The 10-kΩ Hi-R poly resistors (Rn or Rp) are connected to the collectors and the gate terminals of Mn1 or Mp1. The values of the resistors are within the normal range (1~10kΩ) which is often selected for on-chip ESD protection.

## IV. Experimental Results

The 5-V CMOS devices embedded in a 0.5-μm 5V/15V/25V/40V BCD process has been adopted to realize the proposed design. Fig. 6(a) shows the layout photo of the testkey with the proposed design, and Fig. 6(b) shows the enlarged part at the location of the additional junctions. The distance between the guard rings of Mp1 and Mn1 is 12.9 μm. The NBL is slight extended to cover the nwell region, as well as the width of NBL (the extended length for NBL to nwell) and the nwell to p+ diffusion region follow the layout rules provided by foundry. Fig. 6(c) shows the whole top view of the test chip to verify the proposed design.

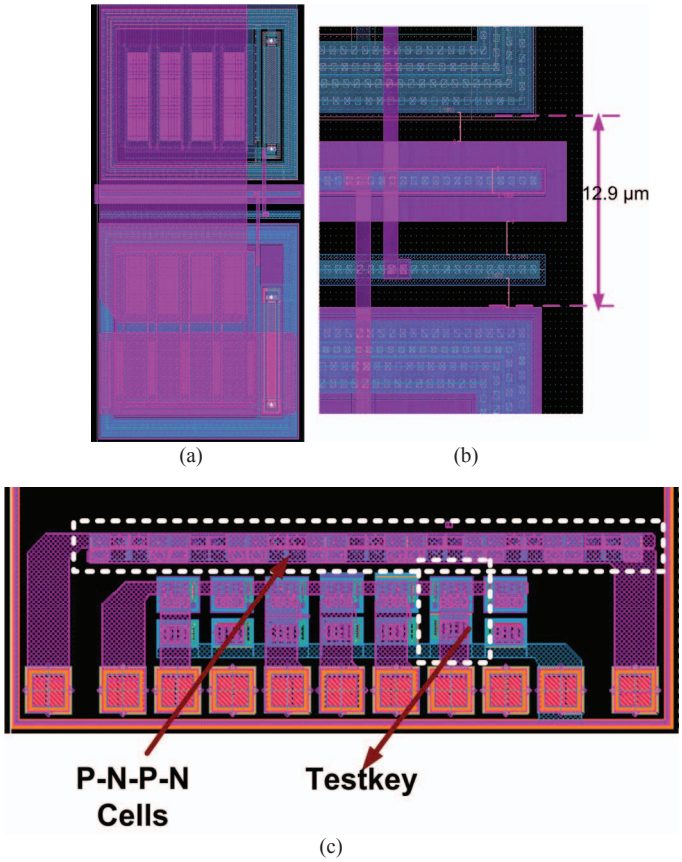


Fig. 6. Layout photos of (a) testkey with the proposed work, (b) enlarged graph at the location of additional junctions, and (c) the whole top view of the test chip.

The measurement setup to verify the testchip under latchup I-test is shown in Fig. 7. The sensors at the location of internal circuits to detect latchup occurrence are the pnpn cells which are about 30-μm away from the I/O cells. The distances (hn, hp, Xn, and Xp) in each pnpn cell are drawn with the typical layout rules in the given CMOS process provided by foundry, which are 35μm, 35μm, 20μm, and 20μm, respectively. The *Keithley* 2420 is used as the external source to provide latchup trigger current into the pad. During the latchup I-test, the power pads of VDD and VDD2 are biased at 5V, and the VSS and VSS2 pads are grounded. To easily distinguish the occurrence of latchup without burning out the pnpn sensor due to the inrushing short-circuit current when latchup happens,

the power supply pin (VDD2) of the internal pnpn sensors is connected to the 5-V supply through a 100-Ω resistor. A voltage meter is used to monitor the voltage level on the VDD2 pad. Once the apparent voltage drop at VDD2 is found (such as the change from ~5V to ~1.1V) after specific external trigger current is applied to the I/O pad, the latchup event is confirmed to be triggered on.

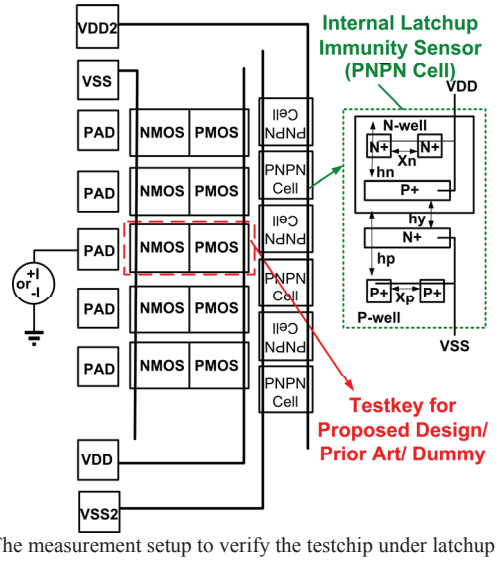


Fig. 7. The measurement setup to verify the testchip under latchup I-test.

Table III shows the measured results under positive and negative I-test on the testchip protected by the traditional method with single guard ring or by the proposed design. The total width/length of ESD device Mp1 (Mn1) in the I/O cell is 360μm/0.7μm (240μm/0.6μm). From Table III, the positive I-test immunity of the proposed work is enhanced to 29 mA, which is ~2.4 times larger as comparing to that of 12-mA immunity protected by only signal guard ring. For negative I-test, the robustness of the testkey with the proposed design is -370 mA which is about 15% increase as compared with that of -320 mA protected by only signal guard ring. Since the layout location of Mp1 is closer than Mn1 to the internal latchup sensor, and no additional junction was placed between the Mp1 and internal pnpn cells to pick up the substrate current, the immunity for positive I-test is inherently weaker than that for negative I-test.

TABLE III
MEASURED LATCHUP IMMUNITY OF THE TESTCHIP

| Latchup Trigger source | Protection by the traditional method with single guard ring | Protection by the proposed design |
|---|---|---|
| Positive I-test | +12 mA | +29 mA |
| Negative I-test | -320 mA | -370 mA |

## V. DISCUSSION

To meet the latchup immunity of +/-100mA or even higher of +/-200mA for IC products, the compensation current should be increased by enlarging the device dimensions of Mp1 and Mn1 in the I/O cell. In addition, the sensing junctions can be re-placed at the location between the I/O cells and the internal circuits to sense the injected current from the I/O cell toward the internal circuits. By the way, some circuit solutions to further improve latchup immunity of CMOS ICs were also reported in [10]-[12].

## VII. CONCLUSION

With additional junctions to sense latchup trigger current, the injected trigger current from the I/O cell toward the internal circuits can be detected. The ESD protection devices in the I/O cell are therefore turned on to generate the compensation current, which can reduce the latchup trigger current injected toward the internal circuits. Thus, the latchup immunity of CMOS ICs can be effectively improved. The proposed design verified in a 0.5-μm BCD process has successfully provided higher immunity against latchup I-test than that by traditional prevention with guard ring only.

## ACKNOWLEDGMENT

The authors want to thank Leadtrend Technology Corp. for the support of chip fabrication and latchup measurement. This work was also supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 103-2221-E-009-197-MY2 and MOST 104-2622-E-009-003.

## REFERENCES

[1] G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," in *Proc. IRPS*, 2005, pp. 137-144.

[2] V. Khemka, R. Zhu, A. Bose, and T. Roggenbauer, "Optimization and elimination of parasitic latchup in advanced smart-power technologies," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 1, pp. 69-73, Mar. 2007.

[3] S. Voldman, *Latchup*. John Wiley & Sons, 2007.

[4] *IC Latch-Up Test*, JEDEC Solid State Technology Organization, JESD78A Standard, 1997.

[5] *IC Latch-Up Test*, JEDEC Solid State Technology Organization, JESD78D Standard, 2011.

[6] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs of mixed-voltage I/O interfaces: design concept and circuit implementations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 235-246, Feb. 2006.

[7] S. Voldman, C. N. Perez, and A. Watson, "Guard ring: Theory, experimental quantification and design," in *Proc. EOS/ESD Symp.*, 2005, pp. 1-10.

[8] T.-L. Hsu, Y.-C. Chen, H.-C. Tseng, V. Liang, and J.-S. Jan, "Psub guard ring design and modeling for the purpose of substrate noise isolation in the SOC era," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 693-695, Sep. 2005.

[9] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semicond. Manufact.*, vol. 16, no. 2, pp. 319-334, May 2003.

[10] J.-J. Peng, M.-D. Ker, and H.-C. Jiang, "Latchup current self-stop circuit for whole chip latchup prevention in bulk CMOS integrated circuits," in *Proc. IEEE Int. Symp. Circuits & Systems*, vol. 5, 2002, pp. 537–49.

[11] J. A. Camarena, D. J. McQuirk, and M. H. Nagda, "Integrated circuit having latch-up recovery circuit," U.S. Patent 8638135, Jan. 28, 2014.

[12] H.-W. Tsai and M.-D. Ker, "Active guard ring to improve latch-up immunity," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4145-4152, Dec. 2014.