# ESD Protection Design with Stacked Low-Voltage Devices for High-Voltage Pins of Battery-Monitoring IC

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***Abstract*— For high-voltage (HV) application, an on-chip ESD protection solution has been proposed in a 0.25-µm HV BCD process by using low-voltage (LV) p-type devices with the stacked configuration. Experimental results in silicon chip have verified that the proposed design can successfully protect the 60-V pins of a battery-monitoring IC against over 8-kV human-body-mode (HBM) ESD stress.**

## I. Introduction

In smart power technologies, on-chip electrostatic discharge (ESD) protection design is one of the most challenging issues because ESD protection elements in high-voltage (HV) domains need to fit a narrow ESD protection design window for a successful ESD protection and to avoid latchup risk [1]–[4]. The narrow ESD protection design window is defined by the voltage difference between the maximum operating voltage and the breakdown voltage of the protected pin under ESD stress conditions. Some prior studies [5]–[7] had reported that using the HV device with a weak snapback characteristic as ESD protection element is easily adjusted to fit such requirement. However, the multi-layer structures in HV process drastically degrade the current capability of HV device to sustain ESD stress, as comparing to that of low-voltage (LV) device. Traditional ESD protection design by using HV device, such as LDMOS, must be often drawn with a large enough silicon area to meet the desired ESD specification. Comparing to HV device, LV device features simple device structure and high current capability. Moreover, it has been reported that the stacked devices can sustain high operating voltage and avoid latchup risk [8], [9]. LV devices with the stacked configuration can be an appropriate design to save silicon area for HV applications.

This work continues to verify the stacked configuration of LV devices for HV application. The structures of the stacked LV devices and its ESD protection effectiveness for the 60-V pins of a battery-monitoring IC are proposed and verified in a 0.25-µm HV BCD process.

## II. Proposed ESD Protection Design

The circuit scheme of a battery-monitoring IC studied in this work is shown in Fig. 1. It is designed to sense the battery current by HV input pins A and B (Va and Vb) for power management system in the electrical vehicles. Fig. 2 shows the ESD protection scheme for the battery-monitoring IC which includes HV and LV domains. In LV domain, the circuit block of output stage is protected by the LV IO cells with LV ESD elements. In HV domain, the circuit block of current sensing stage is protected by HV ESD element which consists of the stacked LV devices. The LV p-type MOS (PMOS) and p-type field-oxide device (PFOD) are used in this work. Such HV circuits and LV devices are realized with 60-V and 5-V standard devices, respectively, in a 0.25-µm HV BCD process. The battery voltage is ~55 V at the HV input pins (Va and Vb).

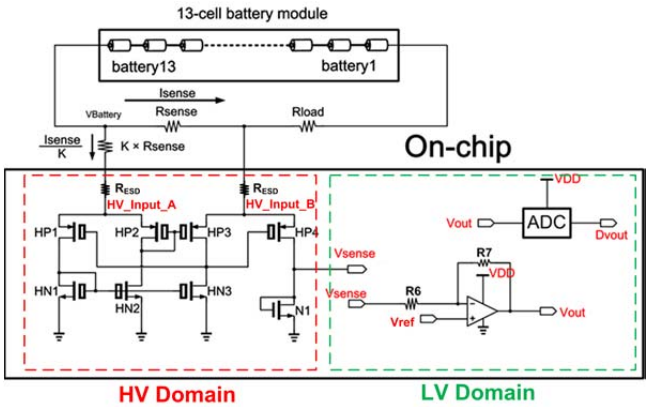



Fig. 1. Circuit scheme of the battery-monitoring IC.

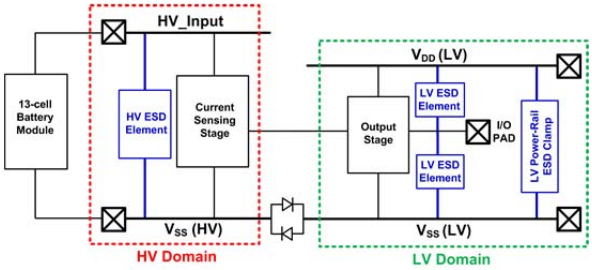
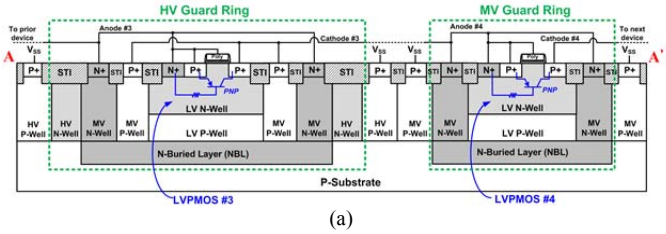


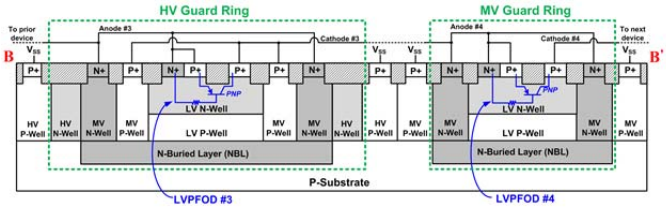

Fig. 2. ESD protection scheme for the battery-monitoring IC.

Figs. 3(a) and 3(b) show the cross-sectional view of the stacked LV-PMOS and LV-PFOD, respectively, where the MV (medium-voltage) N-well, HV N-well, and N-buried layer (NBL) are used to isolate the bias between the body of each device and the common p-type substrate to avoid breakdown when the HV signal is applied. According to the process information, the maximum breakdown voltage between MV N-well and P-well is ~50 V, and ~100 V between HV N-well and P-well, which should be taken into consideration when they are used in the stacked structure. FOD device features a gate-less structure as comparing to MOS device. Their inherent parasitic PNP BJTs, as main ESD dissipation path, are also designated in these plots. The device dimension of LV-PMOS is chosen as W/L of 2400µm/0.5µm with minimum layout spacing at drain and source sides to guarantee its high ESD robustness and to minimize the silicon area. The device dimension of LV-PFOD is chosen the same as that of LV-PMOS. The drain-to-source

breakdown voltage (BV) of each LV-PMOS or LV-PFOD is ~9 V in the given process. Thus, the stacked number is chosen as 7, so that the total BV is adjusted to be over 60 V to sustain the input signal of ~55 V at the HV input pins. The layout top view of 7 stacked devices with LV-PMOS and LV-PFOD are shown in Figs. 4(a) and 4(b), respectively. In consideration of a high voltage drop at the junction of the anode-connected LV N-well of the first 3 cascaded devices to the common p-type substrate when the stacked devices are triggered on by ESD stress, the HV guard ring is individually used for them to avoid the unwanted junction breakdown. The last 4 cascaded devices are individually surrounded by the MV guard ring due to the lower voltage drop at the junction of the MV N-well and the MV P-well, which can save the area footprint of the stacked structure. The cross-sectional views of 2 cascaded devices along the A-A' and B-B' regions in Fig.4 are also shown in Fig. 3(a) and 3(b), respectively.

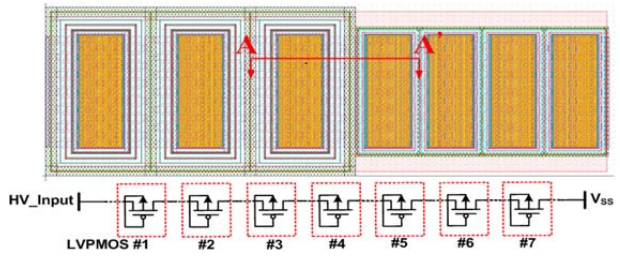



(a)

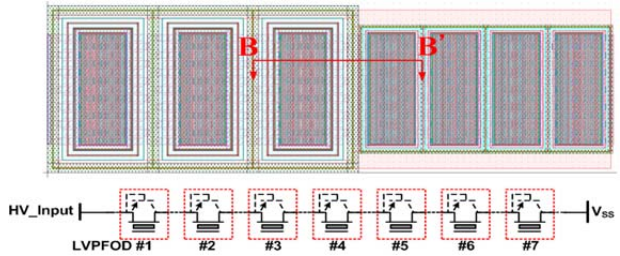



(b)

Fig. 3. Cross-sectional view of 2 cascaded devices with (a) LV-PMOS and (b) LV-PFOD, respectively.




(a)




(b)

Fig. 4. Layout top view of (a) 7 stacked LV-PMOS and (b) 7 stacked LV-PFOD, respectively.

## III. Experimental Results

### A. ESD Robustness of the Stacked LV Devices

To investigate the turn-on behavior of ESD device during high ESD current stress, a TLP generator [10] with a pulse width of 100 ns and a rise time of 10 ns is used to measure the snapback I-V curves of the stacked devices. The TLP-measured I-V curves of these two stacked structures are shown in Fig. 6 and the test results are listed in Table I. The ESD robustness is measured by the ESD tester with HBM model [11]. The TLP-measured failure current ($I_{t2}$) of stacked LV-PMOS and LV-PFOD are 5.37 A and 5.18 A, respectively. The holding voltage ($V_h$) of these two stacked structures are both higher than ~55 V to avoid the latchup risk, and their BV are higher than ~60 V as expected. The stacked LV-PMOS shows its HBM level of 6.5 kV, and stacked LV-PFOD shows over 8 kV. The holding voltage and on-state resistance ($R_{on}$) of LV-PFOD are higher than that of LV-PMOS because the thick oxide structure in FOD not only reduces the beta gain of intrinsic PNP BJT but also increases its series resistance.

Furthermore, it is found that the TLP-measured failure current is not so consistent with the HBM level from the measurement results of stacked LV-PMOS. The failure mechanism of such non-consistent phenomenon had been reported in some studies [12]–[14]. This may be attributed to the gate oxide (GOX) failure under HBM ESD test. The device, which has thin gate oxide structure, is easily damaged during HBM ESD stress to cause a miscorrelation between TLP and HBM ESD test results.

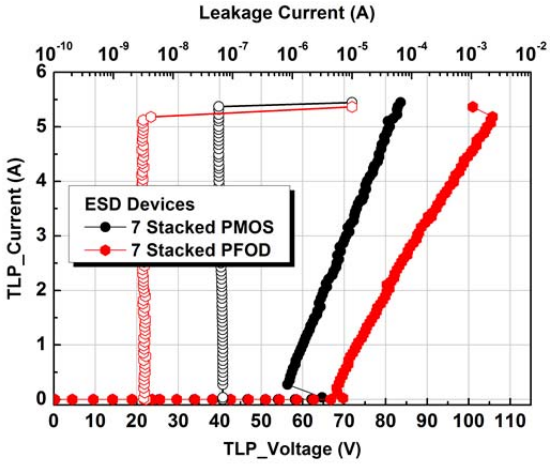



Fig. 6. TLP-measured I-V curves of stacked LV-PMOS (black dot) and LV-PFOD (red dot).

TABLE I ESD Robustness of Stacked Devices

| Device Type | Stacked LV-PMOS | Stacked LV-PFOD |
|---|---|---|
| Layout Area ($\mu m^2$) | 153 x 440 | 153 x 440 |
| BV (V) | 61.54 | 66.12 |
| $V_{hold}$ (V) | 56.35 | 68.19 |
| $I_{t2}$ (A) | 5.37 | 5.18 |
| HBM (kV) | 6.5 | > 8 |

*B. ESD Verification on HV Input Pin*

To verify ESD protection effectiveness of the stacked devices to protect the HV input pin, the measurement setup is shown in Fig. 7. HV input pin (Va or Vb) is connected with stacked devices under HBM ESD test. The resistance $R_{ESD}$, chosen as 2kΩ, is used to limit HBM ESD current into HV circuit block, but without affecting the normal HV circuit function. The leakage current is measured under DC bias at room temperature (25 ºC). When the current abruptly increases up to 1 μA, the corresponding bias voltage is judged as the breakdown voltage. The failure criterion is 10% deviation from its original I-V curve. After HBM ESD stress, the I-V curves of leakage current are measured on the HV pin Vb with the stacked LV devices, as shown in Figs. 8 and 9.

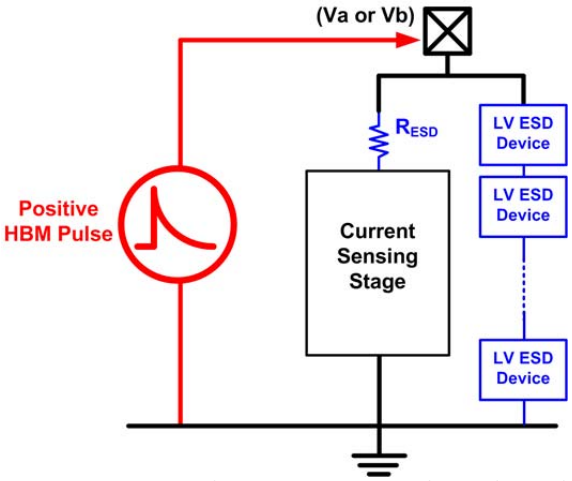



Fig. 7. Measurement setup for HBM ESD test on the HV input pin (Va or Vb) protected by the stacked LV devices.

TABLE II ESD ROBUSTNESS OF THE HV PIN WITH/WITHOUT ESD PROTECTION ELEMENT

| HV Pin with / without ESD Protection Element | HBM ESD Level (kV) |
|---|---|
| HV Pin (Va or Vb) | < 0.5 |
| HV Pin (Va or Vb) with Stacked LV-PMOS | 6.5 |
| HV Pin (Va or Vb) with Stacked LV-PFOD | > 8 |

In Fig. 8, the I-V curves of HV pin Vb with stacked LV-PMOS did not show any degradation after 6.5-kV HBM ESD test. However, after 7-kV HBM ESD stress, the I-V curve of HV pin Vb with stacked LV-PMOS shifts over 10% from its original curve. Thus, the HBM ESD level of HV input pin protected by the stacked LV-PMOS is judged to be 6.5 kV. In Fig. 9, the I-V curves of HV pin Vb with stacked LV-PFOD did not show any obvious degradation after 8-kV HBM ESD stress. Thus, the HBM ESD level of the HV pin Vb protected by the stacked LV-PFOD can be over 8 kV. The ESD test results on the HV pin Va are the same as those of HV pin Vb, due to the symmetric circuit structure in the current sensing stage. The test results are also summarized in Table II. Without using the stacked LV-PMOS or LV-PFOD to protect the HV pin, its original HBM ESD level is below 500V. Through the practical ESD test on the silicon chip, it has been verified that the stacked LV devices can provide effective ESD protection for those 60-V HV pins in the battery-monitoring IC.

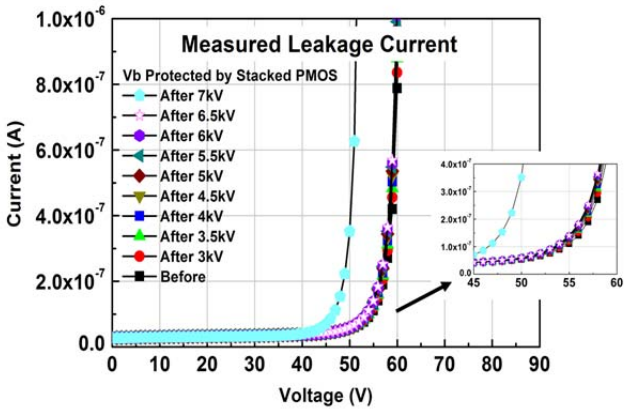



Fig. 8. Measured leakage current on the HV pin Vb, protected by the stacked LV-PMOS, after each HBM ESD test.

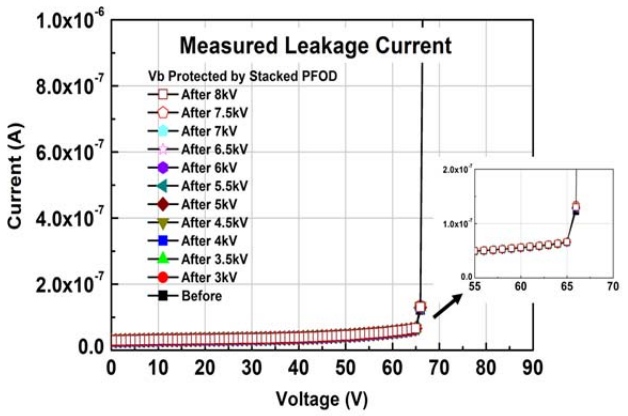
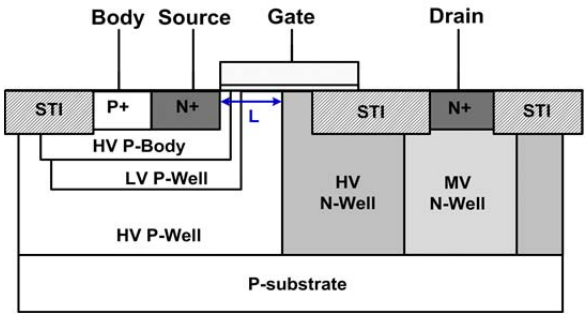


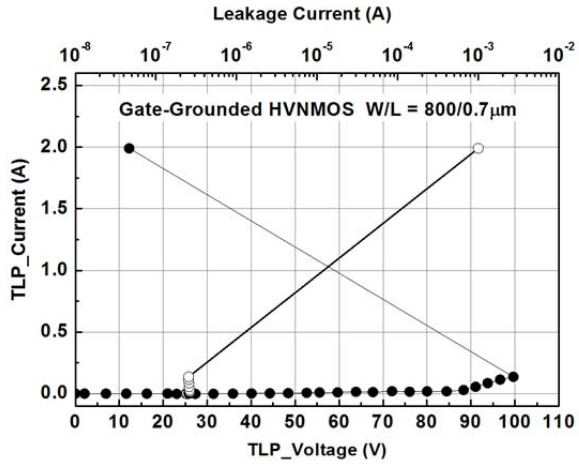

Fig. 9. Measured leakage current on the HV pin Vb, protected by the stacked LV-PFOD, after each HBM ESD test.

*C. ESD Robustness of HV NMOS*

To verify the intrinsic ESD robustness of HV NMOS in the given 0.25-μm HV BCD process, the stand-alone HV NMOS was also drawn and fabricated in the same process. The device structure of HV NMOS in the 0.25-μm HV BCD process is shown in Fig. 10(a). The TLP-measured I-V curves of stand-alone HV NMOS with device dimension (W/L) of 800μm/0.7μm is shown in Fig. 10(b). The failure current of this HV NMOS is only ~0.2 A, even if its channel width is as large of 800 μm. The HBM ESD level of such a stand-alone HV NMOS is around ~300 V. The self-protection ability of such HV devices in the 0.25-μm HV BCD process against ESD stress is very weak. Thus, the ESD protection solution proposed in this work is an effective way to protect the HV ICs against ESD stress.




(a)




(b)

Fig. 10. (a) Device structure of the HV NMOS in a 0.25-μm HV BCD process. (b) TLP-measured I-V curves of the stand-alone HV NMOS with a W/L of 800μm/0.7μm.

## IV. Conclusion

HV ESD protection design realized by stacked LV devices has been proposed and verified in a 0.25-μm HV BCD process. By adjusting the stacked number of LV devices, the total holding voltage and total breakdown voltage of the stacked devices can be higher than the maximum supply voltage of the protected pins to avoid either latchup issue or breakdown event during the normal HV circuit operation. From the experimental results, the stacked LV devices can successfully protect the 60-V input pin of HV circuit block against 8-kV HBM ESD stress. Stacked structure of LV devices can be an appropriate ESD protection solution to fit the required ESD protection window in various high-voltage applications, without developing special modification on the HV devices with additional mask layers and process steps.

## Acknowledgment

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## References

[1] B. Keppens, M. Mergens, C. Trinh, C. Russ, B. Camp, and K. Verhaege, "ESD protection solutions for high voltage technologies," in *Proc. EOS/ESD Symp.*, 2004, pp. 289–298.

[2] M. Mergens, M. Mayerhofer, J. Willemen, and M. Stecher, "ESD protection considerations in advanced high-voltage technologies for automotive," in *Proc. EOS/ESD Symp.*, 2006, pp. 54–63.

[3] W.-Y. Chen, M.-D. Ker, and Y.-J. Huang, "Investigation on the validity of holding voltage in high-voltage devices measured by transmission-line-pulsing (TLP)," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 762–764, Jul. 2008.

[4] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain extended MOS devices," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 4, pp. 615–625, Dec. 2012.

[5] A. Gendron, P. Renaud, P. Besse, C. Salamero, M. Bafleur, and N. Nolhier, "Area-efficient reduced and no-snapback PNP-based ESD protection in advanced smart power technology," in *Proc. EOS/ESD Symp*., 2006, pp. 69–76.

[6] P. Renaud, A. Gendron, M. Bafleur, and N. Nolhier, "High robustness PNP-based structure for the ESD protection of high voltage I/Os in an advanced smart power technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technology Meeting*, 2007, pp. 226–229.

[7] C.-K. Chen, C.-F. Huang, Y.-F. Chang, J.-W. Lee, S.-M. Cheng, and M.-H. Song, "Schottky emitter high holding voltage ESD clamp in BCD power technology," in *Proc. EOS/ESD Symp*., 2012.

[8] M.-D. Ker and K.-H. Lin, "The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1751–1759, Aug. 2005.

[9] O. Quittard, Z. Mrcarica, F. Blanc, G. Notermans, T. Smedes, and H. Zwol, "ESD protection for high-voltage CMOS technologies," in *Proc. EOS/ESD Symp.*, 2006, pp. 77–86.

[10] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.

[11] Electrostatic Discharge (ESD) Sensitivity Testing — Human Body Model (HBM), EIA/JEDEC Standard Test Method A114-D, 2006.

[12] D. Linten, V. Vashchenko, M. Scholz, P. Jansen, D. Lafonteese, S. Thijs, M. Sawada, T. Hasebe, P. Hopper, and G. Groeseneken, "Extreme voltage and current overshoots in HV snapback devices during HBM ESD stress," in *Proc. EOS/ESD Symp.*, 2008, pp. 204–210.

[13] M. Scholz, D. Linten, S. Thijs, S. Sangameswaran, M. Sawada, T. Nakaei, T. Hasebe, and G. Groeseneken, "ESD on-wafer characterization: Is TLP still the right measurement tool," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 10, pp. 3418–3426, Oct. 2009.

[14] S.-H. Chen, S. Thijs, A. Griffoni, D. Linten, A. Keersgistere, and G. Groeseneken, "Unexpected failure during HBM ESD stress in nanometer-scale nLDMOS-SCR devices," in *IEDM Tech. Dig.*, 2011, pp. 6.4.1–6.4.4.