ESD Protection Design with Latchup-Free Immunity in 120V SOI Process

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***Abstract*— Electrostatic discharge (ESD) protection with low-voltage (LV) field-oxide devices in stacked configuration are proposed for high-voltage (HV) applications in a 0.5-μm 120V SOI process. Stacked LV field-oxide devices with different stacking numbers have been verified in silicon chip to exhibit both of high ESD robustness and latchup-free immunity for HV applications.**

I. Introduction

In high-voltage (HV) applications, the power management ICs and automotive ICs play a major role, which were often realized with the Laterally-Diffused-MOS (LDMOS) devices [1]. The HV ICs implemented in the SOI process have got more advantages to manage HV blocks, to reduce parasitic bipolar effect, and to increase circuit speed. To get sufficient ESD robustness for the HV ICs, the HV devices at the I/O pins were often drawn with a large device dimension to meet the ESD specifications. In the literatures [2]-[9], ESD protection in SOI process was reported with MOS and SCR combining together into the same device structure, which allowed SCR being triggered on to reach a high ESD robustness. However, the holding voltage of SCR was much lower than the circuit operation voltage level, that would cause serious latchup-like failure issue in the HV applications. The typical I-V characteristics of ESD protection devices are shown in Fig. 1. The snapback behavior of the SCR embedded with HV LDNMOS together is still not to fulfill ESD design window for HV applications. Comparing to HV devices, the LV devices were relatively good at ESD robustness, and the stacked configuration is a way to achieve a high holding voltage [10].

In this work, the stacked low-voltage p-type field-oxide devices (LVPFOD) with different stacking numbers for 120-V applications were investigated in a 0.5-μm SOI process. Different HV ESD protection devices were also accomplished as reference. Experimental results measured by DC I-V curve tracer, transmission-line-pulsing (TLP) system, and ESD tester have confirmed that the proposed solution can achieve both of high ESD robustness and latchup-free immunity for 120-V applications.

II. Typical HV Device in SOI Process

The simplified device cross-sectional view and the corresponding layout top view of the 120-V LDNMOS are shown in Fig. 2(a) and 2(b), respectively. The device dimension of LDNMOS was drawn as 2W/L = 200μm/0.9μm in the testchip. The TLP-measured I-V characteristics of the 120-V LDNMOS is shown in Fig. 3. The drain breakdown voltage of the 120-V LDNMOS is 141V, and the trigger voltage (V_{t1}) is 155V. But, such a 120-V device got a very low ESD robustness (<200V, HBM), which was almost burned out immediately when entering into its snapback region. Such a 120-V LDNMOS cannot provide self protection, but also unable to protect the internal circuits or devices in the HV ICs.

III. Proposed Solution with Stacked LVPFOD

The device cross-sectional view and the layout top view of the stacked LVPFOD structure in the 0.5-μm 120V SOI process are shown in Fig. 4(a) and 4(b), respectively. The dimension of each LVPFOD in the stacked configuration was drawn with W=800μm and S=0.9μm, which was fully isolated to each other by the DTI and buried oxide. Every LVPFOD was only connected through the metal layers to make the stacked configuration with different stacking numbers. The TLP-measured I-V characteristics of the stacked LVPFOD with different stacking numbers are shown in Fig. 5. The detailed characteristics of stacked LVPFOD with different stacking numbers are listed in Table I. The trigger voltage (V_{t1}) of stacked LVPFOD can be smaller than the breakdown voltage of HV LDMOS to get an effective ESD protection. The holding voltage (V_h) of stacked LVPFOD can be greater than the maximum operation voltage (Vcc) to avoid latchup issue. The stacked LVPFOD also exhibited excellent ESD robustness of up to 4.5kV in HBM ESD test. Table II depicts the comparison among HV ESD protection in SOI process with the previous arts. The silicon data reported in this work showed the first solution in SOI process that can provide over 4-kV HBM ESD level in a 120-V SOI process with reasonable layout area.

IV. Conclusion

An effective ESD protection solution realized with stacked LVPFOD has been successfully verified in a 0.5-μm SOI process for 120-V applications. The 12-LVPFOD stacked structure can get a holding voltage of 130.9V and pass HBM ESD test of 4.5kV. By adjusting the stacking numbers, the proposed ESD protection solution can be further used for higher voltage applications and also get latchup-free immunity.

Acknowledgment

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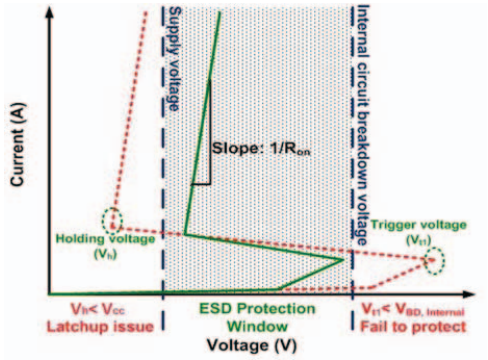
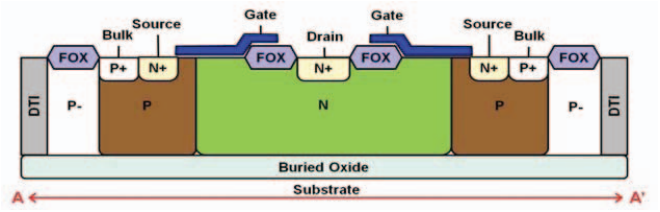
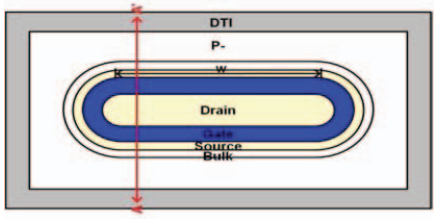


Fig. 1. I-V characteristics of ESD protection device to meet ESD protection window.



(a)



(b)

Fig. 2. (a) Device cross-sectional view, and (b) layout top view of 120-V LDNMOS in a 0.5-μm SOI process.

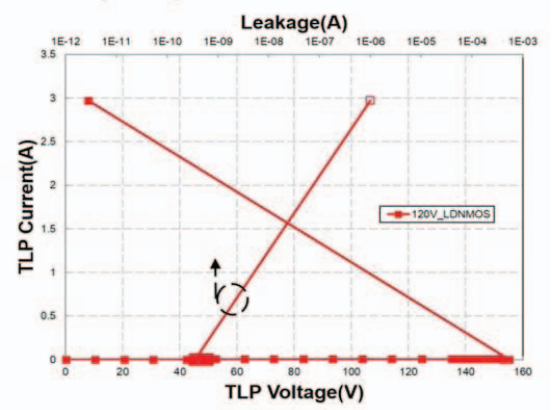
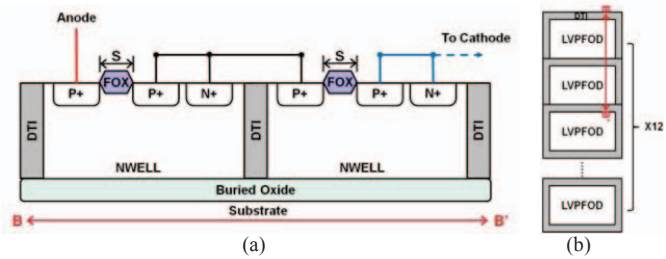


Fig. 3. TLP I-V characteristics of 120-V LDNMOS in a 0.5-μm SOI process.



(a) (b)

Fig. 4. (a) Device cross-sectional view, and (b) layout top view of the proposed ESD protection solution realized with the stacked LVPFOD in a 0.5-μm SOI process.

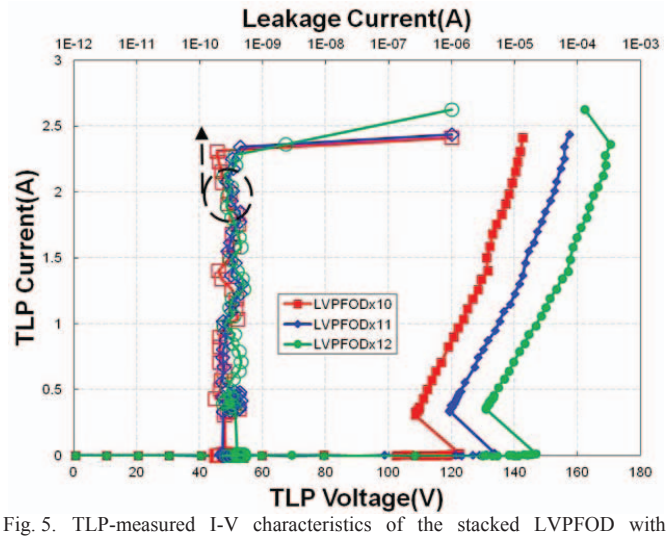


Fig. 5. TLP-measured I-V characteristics of the stacked LVPFOD with different stacking numbers of 10, 11, and 12, verfified in a 0.5-μm SOI process.

TABLE I
Summary of stacked LVPFOD with different stacking numbers.

Stacked LVPFOD	10 units	11 units	12 units
V_{t1}	122.5V	133.7V	146.7V
V_h	108.4V	119.4V	130.9V
I_{t2}	2.31A	2.34A	2.36A
BV (I@1μA)	111.5V	122.5V	133.5V
HBM ESD Level	4.5kV	4.5kV	4.5kV

TABLE II
Comparison of HV ESD protection solutions among the prior arts in SOI process.

ESD Solutions	Technology (SOI)	Device used for ESD protection	Supply Voltage (Vcc)	TLP (100ns)			HBM ESD Level	Device Width (μm)	Latchup Issue (*2)
				V_{t1} (V)	V_h (V)	I_{t2} (A)			
[2]	40V SOI LDMOS process	LDMOS-SCR	40V	53	4	1.25	N.A.	N.A.	Yes
[3]	60V SOI BCD process	LDMOS-SCR	60V	70	3.5	1.25	N.A.	N.A.	Yes
[4]	0.18μm 60V SOI BCD process	LDMOS-SCR	60V	65	10	2.5	N.A.	40	Yes
[5], [6]	0.8μm SOI BCD process	LDMOS-SCR	25V	37	3	5.5	N.A.	300	Yes
[7]	SOI process	LDMOS-SCR	42V	65	5	>10	N.A.	N.A.	Yes
[8]	0.5μm SOI process	LDMOS-SCR	15V	42	17	5.1	N.A.	120	No
[9]	0.18μm 40V SOI BCD process	LDMOS	40V	47	10	2.14	N.A.	N.A.	Yes
This work	0.5μm 120V SOI process	12-LVPFOD stacked	120V	146.7	130.9	2.36	4.5kV (*1)	800	No

(*1) ESD failure criteria : BV (I @1μA) shift >20%.
(*2) The holding voltage (V_h) should be larger than the supply voltage (V_{CC}) to avoid latchup issue.

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