A Gigahertz Low-Noise Amplifier with ESD Protection in Nanoscale CMOS Technology

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ABSTRACT

To provide the effective electrostatic discharge (ESD) protection for a gigahertz low-noise amplifier (LNA) with less radio-frequency (RF) performance degradation, a new ESD protection circuit is studied in this work. Such LNA with the proposed ESD protection has been successfully verified in silicon chip to achieve 4kV human-body-model (HBM) ESD robustness. With the better performances, the proposed ESD protection circuit is very suitable for gigahertz RF applications.

INTRODUCTION

The ESD protection must be taken into consideration during the design phase of integrated circuits, including the RF circuits. However, adding ESD protection causes RF performance degradation with several undesired effects. The parasitic capacitance of ESD protection device is one of the most important design considerations for RF circuits. A typical specification for a gigahertz LNA on HBM ESD robustness and the maximum parasitic capacitance of ESD protection device are 2kV and 200fF, respectively [1]. As the operating frequencies of RF circuits increase, the parasitic capacitance was more strictly limited. In order to fulfill such a tight specification, diodes have been commonly used for RF ESD protection. The conventional double-diode ESD protection design for LNA is shown in Fig. 1, where two ESD diodes (D_P and D_N) at RF input (RF_{in}) pad are assisted with the power-rail ESD clamp circuit to prevent LNA from ESD damage.

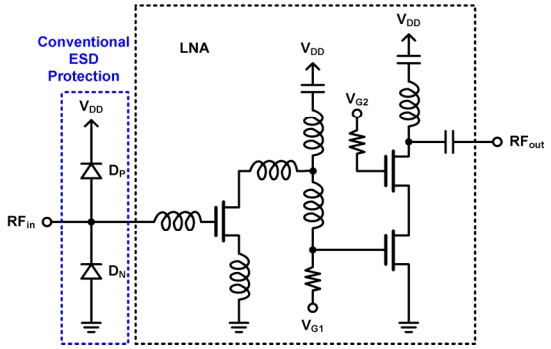

Fig. 1 Conventional ESD protection for LNA.

PROPOSED ESD PROTECTION

The proposed ESD protection is shown in Fig. 2, which consists of a silicon-controlled rectifier (SCR), an inductor, and a diode string [2]. The Q_{PNP} is formed by the P+, N-well, and P-well, and the Q_{NPN} is formed by the N-well, P-well, and N+. The ESD current path from RF_{in} to ground consists of P+/N-well/P-well/N+ SCR. The diode string is used to enhance the turn-on efficiency of SCR. The ESD current path from ground to RF_{in} consists of P-well/N-well diode and inductor.

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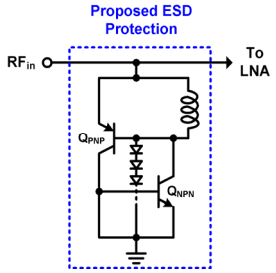

Fig. 2 Proposed ESD protection for LNA.

VERIFICATION IN SILICON

In order to verify the RF characteristics and ESD robustness, the LNA circuits with and without ESD protections are fabricated in the same chip. The RF performances of all LNA circuits before and after HBM ESD stresses are measured. The gains of three LNA circuits after various ESD stresses are shown in Fig. 3. The stand-alone LNA is severely degraded after 0.5kV HBM ESD stress. The LNA with conventional ESD protection can sustain 1.5kV HBM ESD stress. The LNA with proposed ESD protection can sustain 4kV HBM ESD stress.

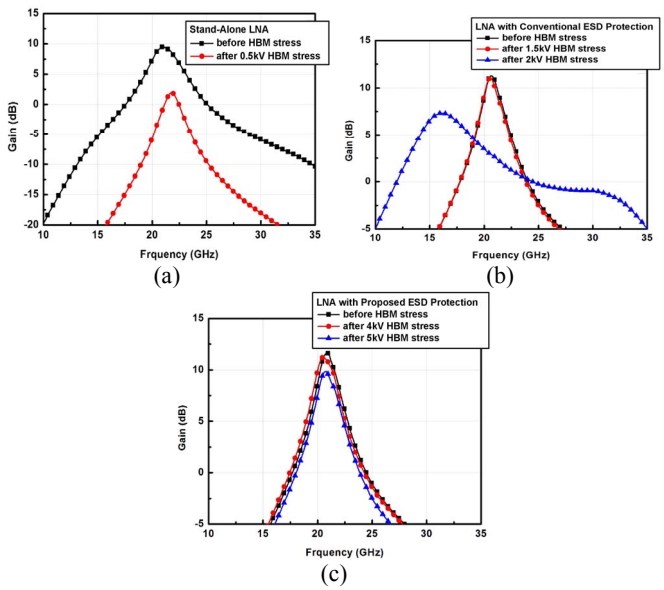

Fig. 3 Measured gain of LNA (a) without ESD protection, (b) with conventional ESD protection, and (c) with proposed ESD protection.

CONCLUSION

The proposed ESD protection has been developed in nanoscale CMOS process for RF applications. Measurement results verify the high-frequency performances and confirm the ESD protection ability of the proposed ESD protection design.

REFERENCES

[1] M.-D. Ker *et al.*, "ESD test methods on integrated circuits: an overview," in *Proc. IEEE ICECS*, 2001, pp. 1011-1014.

[2] C.-Y. Lin and R.-K. Chang, "Design of ESD protection device for K/Ka-band applications in nanoscale CMOS process," *IEEE T-ED*, vol. 62, no. 9, pp. 2824-2829 Sep. 2015.

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