On-Chip ESD Protection Design for HV Integrated Circuits

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***Abstract* — Electrostatic discharge (ESD) protection has been an important reliability issue to CMOS integrated circuits, especially in high-voltage (HV) applications. In this invited talk, a brief overview on ESD protection designs for HV integrated circuits is presented. The useful and safe solutions are highlighted for real applications in HV IC products.**

***Keywords* — *ESD protection; high-voltage (HV) IC*.**

I. Introduction

Electrostatic discharge (ESD) may occur accidentally during the fabrication, package, and assembling processes of IC products, which often caused serious damages on ICs. High-voltage (HV) ICs were found with bad ESD robustness [1]. Lateral DMOS (LDMOS) was often used as ESD protection device in HV process, but the holding voltage (V_h) of LDMOS after snapback was smaller than the circuit operating voltage (V_{CC}) [2]. During normal circuit operation, the noise might unpredictably trigger the parasitic BJT of the ESD devices, and the supply voltage (V_{CC}) keeps the parasitic BJT to be continually turned on. Such on-chip HV ESD device would be burned out after a period of time, under the circuit normal operating condition. Thus, the LDMOS was sensitive to latchup-like issue.

The typical I-V characteristics of ESD protection devices are illustrated in Fig. 1. Breakdown voltage (V_{BD}) and supply voltage (V_{DD} or V_{CC}) of the internal circuits divide the plot into three parts. The middle part is the desired ESD protection window. The blue curve is an example of the desired ESD device's I-V characteristics. To get an effective ESD protection, the trigger voltage (V_{t1}) should be smaller than breakdown voltage (V_{BD}) of internal circuits. Furthermore, to avoid latchup issue, the holding voltage (V_h) should be greater than the supply voltage of the internal circuits. The on-resistance of an ESD protection device should be as small as possible to get a high ESD robustness. The I-V characteristics of ESD devices should fit into this window for both effective ESD protection and latchup-free design.

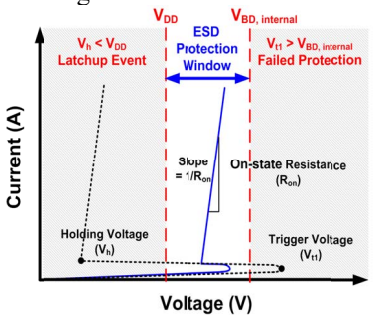
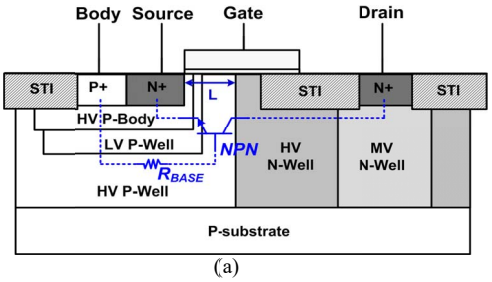


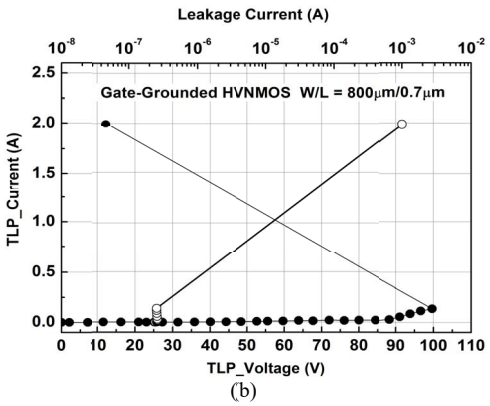
Fig. 1 The I-V characteristics of ESD protection device to meet ESD protection window.

II. ESD Robustness of HV MOSFET

The Reduced Surface Field (RESURF) technology can sustain high operating voltage under compact device size [3], therefore it has been integrated into the digital baseline CMOS processes to support the HV circuit operations with the low-voltage digital circuits together for the trend of SoC integration. To sustain the high voltage in the specified applications without junction breakdown, the lightly-doped diffusion layers were used to surround the drain or source region of HV MOSFET. However, the lightly-doped diffusion layers are also with high resistance that causes seriously negative impact to the ESD robustness of such HV devices.



(a)



(b)

Fig. 2 (a) Device structure of the HV nLDMOS in a 0.25-μm 5-V/60-V BCD process. (b) TLP-measured I-V curves of the gate-grounded HV nLDMOS with W/L of 800μm/0.7μm.

The device structure of a 60-V n-type lateral diffused MOS (nLDMOS) device in a 0.25-μm 5-V/60-V BCD process is drawn in Fig. 2(a). The TLP-measured *I-V* curve of the gate-grounded 60-V nLDMOS with device dimension (W/L) of 800μm/0.7μm is shown in Fig. 2(b). The failure current of this HV nLDMOS is only ~0.2 A with the corresponding HBM ESD level of only ~300V, even if its channel width was as large of 800 μm. Due to the consideration on the safe operating area (SOA) [4], the triggering of parasitic BJT NPN device in this HV nLDMOS is restrained by reducing the base resistance

(R_{BASE}) with the multiple p-well layers under source side, as well as weakening the kirk effect (base push-out effect) with MV (medium-voltage) n-well layer under drain side. The self-protection ability for such HV device against ESD stress becomes very weak. Therefore, additional ESD protection solution must be added into the chip to provide the desired ESD specification, such as ± 2 kV in HBM ESD test.

III. ESD Protection Solutions

A. Protection with embedded SCR device

To improve ESD robustness of HV nLDMOS, the SCR (p-n-p-n) device structure can be embedded into it by simply inserting one additional P+ diffusion in the drain region of the nLDMOS [5]. Although the embedded SCR has been proven as an excellent approach for increasing ESD robustness, mis-triggering of the embedded SCR during normal circuit operating conditions can bring other application reliability concerns. A substantially narrowed SOA had been found due to the insertion of SCR into HV nLDMOS, although the embedded SCR provides superior ESD robustness to protect the output HV array. A poly-bending layout structure for SCR-nLDMOS was reported to further widen the SOA of the nLDMOS array with embedded SCR [6]. Both the high ESD robustness and the improved SOA of circuit operation can be achieved by the poly-bending layout in the nLDMOS array.

B. Protection with stacked LV devices

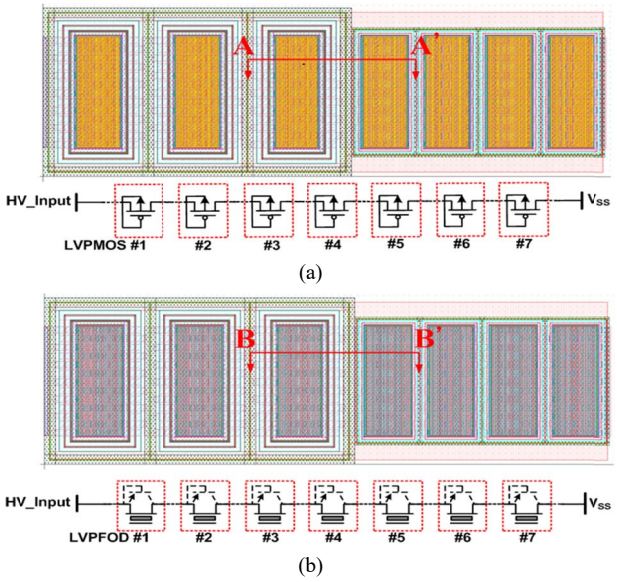


Fig. 3 Layout top view of (a) 7 stacked LV-PMOS and (b) 7 stacked LV-PFOD, respectively.

To fit in the ESD protection window (as shown in Fig.1) for both effective ESD protection and latchup-free design, the stacked configuration of LV devices is an useful way to achieve a high holding voltage for ESD protection in HV applications [7], [8]. For 60-V circuit applications, the layout top view of 7 stacked devices with LV-PMOS and LV-PFOD are shown in Figs. 3(a) and 3(b), respectively [9]. The total holding (trigger) voltage of stacked LV devices is the multiple of the holding (trigger) voltage of single LV device. Therefore, the trigger voltage and the holding voltage of stacked configuration can be adjusted to meet different HV applications. The device dimension of each LV-PMOS (PFOD) is chosen as W/L of 2400μm/0.5μm with minimum layout spacing at drain and source sides in a 0.25-μm HV BCD process to minimize the silicon area. The TLP-measured I-V curves of these two stacked structures are shown in Fig. 4, where the failure current (I_{t2}) of stacked LV-PMOS and LV-PFOD are 5.37 A and 5.18 A, respectively.

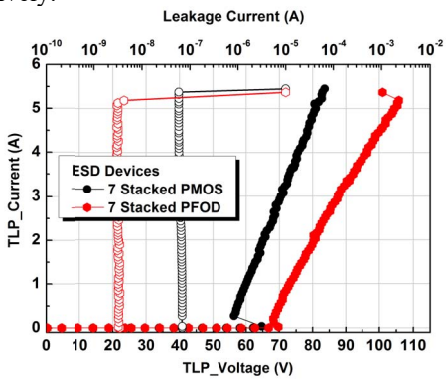


Fig. 4 TLP-measured I-V curves of stacked LV-PMOS (black dot) and LV-PFOD (red dot).

Acknowledgment

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References

[1] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain-extended MOS devices," *IEEE Trans. Device and Mater. Reliab.*, vol. 12, no. 4, pp. 615-625, Dec. 2012.

[2] W.-Y. Chen, M.-D. Ker, and Y.-J. Huang, "Investigation on the validity of holding voltage in high-voltage devices measured by transmission-line-pulsing (TLP)," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 762–764, Jul. 2008.

[3] R. Bianchi, F. Monsieur, F. Blanchet, C. Raynaud, and O. Noblanc, "High voltage devices integration into advanced CMOS technologies," *IEEE Int. Electron Device Meeting (IEDM)*, 2008, pp. 1-4.

[4] W.-Y. Chen and M.-D. Ker, "Characterization of SOA in time domain and the improvement techniques for using in high-voltage integrated circuits," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 382–390, Jun. 2012.

[5] J.-H. Lee, J.-R. Shih, C.-S. Tang, K.-C. Liu, Y.-H. Wu, R.-Y. Shiue, T.-C. Ong, Y.-K. Peng, and J.-T. Yue, "Novel ESD protection structure with embedded SCR LDMOS for smart power technology," in *Proc. of IEEE Int. Reliab. Phys. Symp.*, 2002, pp. 156–161.

[6] W.-Y. Chen and M.-D. Ker, "Improving safe operating area of nLDMOS array with embedded silicon controlled rectifier for ESD protection in a 24-V BCD process," *IEEE Trans. on Electron Devices*, vol. 58, no. 9, pp. 2944-2951, Sep. 2011.

[7] M.-D. Ker and K.-H. Lin, "The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1751-1759, Aug. 2005.

[8] K.-N. Tang, S.-F. Liao, M.-D. Ker, H.-C. Chiou, Y.-J. Huang, C.-C. Tsai, Y.-N. Jou, and G.-L. Lin, "Stacked low-voltage PMOS for high-voltage ESD protection with latchup-free immunity," in *Proc. of APEMC*, 2015.

[9] C.-T. Dai and M.-D. Ker, "ESD protection design with stacked low-voltage devices for high-voltage pins of battery-monitoring IC," *Proc. of IEEE Int. System-on-Chip Conf.*, 2015, pp. 380-383.