Design of High-Voltage-Tolerant Level Shifter in Low Voltage CMOS Process for Neuro Stimulator

Zhicong Luo[1,2] and Ming-Dou Ker[1]
[1]Biomedical Electronics Translational Research Center, National Chiao-Tung University, Taiwan
[2]The College of Mechanical and Electronic Engineering, Fujian Agriculture and Forestry University, China

***Abstract*—A new high-voltage-tolerant level shifter is proposed and verified in a 0.18-μm CMOS process with 1.8-V/3.3-V devices, whereas the operation voltage can be up to 12V. The output signal of high-voltage-tolerant level shifter has an offset of 3 times the normal supply voltage (V_{DD}) of the used technology with respect to the input signal. The converting speed of level shifter is improved by using the coupling capacitors and the cross-coupled transistor pairs. Electrical overstress and the gate-oxide reliability issues can be fully eliminated because all transistors in the proposed level shifter are operating within the safe voltage range.**

I. Introduction

Neuro-Stimulator has been widely used in the cardiac pacemaker, cochlear implant, bladder stimulation, neuromuscular electrical stimulation, deep brain stimulation, implantable visual prosthesis, and so on [1], [2]. In general, there are three methods to control the charge injection from the electrodes into the electrolyte, which are (1) the voltage-controlled stimulation (VCS), (2) the switched-capacitors stimulation (SCS), and (3) the current-controlled stimulation (CCS). CCS is the most favorable method because of its precise charge balance and safe operation. The required supply of stimulator varies from a few volts to tens volts. There are two approaches to design a high-voltage-tolerant stimulator. One approach is to use the high voltage (HV) process at the expense of the area and power consumption. The other approach is to use the concept of stacked devices, realized in low voltage (LV) CMOS process, with the dynamic bias voltage to withstand the high supply voltage. The objective of high voltage design in LV CMOS process is to make sure the transistors be in the safe operating region. In other word, the maximum voltages across the terminals of the transistors should be kept within the normal supply voltage (V_{DD}) [3], [4]. One of the advantages of this approach is that the neuro stimulator can be fully integrated with the microcontroller or the biomedical signal processor into a SoC chip fabricated in a LV CMOS technology.

Fig. 1 shows a type CCS-based neuro stimulator with $n\times V_{DD}$ supply realized in LV CMOS process. The outer transistors (M_A, M_B, M_C, and M_D) are controlled by the level shifter which converts the low-level voltage to the high-level voltage with an DC offset of $(n-1)\times V_{DD}$. When the transistors (M_A and M_D) are turned on, and the transistors (M_B and M_C) are turned off, cathodic electrode C_E is pulled down to ground. The stimulus current I_{STIM} flows into the tissue through the anodic electrode W_E. If sufficient charges are injected into the working electrodes, it will depolarize the membrane of the tissue to the threshold, and produce an unidirectional propagating action potential signal. The self-adaption bias circuit ensures that every stacked transistor in the high-voltage-tolerant buffer is in its safe operating region during the operation.

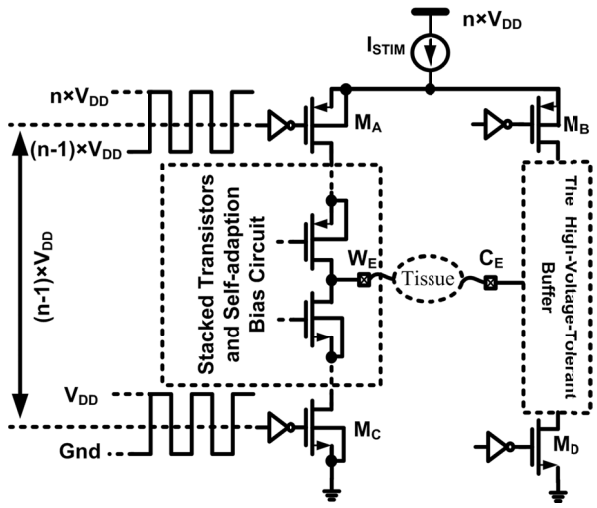

Fig. 1. A CCS-based neuro stimulator with its control signals.

The prior circuit topologies of high-voltage-tolerant level shifter in LV technologies suffered the large delay between the input and output siganl. In addition, the high-voltage-tolerant level shifter with the stacking transistors in LV CMOS process may have the start-up issue during the power-on transition. In the worst case, the level shifter may not work properly. In this work, a new 12V-tolerant level shifter is designed with 1.8-V/3.3-V devices and successfully verified in a 0.18-μm CMOS process.

II. Conventional Level Shifter Circuits

A conventional voltage level shifter realized in HV process is shown in Fig. 2. Four HV devices and two bias voltages (Biash and Biasl) are used to limit the voltage swing on the nodes O1 and O2. But, the HV devices should be manufactured by using the standard CMOS process with some special layout techniques and HV layers. The layout area of the level shifter is disadvantageously increased. Fig. 3 shows the conventional high-voltage-tolerant voltage level shifters with stacked MOS configuration in LV CMOS process. The operation is similar to the original circuit except the stacked inverters. Fig. 3(a) suffers from the large delays between the input and output, because its

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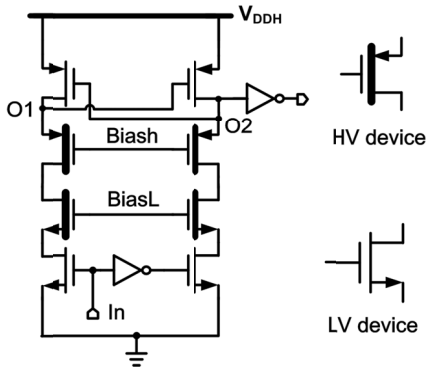

Fig. 2. A conventional voltage level shifter circuit in HV process. The HV devices should be manufactured by using the standard CMOS process with some special layout techniques and the HV layers.

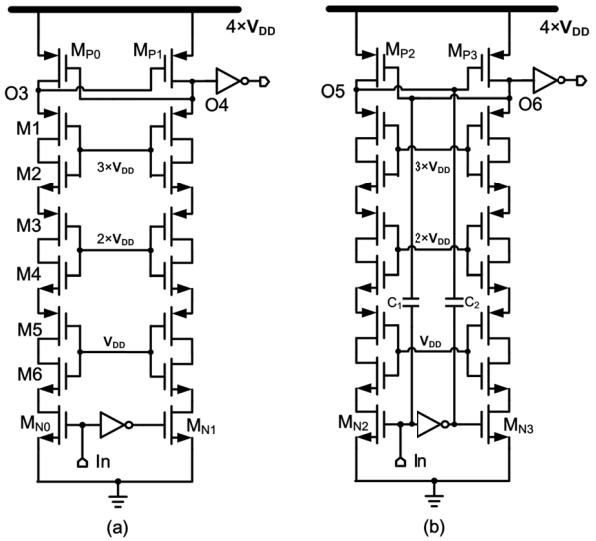

Fig. 3. (a) Conventional $4\times V_{DD}$ voltage level shifter circuit in LV process. (b) The $4\times V_{DD}$ voltage level shifter circuit with coupling capacitors. The start-up circuit is necessary.

pull-down ability is limited by the stacked transistors. In addition, the electrical overstress on the transistors may occur during the circuit switching operation.

The conventional $4\times V_{DD}$ voltage level shifter circuit with coupling capacitors to enhance the converting speed is shown in Fig. 3(b). Fig. 4 shows the simulation result of the drain-to-source voltage (V_{DS}) for all devices in the conventional design of Fig. 3(a). The input signal (In) switches between 0V and V_{DD} (3V), the simulation result shows that the maximum transient V_{DS} is about 4.2V which appears during the circuit switching operation. The peak voltage appears in the circuit switching operation and the delay can be improved significantly by using the level shifter with the coupling capacitors, as that shown in Fig. 3(b).

The conventional level shifters in Fig. 3 may suffer the start-up issue during the power-on transition, especially with the coupling capacitors. In the worst case, the stacked LV devices may be damaged. For example, when the power supply rises from 0V to $4\times V_{DD}$, the voltage on the node O5 (or O6)

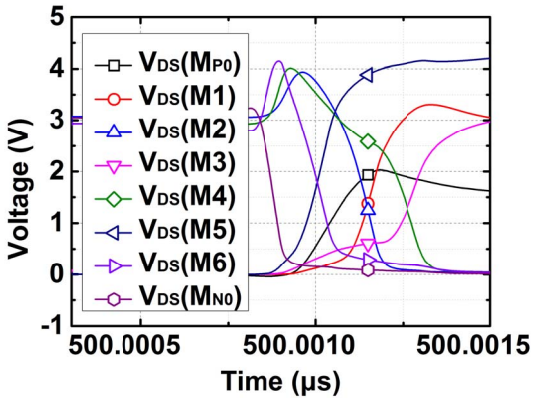

Fig. 4. V_{DS} simulation results among the devices in Fig. 3(a). V_{DS}(M6) is the drain-to-source voltage of the transistor M6. Obviously, electrical overstress appears in the circuit switching operation.

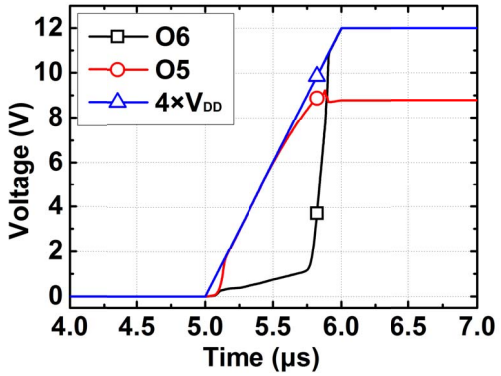

Fig. 5. The voltages on the nodes O5, O6, and the $4\times V_{DD}$ power supply port in Fig. 3(b) during the power-on transition. The electrical overstress on the transistors (M_{P2} and M_{P3}) occurs in the power-on transition.

may be pulled up to the high supply voltage. So, transistor M_{P3} (or M_{P2}) is turned off, that means, the drain current (leakage current) of transistor M_{P3} (or M_{P2}) is very small. Thus, the node O6 (or O5) is charged up slowly. If the charged up time is longer than the rising time of supply voltage, the voltages across the terminals of transistors M_{P3} and M_{P2} may exceed the safe voltage range of $1\times V_{DD}$. Fig. 5 shows the simulation result of the voltages on the nodes O5 and O6 during the power-on transition. In Fig. 5, the voltage on node O5 rises rapidly by following the power supply in the beginning, but the voltage on node O6 rises slowly. Thus, the electrical overstress on the transistors (M_{P2} and M_{P3}) occurs, the devices may be damaged. The start-up circuit should be designed to avoid such electrical overstress during the power-on transition.

III. Design of New Level Shifter Circuit

The new high-voltage-tolerant level shifter is shown in Fig. 6. The capacitor C_3 (C_4) couples between the node O9 (O10) with the node O7 (O8), respectively. If the input control signal (In) switches from low (0 V) to high (V_{DD}), the voltage at node O8 couples up with a factor ΔV, which is expressed approximately as

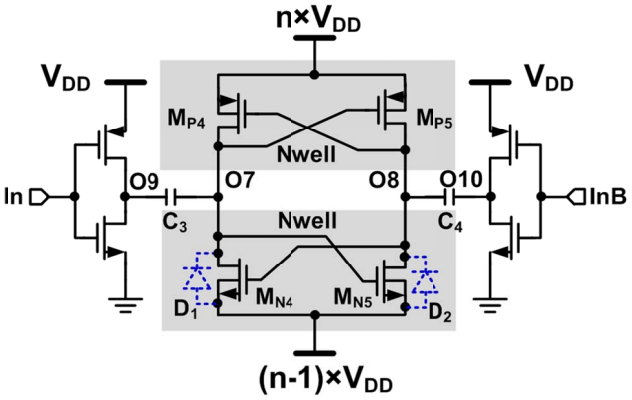

Fig.6. The proposed level shifter in LV CMOS process. In this work, n is 4, V_{DD} is 3V. The bias voltage (n-1)×V_{DD} can be supplied by the resistive voltage divider with low DC current. The start-up circuit is unnecessary.

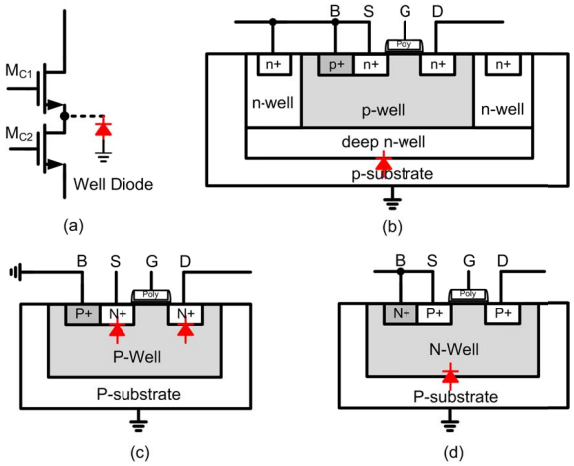

Fig.7. (a) Connection of two stacked transistors. (b) NMOS devices in deep n-well and the parasitic well diode. (c) NMOS device and the parasitic well diode. (d) PMOS device and the parasitic well diode.

$$\Delta V = \frac{C_4 \cdot V_{DD}}{C_4 + C_{par}}, \quad (1)$$

where C_{par} is the parasitic capacitance at the node O8. On the contrary, the voltage at the node O7 couples down with a factor ΔV. By well adjustment, the cross-coupled PMOS pair (M_{P4} and M_{P5}) and the cross-coupled NMOS pair (M_{N4} and M_{N5}) can switch faster from one state to the other. If the voltages on the nodes (O7 and O9) become lower than (n-1)×V_{DD}, the parasitic diodes (D_1 and D_2) will be turned on. Thus, the voltages on the nodes (O7 and O9) will be clamped to (n-1)×V_{DD}. In this way, the start-up circuit is unnecessary. The bias voltage (n-1)×V_{DD} can be supplied by the resistive voltage divider with low DC current.

The maximal operation voltage of the high-voltage-tolerant level shifter is limited by the breakdown voltage of the parasitic well diode [5]. Fig. 7 shows an example of two stacked transistors. For the deep n-well technologies, the breakdown voltages of NMOS transistor with deep n-well layer, NMOS transistor without deep n-well layer, and PMOS transistor are limited by the n-well/p-substrate diode, n+/p-well diode, and n-well/p-substrate diode, respectively. The breakdown voltage of the n-well/p-substrate diode is higher than that of the n+/p-well diode. For example, the reverse breakdown voltage of the n+/p-well diode is ~ 10 V in a 0.18-μm 1.8-V/3.3-V CMOS process. Thus, the new 4×V_{DD} level shifter is realized with the 3.3-V PMOS transistors and the 3.3-V NMOS transistors with a deep n-well layer, and all of the bodies of the transistors are connected to their source terminals, respectively.

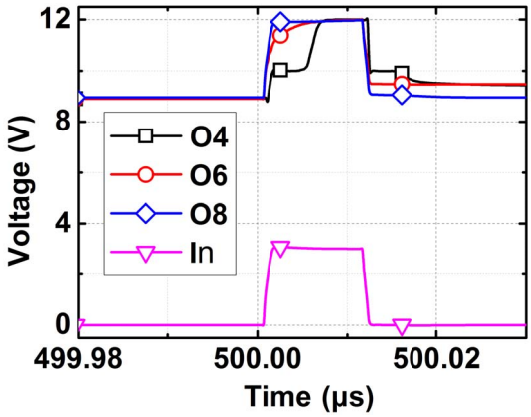

Fig. 8. Input-output characteristics of the level shift circuits shown in Fig. 3(a), Fig. 3(b), and Fig. 6.

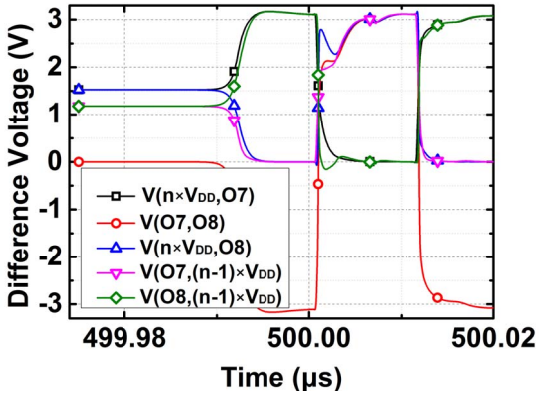

Fig. 9. V_{DS}, V_{GS}, and V_{DS} simulation results of all the devices in Fig. 6. V(n×V_{DD}, O7) denotes the difference voltage between the power supply and node O7. The voltages across the terminals of every transistor are kept within the safe voltage range of 1×V_{DD} during the operation.

Fig. 8 compares the input-output characteristics of the level shift circuits shown in Fig. 3(a), Fig. 3(b), and Fig. 6. A pulse signal, shown in the bottom of Fig. 8, is applied to the input port of the level shifters. It can be clearly found that the new high-voltage-tolerant level shifter of Fig. 6 switches quickly. Fig. 9 shows the V_{DS}, V_{GS}, and V_{DS} simulation results of all the devices in Fig. 6. Obviously, all transistors in the new level shifter are operating within the safe voltage range of 1×V_{DD}.

Table I gives a comparison of the delays among the three topologies. T_{dlh} is defined as a delay in the rising edge, and T_{dhl} is defined as a delay in the falling edge. It can be found that the delay of the new level shifter relates to the coupling capacitor. When the coupling capacitor is larger, the delay of level shifter

TABLE I
COMPARISON OF THE DIFFERENT TOPOLOGIES

Condition	Parameters	Level shifter in Fig. 3(a)	Level shifter in Fig. 3(b)	This work (Fig.6)
C_1= C_2= C_3=C_4=0.9pF	T_{dlh}	4500ps	16ps	11ps
	T_{dhl}	304ps	2.2ps	3.2ps
C_1= C_2= C_3=C_4=0.1pF	T_{dlh}	4500ps	980ps	86ps
	T_{dhl}	304ps	60ps	32ps
	Number of devices in core circuit	16	18	6
	Start-up circuit	Necessary	Necessary	Unnecessary

is smaller. In addition, only six devices are used in the core circuit of the new proposed level shifter.

IV. EXPERIMENTAL RESULTS

The neuro stimulator designed with the new level shifter of Fig. 6 has been fabricated in a 0.18-μm 1.8V/3.3V CMOS process, which is also verified in the animal trials. In this experiment, the electrodes were bilaterally implanted over the area of the right side zona incerta of the Long-Evans rat. The output ports of the stimulator and the electrodes are connected with the Teflon-insulted stainless steel wire [1].

Fig. 10 shows an oscilloscope capture of the voltages on the electrodes. During 0–2500μs, the outer transistors (M_A, M_B, M_C, and M_D in Fig. 1) are turned off by the level shifter. The voltages on the electrodes (C_E and W_E in Fig. 1) are 0 V. Then, during 2500–3000μs, the cathodic stimulation starts, the transistors (M_A and M_D) are turned off, and the transistors (M_B and M_C) are turned on, the voltage on the cathodic electrode rises up to 12V. It can be clearly verified that the level shifter operates properly according the timing sequence.

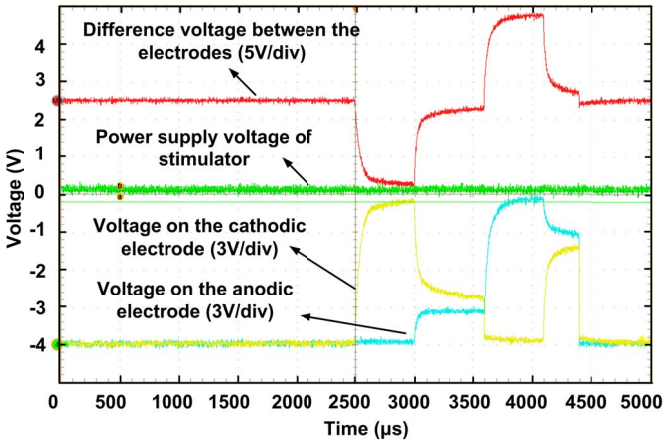

Fig. 10. The measured voltages on the electrodes during animal test by the neuro stimulator with 50-μA stimulus current. The supply voltage of the neuro stimulator is up to12V.

V. CONCLUSION

A high-voltage-tolerant and high speed level shifter has been designed and successfully verified in a 0.18-μm 1.8-V/3.3-V CMOS process. The new proposed level shifter converts the low-level voltage to the high-level voltage with DC offset of 3 times V_{DD}. Reliability is guaranteed because the voltages across the terminals of every transistor are kept within the safe voltage range of $1\times V_{DD}$ during the operation. High converting speed is achieved by using the coupling capacitors and the cross-coupled MOS pairs. The core circuit of the new level shifter consists of two capacitors, two PMOS transistors, and two NMOS transistors. The number of transistors used in the new level shifter is the least among the prior level shifters.

VI. ACKNOWLEDGMENT

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