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ESD Protection Design with Low-Leakage Consideration for Silicon Chips of IoT Applications

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***Abstract*—On-chip electrostatic discharge (ESD) protection design with low-leakage consideration for the silicon chips of IoT applications is presented. The proposed ESD protection design uses the fast turn-on silicon-controlled rectifier (SCR) device to implement the power-rail ESD clamp circuit. Experimental results verified in TSMC 28nm CMOS process have shown that the proposed design has advantages of low leakage current (2~3nA), low trigger voltage (~2V), high ESD robustness (>8kV), and free to latchup issue.**

Keywords— CMOS ; electrostatic discharge (ESD); ESD protection; low-leakage.

I. Introduction

The low-power integrated circuits (ICs) are needed for the internet of things (IoT) applications. Therefore, the electrostatic discharge (ESD) protection circuits with the feature of low leakage / low power are needed for the silicon chips of IoT applications [1]. However, the ICs are very sensitive to ESD events, especially those fabricated by the advanced nanoscale CMOS technology [2]. To provide the required ESD robustness for silicon chips of IoT applications, where the IoT environments would be the fields without any ESD control, the ESD protection circuits should be equipped at all pads of a chip which may be stressed by ESD pulses.

The ESD protection circuit should be carefully designed into an ESD design window, as shown in Fig. 1 [3]. The ESD design window is defined by the power-supply voltage (V_{DD}) and the gate-oxide breakdown voltage (V_{BD}) of MOSFET with typically 10~20% buffer zones. Therefore, the trigger voltage (V_{t1}) and holding voltage (V_h) of ESD protection circuit must be lower than 0.8x ~ 0.9x V_{BD} to prevent the internal circuits from damage before the ESD protection circuit is turned on during ESD stresses. Besides, the V_{t1} and the V_h must be higher than 1.1x ~ 1.2x V_{DD} to prevent the ESD protection circuit from being mis-triggered under normal-circuit-operating conditions. Moreover, the turn-on resistance (R_{on}) of ESD protection circuit should be minimized to reduce the joule heat generated in the ESD protection circuit and the clamping voltage of the ESD protection circuit during ESD stresses. For a 28nm CMOS technology, the ESD design window should be within ~1V and ~5V [4].

To achieve effective ESD protection, the typical whole-chip ESD protection design for silicon chips is shown in Fig. 2, where the power-rail ESD clamp circuit is the key circuit to achieve whole-chip ESD protection [5]. In addition, with the advantages of high ESD robustness, compact layout area, and latchup free in low-voltage applications, the silicon-controlled rectifier (SCR) device has been reported to be a useful component for on-chip ESD protection in CMOS ICs [6]. The conventional SCR device in CMOS processes consists of a P+ region, N-well, P-well, and N+ region. To efficiently discharge the ESD current from anode to cathode through the SCR device, several gate-bounded SCR devices had been reported [7]-[9]. The ability of SCR device that can be quickly triggered on to clamp the overstress voltage to a safe low voltage level is one of the major important design considerations for on-chip ESD protection in the advanced CMOS processes. Thus, an effective design to reduce the trigger voltage of SCR device is needed.

In this work, two fast turn-on SCR devices with low trigger voltage, low leakage current, free to latchup, and fully process-compatible to general CMOS processes are proposed. Such fast turn-on SCR devices are used in the power-rail ESD clamp circuits to sustain high ESD stress in the IoT field applications.

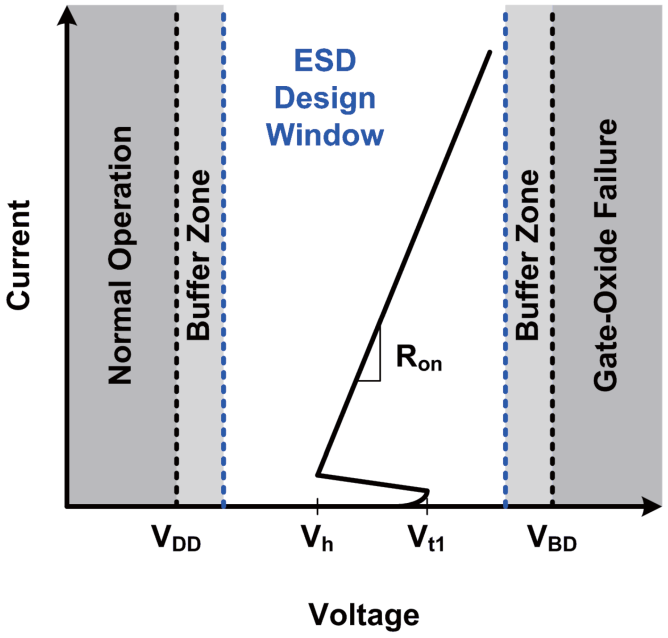


Fig. 1. ESD design window defined by the power-supply voltage (V_{DD}) and the gate-oxide breakdown voltage (V_{BD}) with 10~20% buffer zones.

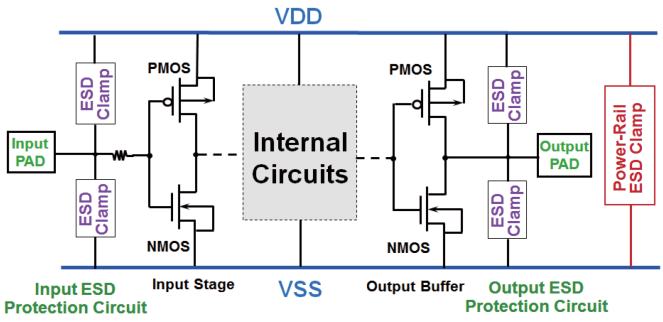


Fig. 2. Whole-chip ESD protection with I/O and power-rail ESD clamp circuits.

II. Conventional SCR Device for ESD Protetion

The device structure of the conventional SCR device used between V_{DD} and V_{SS} is illustrated in Fig. 3(a). The V_{DD} pad is connected to the first P+ and the pickup N+, which are formed in the N-well. The V_{SS} pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The SCR path between V_{DD} and V_{SS} consists of P+, N-well, P-well, and N+. The equivalent circuit of the SCR consists of a PNP BJT (Q_{PNP}) and an NPN BJT (Q_{NPN}), as shown in Fig. 3(b). The Q_{PNP} is formed by the P+, N-well, and P-well, and the Q_{NPN} is formed by the N-well, P-well, and N+. As ESD zapping from V_{DD} to V_{SS}, the positive-feedback regenerative mechanism of Q_{PNP} and Q_{NPN} results in the SCR device highly conductive to make SCR very robust against ESD stresses. Under normal circuit -operating conditions, the SCR path remain off to prevent from leakage. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent into the base terminal of Q_{NPN} to enhance the turn-on speed. The voltage level of the trigger port is in reverse proportion to the trigger voltage of the SCR device. Therefore, some circuit design techniques are reported to enhance the turn-on efficiency of SCR devices [7]-[20]. However, an SCR device with a low trigger voltage, low leakage current, and which requires no additional process step for ESD protection is still needed.

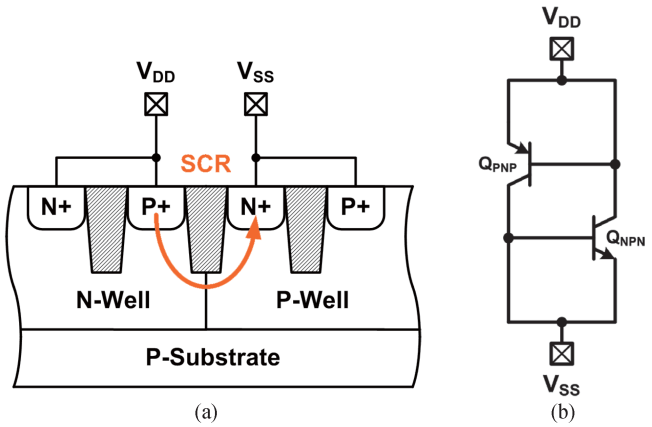


Fig. 3. (a) Device cross-sectional view, and (b) equivalent circuit, of SCR device used between V_{DD} and V_{SS}.

III. Proposed Low-Leakage-Current and Fast-Turn-on SCR Device for ESD Protetion

Two low-leakage-current and fast-turn-on SCR devices (P-SCR and N-SCR) are presented in this work. In each fast turn-on SCR device, two gates are embedded into device structure to separate its anode and cathode. One gate lies on the N-well/P-well junction, and the other lies on the N-well (P-well) to form a PMOS (NMOS) in the P-SCR (N-SCR) device, as shown in Figs. 4(a) and 4(b), respectively. To reduce the turn-on voltage of the P-SCR (N-SCR) device under ESD stress conditions, the gates in P-SCR (N-SCR) device are controlled by the ESD detection circuit. As shown in Fig. 4, both ESD detection circuits consist of a resistor-capacitor (R-C) timer and two inverters to generate the trigger voltages at the nodes of T1 and T2. The trigger mechanism of both P-SCR and N-SCR devices are similar. When ESD pulse is zapping to V_{DD} with V_{SS} grounded, the T1 is initially kept at high voltage to induce the N-type channel, and T2 is initially kept at low voltage to induce the P-type channel. These two induced channels form the trigger currents to trigger SCR on. The turned-on SCR can discharge ESD current efficiently to protect the internal circuits inside the silicon chip. Under the normal circuit -operating conditions, the voltage levels of T1 and T2 nodes remain at V_{SS} and V_{DD}, respectively, those keep SCR off. The leakage current through the SCR in off state is very small.

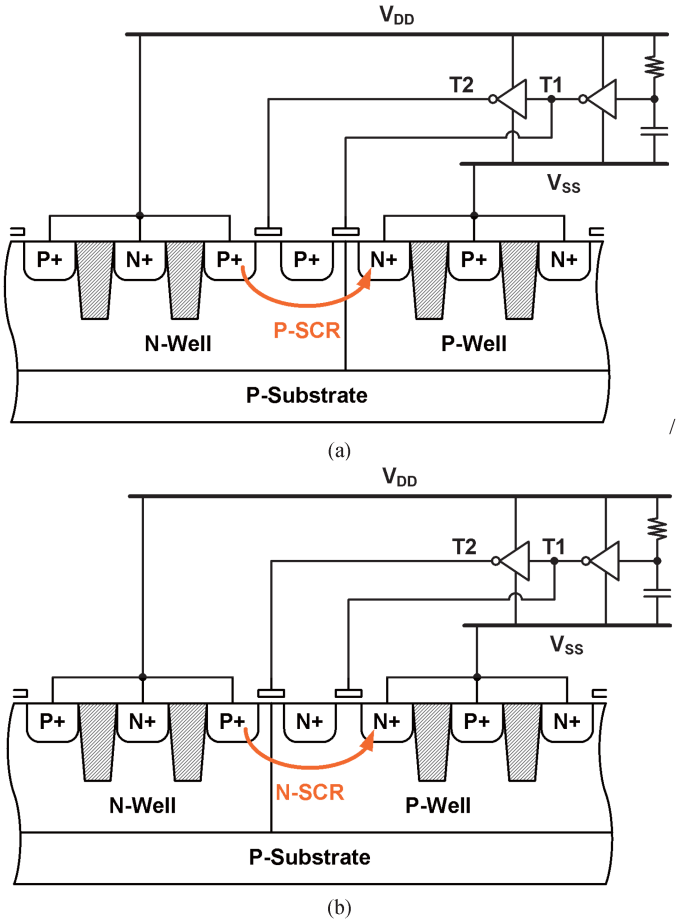


Fig. 4. Proposed ESD protection design with (a) P-SCR and (b) N-SCR.

IV. Experimental Results

Both power-rail ESD clamp circuits designed with P-SCR and N-SCR devices have been fabricated in a TSMC 28nm CMOS process. The dimension (width) of each SCR device is drawn as 120μm in layout, the RC time constant is 100ns, and the width of PMOS (NMOS) in each inverter is 14μm (6μm).

The human-body-model (HBM) ESD robustness of each circuit is tested. Both the circuits with P-SCR and N-SCR have been double confirmed to pass the HBM ESD test of 8kV.

A transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used to investigate the I-V characteristics of the test devices. Figure 5 shows the TLP-measured I-V curves of both ESD circuits. The P-SCR and N-SCR can be triggered on at ~2V. After TLP tests, the scanning electron microscope (SEM) was used to find the failure locations. Figure 7 shows the SEM photographs of P-SCR device after TLP tests. The failure points are located at the SCR paths.

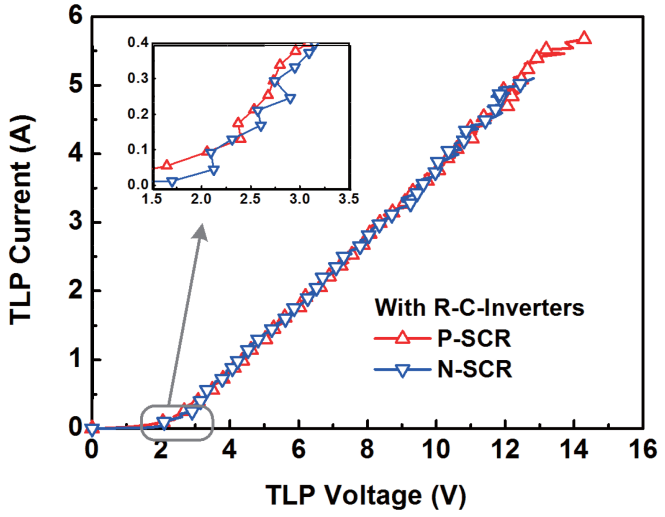


Fig. 5. TLP-measured I-V curves of the proposed ESD protection design with P-SCR or N-SCR.

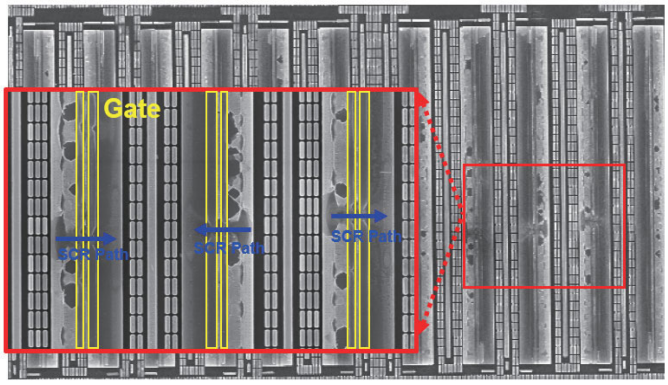


Fig. 6. SEM photo of P-SCR after TLP tests.

Another very-fast TLP (VF-TLP) system with 0.2-ns rise time and 5-ns pulse width is used to evaluate the effectiveness of the proposed devices in faster ESD -transient events (charged-device-model, CDM). Figure 7 shows the VF-TLP-measured I-V curves of both ESD circuits, where both P-SCR and N-SCR can be turned on fast enough to provide CDM ESD protection.

The P-SCR (N-SCR) has a holding voltage of ~1.7V (1.5V) that prevent the latchup issue in the given 28nm CMOS process with V_{DD} of 1.05V for normal circuit operations. To verify latchup immunity, the fabricated ESD protection circuits are tested by the transient-induced latchup (TLU) method [21]. Figure 8 shows the measured transient voltage waveforms of the ESD circuits under TLU test with a charging voltage of 10V. After the TLU tests, the voltage across the ESD circuits are still stayed at 1.05V (V_{DD}). Based on the TLU test results, the proposed ESD circuits with P-SCR (N-SCR) are confirmed to immune from the latchup issue.

Under normal circuit operating conditions with V_{DD} of 1.05V, the leakage current of the fabricated ESD circuit with P-SCR (N-SCR) is measured and listed in Table I, which is very small of only 3.1nA (2.5nA).

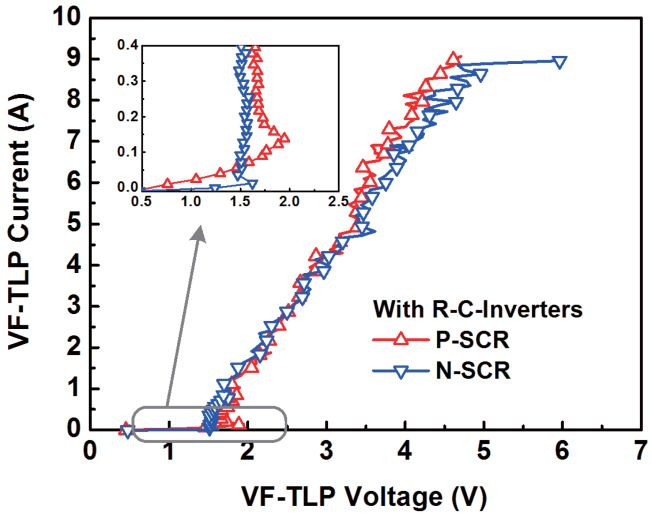
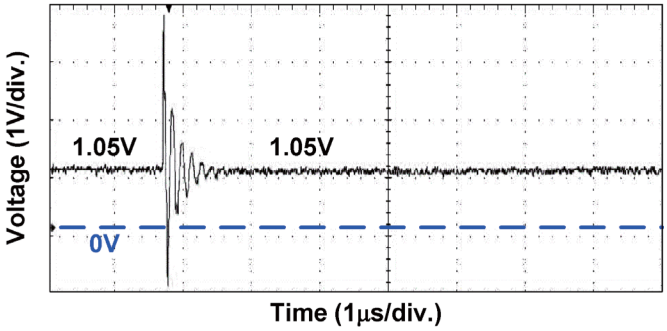


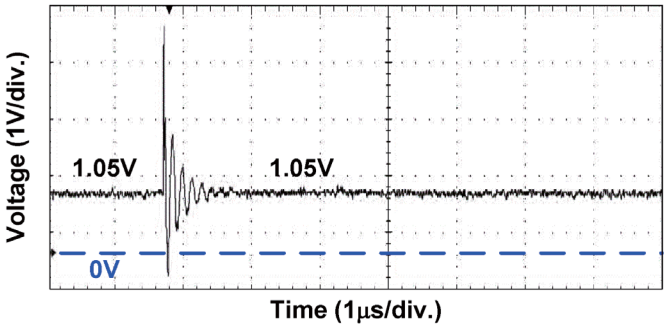
Fig. 7. VF-TLP-measured I-V curves of the proposed ESD protection design with P-SCR or N-SCR.

Table I. Device Dimensions and Test Results of Proposed ESD Circuits.

ESD Protection Design	with P-SCR	with N-SCR
Device Width	120μm	120μm
HBM ESD Robustness	>8kV	>8kV
TLP I_{t2}	5.62A	5.05A
VF-TLP I_{t2}	8.98A	8.89A
Leakage at 1.05V (V_{DD})	3.1nA	2.5nA



(a)



(b)

Fig. 8. Measured voltage waveforms on the proposed ESD protection design with (a) P-SCR, and (b) N-SCR, under TLU tests.

V. Conclusion

On-chip ESD protection designs with P-SCR or N-SCR devices to achieve low leakage current, low trigger voltage, fast turn-on speed, high ESD level, and free to latchup are presented and successfully verified in a 28nm CMOS process. The proposed ESD protection solution is highly suitable for the silicon chips of IoT applications in nanoscale CMOS process.

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