ESD Protection Design on T/R Switch with Embedded SCR in CMOS Process

Tao-Yi Hung and Ming-Dou Ker
Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

***Abstract*- ESD protection design for the RF transmit/receive switch (T/R switch) with embedded silicon-controlled rectifier (SCR) is proposed, where the SCR device is embedded in the ESD diode and the transistors of T/R switch by layout skill. Silicon chip verified in a 90-nm CMOS process has been measured by TLP and HBM ESD test to confirm its efficiency for ESD protection. The parasitic capacitance from the ESD devices was also measured. Failure analysis by SEM was performed to find the burned-out site on the T/R switch with the proposed design. From the failure analysis SEM pictures, the embedded SCR in the proposed design is actually triggered on to discharge ESD current.**

I. Introduction

In recent years, RF transceivers have been widely integrated in a system on chip (SoC) for mass production with lower manufacturing cost. The RF transmit/receive front-end circuit plays an important role between antenna and mixer, including low noise amplifier (LNA), power amplifier (PA), and transmit/receive switch (T/R switch), as shown in Fig. 1 [1]-[4]. On the other hand, owing to the fast development of CMOS process technologies, MOS transistors have been scaled down rapidly, and therefore provide faster logic performance with lower energy consumption. However, with the thinner gate oxide in the scaled-down MOS devices, the threat from ESD phenomenon was not alleviated as technology advances. To solve this issue, ESD protection circuits such as conventional dual diodes and power-rail ESD clamp circuit must be co-designed with the RF transmit/receive front-end circuit together [5]. More precisely, due to the position between antenna and the transceiver circuits, the ANT node of T/R switch is very sensitive to ESD stress during module assembly. Therefore, ESD protection design on T/R switch requires a more efficient and effective way than ESD design on either LNA or PA [6], [7]. With the ESD protection circuit on T/R switch, the ESD current from antenna node is discharged to VDD or ground before it rushes into LNA or PA [8]-[10].

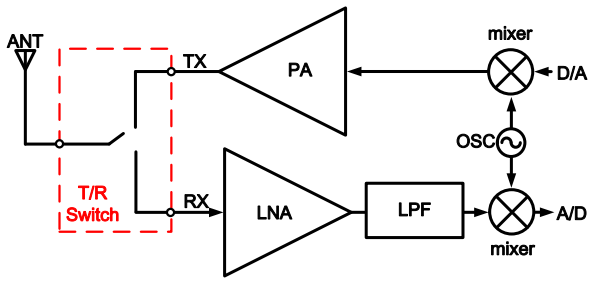


Fig. 1 RF transceiver front-end circuit with T/R switch.

In this work, the ESD protection design for T/R switch with embedded SCRs and power-rail ESD clamp circuit is proposed and implemented in a 90-nm CMOS process. The embedded SCRs are formed by conventional ESD diode and the shunt MOS transistors of T/R switch together, without additional layout area. With this approach, the proposed design can not only obtain higher failure current (It_2) in transmission line pulse (TLP) test, but also introduce lower parasitic capacitance, compared with the conventional dual-diode method under the same silicon area.

II. Design of T/R Switch

The schematics of a conventional T/R switch, as shown in Fig. 2, is the most commonly used topology [11]. By applying the control signal of logic 1 to V_{TX} (0 to V_{RX}), the T/R switch can be operated in the transmit mode (TX). On the contrary, with the control signal of logic 0 to V_{TX} (1 to V_{RX}), it is operated in the receive mode (RX).

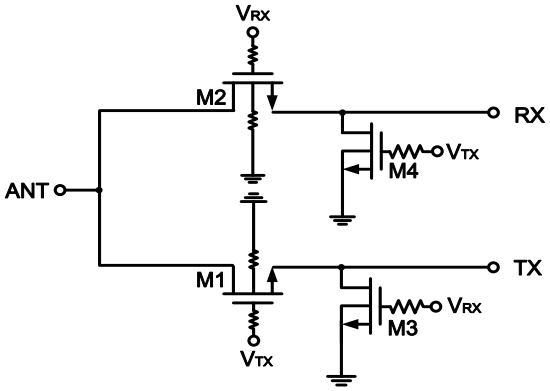


Fig. 2 Typical T/R switch circuit with no ESD protection.

Insertion loss (IL) is one of the most important specifications of receive mode in T/R switch, which is determined by the turn-on resistance (Ron) of the MOS transistors M1 and M2. Thus, the dimensions ratio, W/L, has to be large enough to make Ron as small as possible. However, with the increase in ratio of the transistors, the parasitic capacitances become larger as well. Other factors those can reduce the IL are the resistive body-floating technique [12] and deep N-well doping implantation in CMOS triple-well process [13]. They also reduce signal coupling to ground and prevent noise from the substrate.

The linearity of T/R switch is another major consideration in T/R front-end circuit, which indicates the power handling capability of the transmit mode. With large gate resistance of

the MOS transistors and stacked transistors architecture, the voltage stress on the gate oxide of transistors can be relieved by AC floating technique, and thus enhance the power handling capability of the T/R switch [14].

Last thing to be mentioned is the isolation of the T/R switch. M3 and M4 transistors in shunt with the RF signal path are chosen in a small size relatively. The mission of the transistors (M3 and M4) is avoiding PA signal leak to Rx in transmit mode, and antenna signal leak to Tx while operating in receive mode. In this work, the W/L ratios of M1 (M2) and M3 (M4) are designed with 200/0.1 and 12/0.1, respectively.

III. ESD PROTECTION DESIGN

Conventional ESD protection scheme for T/R switch with dual diodes and power-rail ESD clamp circuit is illustrated in Fig. 3. With appropriate device dimensions, the diode D1, diode D2, and power-rail ESD clamp circuit can provide enough ESD immunity against the four modes of ESD testing in HBM: positive I/O-to-VDD (PD), positive I/O-to-VSS (PS), negative I/O-to-VSS (NS), and negative I/O-to-VDD (ND). When PD or NS ESD zapping occurs, the diodes D1 or D2 operating in the forward-bias condition provide the discharging path for ESD current. As for PS and ND ESD zapping condition, the large transistor M_{ESD} of power-rail ESD clamp circuit will be triggered on by the RC (time constant of ~0.1us) detection mechanism to discharge ESD current. However, for higher frequency-band application, the parasitic capacitance beside the signal path must be further reduced, that in turn to reduce device dimensions of diodes D1 and D2. With the reduced device dimensions of diodes D1 and D2, their ESD robustness will be also degraded. As the T/R switch circuit implemented with all NMOS's (M1 ~ M4 in Fig. 2), the most critical ESD stress to cause damage is the positive-to-VSS (PS-mode) ESD stress. Therefore, how to enhance ESD robustness against PS-mode ESD stress, but without increasing the parasitic capacitance to the ANT node of T/R switch, has been a critical challenge to on-chip ESD protection design.

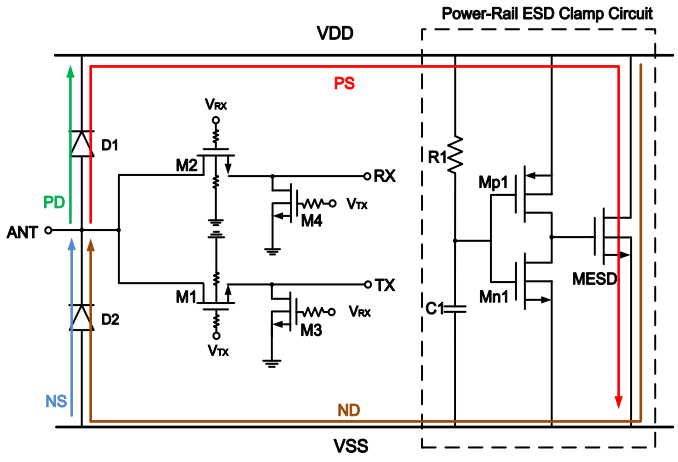
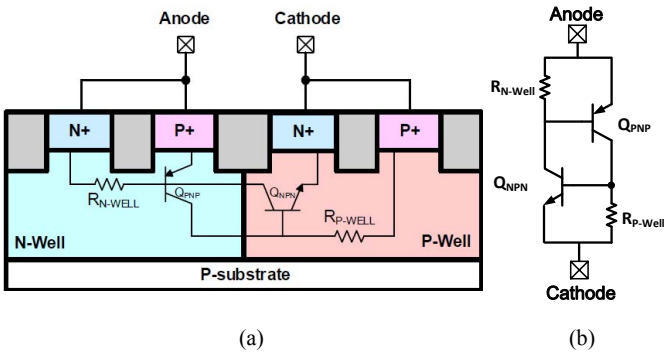
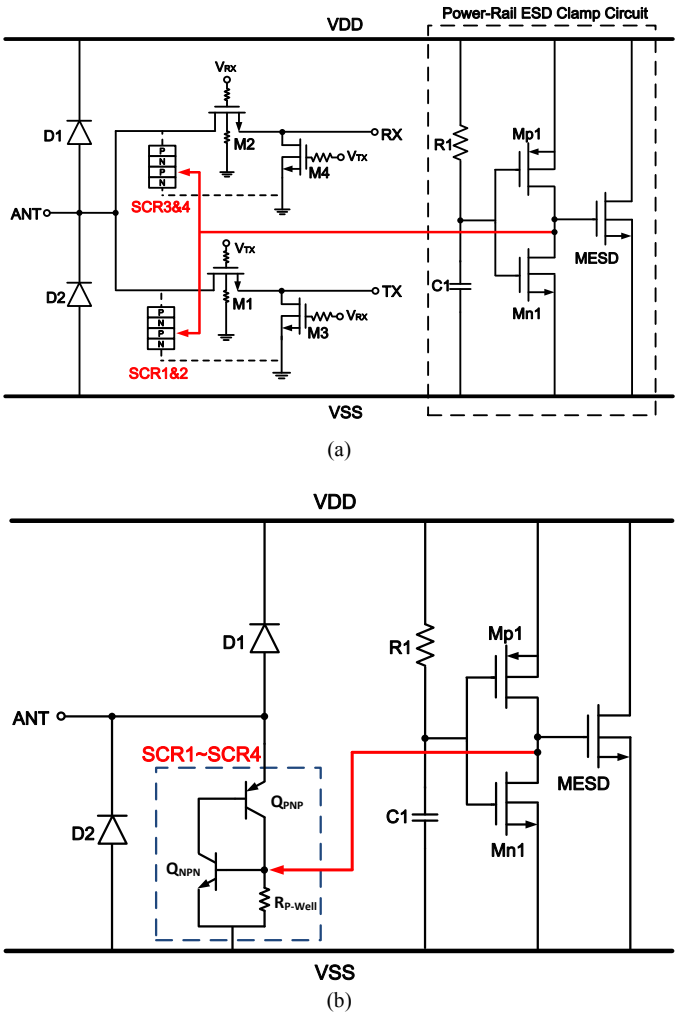


Fig. 3 Conventional ESD protection scheme for T/R switch with dual diodes and power-rail ESD clamp circuit.



(a) (b)

Fig. 4 (a) Cross-section view of SCR device and (b) its equivalent circuit.



(a)

(b)

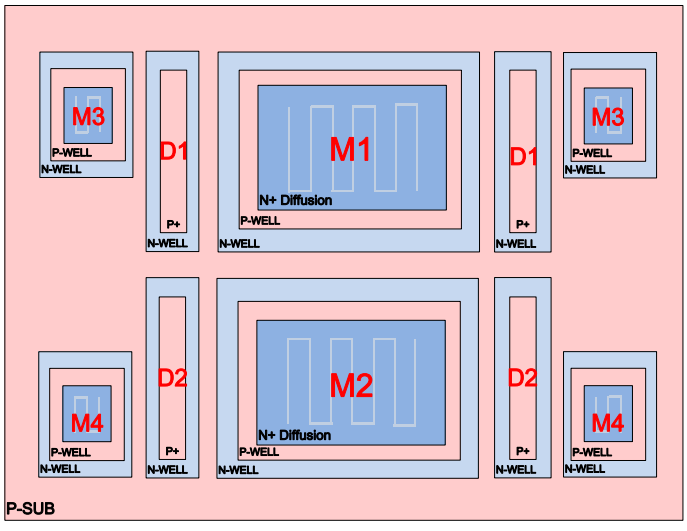
Fig. 5 (a) Proposed ESD protection design for T/R switch with dual diodes, embedded SCRs, and power-rail ESD clamp circuit. (b) Equivalent circuit of the proposed ESD protection design with embedded SCRs (SCR1 ~ SCR4).

Silicon-controlled rectifier (SCR) device, as shown in Fig. 4, has been a suitable ESD protection device in RF ICs due to its low parasitic capacitance and high ESD robustness. However, the turn-on voltage of SCR is usually higher than the oxide breakdown voltage of the transistors. The inner circuit will be damaged before the SCR start to pull down the ESD stress. Thus, an appropriate triggering method is needed. With a

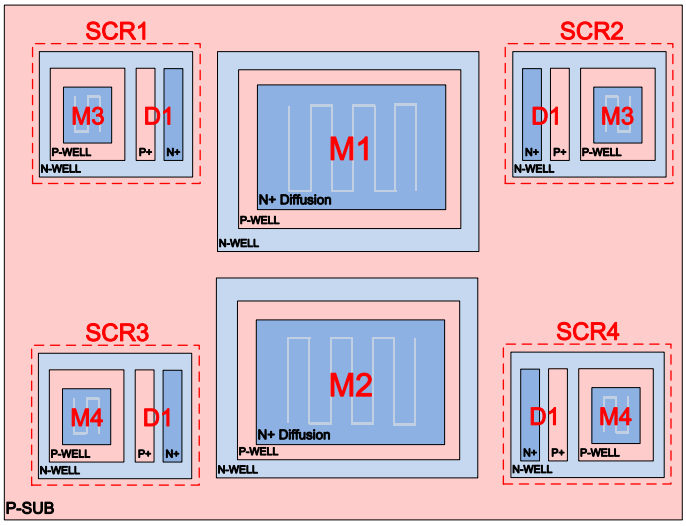
suitable triggering design, the SCR can be turned on quickly to sustain high ESD level in a small device dimension.

In this work, the proposed ESD protection circuit for T/R switch is shown in Fig. 5(a), where the four embedded SCRs (SCR1~SCR4) is used to enhance its PS-mode ESD protection without causing any additional capacitance to ANT node. Apart from the conventional ESD protection scheme in Fig. 3, the proposed design employed four SCRs embedded from the P+ anode of diode D1 to the N+ sources of M3 and M4 by layout skill. Fig. 5(b) indicates the equivalent circuit of the triggering mechanism. In PS-mode ESD zapping event, the RC detection circuit will trigger both embedded SCR and M_{ESD}, simultaneously. With the rising potential in the p-wells of M3 and M4, the parasitic bipolar junction transistors Q_{NPN} will turn on rapidly after the base to emitter voltage V_{BE} exceeds the turn-on voltage of the BJT, and begin a large amount of current conduction due to the Q_{PNP} and Q_{NPN} positive feedback mechanism. With the aid of the additional discharging path provided by the four SCRs, the ESD robustness in PS-mode can be effectively improved.

The layout of the conventional ESD protection and the new proposed ESD protection designs are realized by common centroid method, as illustrated in Fig. 6(a) and Fig. 6(b) respectively, to avoid process variation. Fig. 7(a) sketches the layout top view of one embedded SCR. Fig. 7(b) shows the cross-section view on X-X' line of Fig. 7(a), where the p-n-p-n structure is constructed by diode D1 and M3 naturally. The four embedded SCRs save the layout area by sharing the P+ diffusion of the D1 together which are connected to the antenna (ANT) port. The dimensions of transistors Mp1, Mn1, and M_{ESD} in the power-rail ESD clamp circuit are chosen as 300/0.35, 100/0.35, and 3000/0.35, respectively. Total junction area of the P+/NW diode D1, D2, and embedded SCRs are only 28 μm^2 to reduce the parasitic capacitance for RF applications.

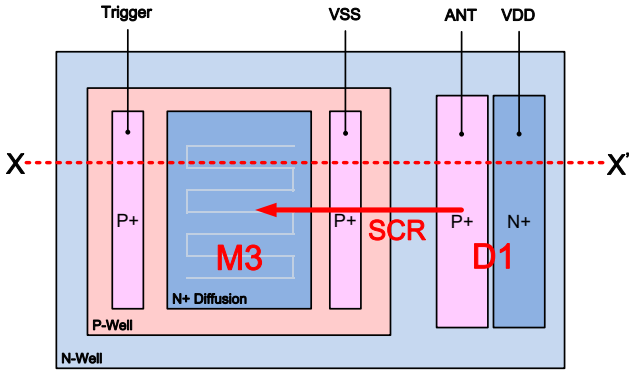


(a)

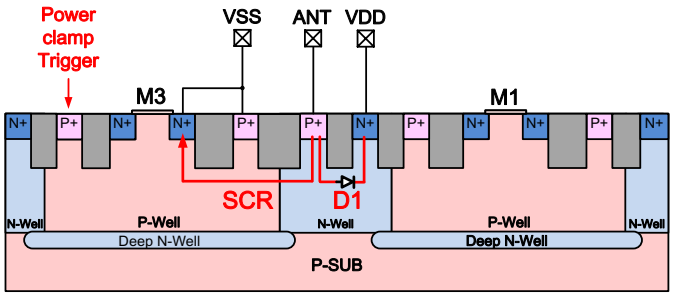


(b)

Fig. 6 Layout top view of (a) the conventional dual-diode ESD protection for T/R switch, and (b) the proposed ESD protection design for T/R switch with diode D1 and embedded SCRs (SCR1~SCR4).



(a)



(b)

Fig. 7 (a) Realization of the embedded SCR with the P+ anode of D1 and the N+ source of M3. (b) Cross-section view on X-X' line of Fig. 7(a) to show the current path of SCR and diode (D1).

IV. Experimental Results

A silicon chip including the T/R switch and LNA with the proposed ESD protection design (Fig. 5) has been fabricated in a 90-nm CMOS process. The chip microphotograph is shown in Fig. 8. The T/R switch with the conventional ESD protection design (Fig. 3) is also fabricated in the same chip. The ESD

characteristics is measured by the transmission line pulse (TLP) HED-T5000-HC with a 10-ns rise time and a 100-ns pulse width. Human-body-model ESD testing is stressed by HBM stimulator HCE-5000. The failure criterion of both TLP and HBM testing is by judging the DC-IV characteristics of the interested pins. In Table I, PS-mode ESD testing results are listed. ESD protection devices used for RFICs are often judged by both Ron and $C_{parasitic}$. The figure of merit (FOM) of the ESD protection design is calculated by the ratio of secondary breakdown current (It_2) and the total parasitic capacitance of the ESD devices. Those are also listed in Table I.

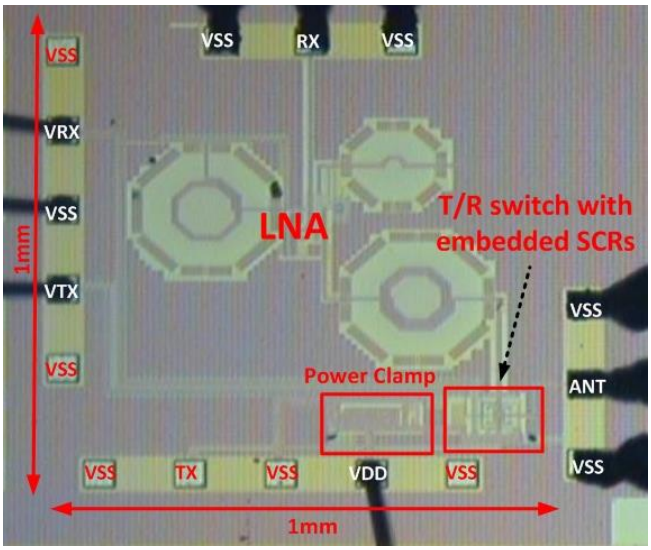


Fig. 8 Chip microphotograph of T/R switch, LNA, and the proposed ESD protection design.

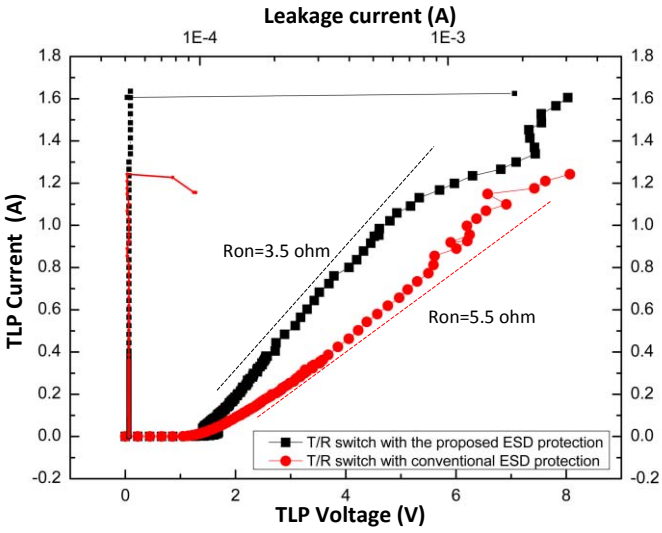
TABLE I
Comparison between the different ESD protection designs in PS-mode testing.

	Conventional ESD protection design	Proposed ESD protection design
It_2 (A)	1.24	1.63
HBM (kV)	2.3	2.4
Ron (Ω)	5.5	3.5
Normalized Capacitance (fF/um²)	2.92	0.59
Ron*$C_{parasitic}$ (Ω · fF)	899.36	630.14
FOM (mA/fF)	7.58	9.05

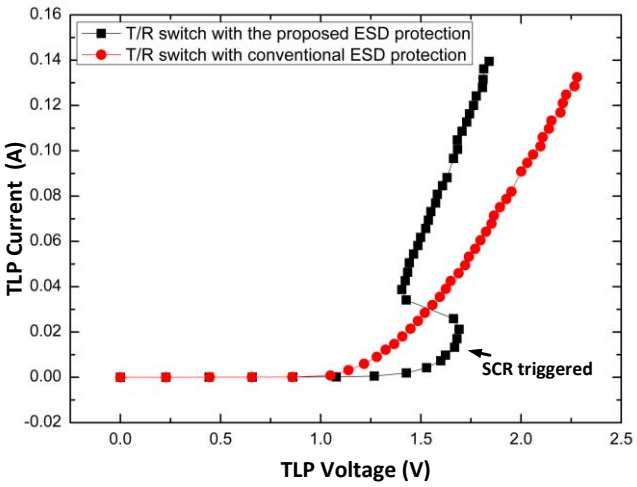
A. Transmission line pulse (TLP) test

TLP measurement has been commonly used to investigate the DUT under HBM ESD stress. The PS-mode TLP-measured characteristics on the ANT node protected by the conventional ESD protection circuit or the proposed ESD protection circuit are compared in Fig. 9(a), where the embedded SCRs further pulled down the turn-on resistance (Ron) from 5.5 ohm to 3.5 ohm. The secondary breakdown current (It_2) of the conventional ESD protection circuit and the proposed ESD protection circuit can achieve 1.24A and 1.63A, respectively. With a lower Ron, the clamping voltage at ANT node can be smaller under the same discharging current to perform better protection efficiency.

The snapback phenomenon of the embedded SCR can be observed in Fig. 9(b) with the enlarged TLP I-V curves. The unique snapback phenomenon demonstrated the parasitic bipolar junction transistor of the embedded SCR is triggered on by the power-rail ESD clamp circuit successfully. The triggered voltage (V_{t1}) in the proposed ESD protection circuit is only 1.7V, which is much lower than that of the common SCR device without triggering.



(a)



(b)

Fig. 9 (a) TLP-measured I-V characteristics in the T/R switch with different ESD protection designs. (b) Enlarged TLP I-V curves from Fig. 9(a) to show the snapback phenomenon on the embedded SCR.

B. Capacitance extraction by de-embedding method

The parasitic capacitance of the ESD protection device is a severe issue in high-speed I/O and RFICs. When it comes to measure the parasitic capacitance of the ESD protection device, the de-embedding method [15] is applied in order to excluding the parasitic effect of the PADs. By measuring the scattering parameters of the DUT with PADs, and the PADs under short,

open, load, and through (SOLT) calibrations, the accurate capacitance of the DUT can be calculated. In Fig. 10, the parasitic capacitance of the stand-alone single diode and embedded SCR (normalized to its layout area) are extracted at wide RF frequency bands. The parasitic capacitance per um^2 of the conventional diode and embedded SCR are 2.92 fF and 0.59 fF, respectively. The p-n-p-n structure of SCR intrinsically contributes less capacitance than the conventional p-n diode does. With smaller capacitance, the RF performance degraded by the ESD device can be minimized.

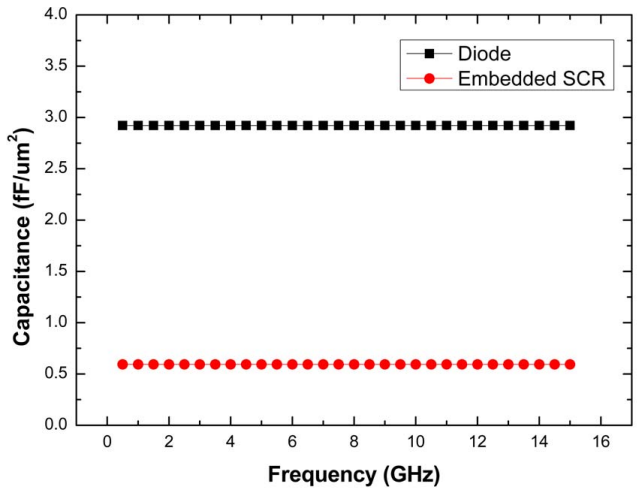


Fig. 10 Normalized parasitic capacitance of the stand-alone diode and embedded SCR device.

C. SEM photos of failure analysis

PS-mode ESD event is the most critical situation for T/R switch, since the reversed body-diode at the drain of NMOS cannot provide efficient discharging path for the PS-mode ESD zapping on ANT node.

Scanning electron microscope (SEM) photos of the conventional ESD protection circuit after PS-mode TLP testing on ANT node are shown in Fig. 11(a). The failure location is found at the transistors M1 and M2, as shown in Fig. 11(b) and Fig. 11(c). Transistors M1 and M2 are damaged, but ESD damage was not on the diodes D1 or D2. This indicates that the conventional ESD dual diodes are not sufficient enough to protect the T/R switch under the PS-mode ESD event.

Fig. 12(a) shows the SEM photos of the proposed ESD protection design after PS-mode TLP stress. The failure sites are located at the embedded SCRs, which is different from that with the conventional ESD protection design. Significant burned-out regions on SCR1 ~ SCR4 are shown in Fig. 12(b) ~ Fig. 12(e), respectively. The burned-out marks indicate the ESD current flow which is discharged from ANT node to VSS by all of the embedded SCRs. Those embedded SCRs are simultaneously triggered on by the driver in the power-rail ESD clamp circuit when ESD event is detected. The embedded SCRs are found to be the first elements damaged in the proposed ESD protection design under the PS-mode ESD stress. It means that the inner circuits can be really protected by the proposed ESD protection design with embedded SCRs.

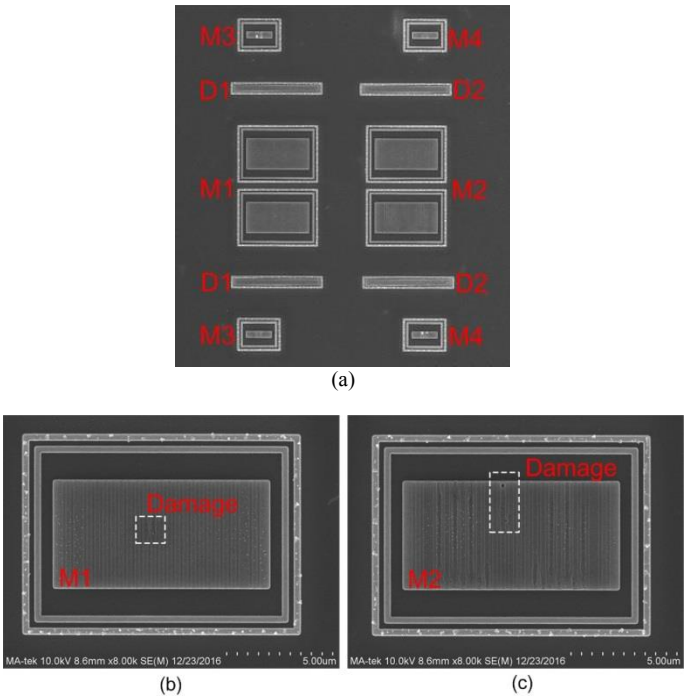


Fig. 11 (a) SEM photos of conventional ESD protection for T/R switch after 2.3kV HBM ESD test. Enlarged photos on (b) M1 and (c) M2 from Fig. 11(a).

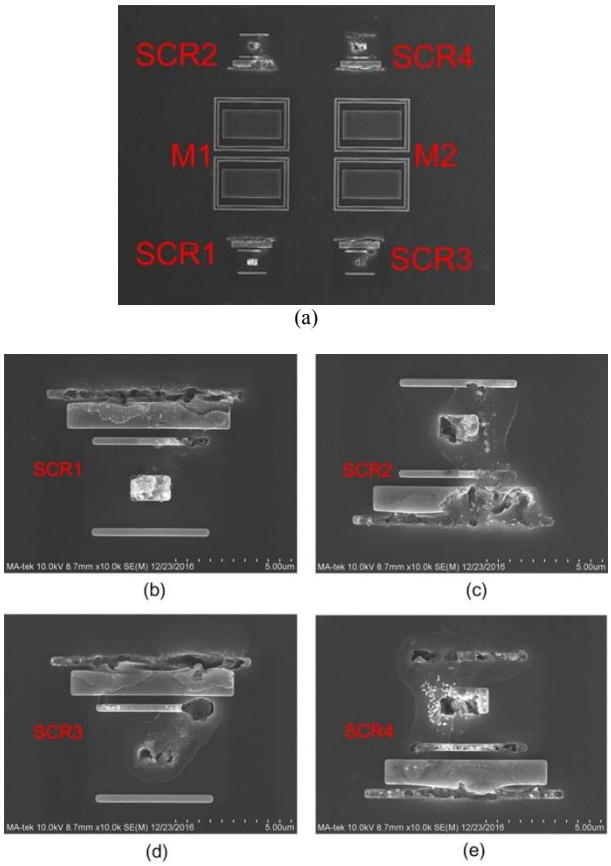


Fig. 12 (a) SEM photos of proposed ESD protection for T/R switch after TLP stress of 1.6A. Enlarged SEM photos from Fig. 12(a) to see the damage on (b) SCR 1, (c) SCR 2, (d) SCR 3, and (e) SCR 4.

V. Conclusion

A T/R switch with embedded SCR for ESD protection is fabricated and verified in 90-nm CMOS process. The proposed design strengthens the ESD immunity of T/R switch circuit especially in the PS-mode ESD stress. The TLP characteristics and parasitic capacitance extraction of the conventional ESD protection and the proposed design are measured and discussed. With lower Ron and parasitic capacitance, the proposed design can be a good ESD solution for T/R switch and other RF applications.

Acknowledgment

This work was supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 105-2221-E-009-166, and MOST 106-2622-8-009-007-TE1. The authors would like to thank Rui-Hong Liu in Realtek for his technical suggestion, and National Chip Implementation Center (CIC), Taiwan, for the support of chip fabrication.

References

[1] H.-S. Chen, H.-Y. Tsai, L.-X. Chuo, Y.-K. Tsai, and L.-H. Lu, "A 5.2-GHz fully integrated RF front-end by T/R switch, LNA, and PA co-design with 3.2-dB NF and +25.9-dBm output power," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2015, pp 1–4.

[2] S. Goswami, H. Kim, and J. Dawson, "A frequency-agile RF frontend architecture for multi-band TDD applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2127–2140, Oct. 2014.

[3] A. A. Kidwai, C.-T. Fu, J. C. Jensen, and S. S. Taylor, "A fully integrated ultra-low insertion loss T/R switch for 802.11b/g/n application in 90nm CMOS process," *IEEE J. Solid-State Circuits,* vol. 44, no. 5, pp. 1352–1360, May 2009.

[4] Q. Li and Y. P. Zhang, "CMOS T/R switch design: towards ultra-wideband and higher frequency," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 563–570, Mar. 2007.

[5] M.-D. Ker and C.-Y. Lin, and Y.-W. Hsiao "Overview on ESD protection designs of low-parasitic capacitance for RF ICs in CMOS technologies," *IEEE Trans. Device and Materials Reliability*, vol. 11, no. 2, pp. 207–218, Jun. 2011.

[6] C.-Y. Lin, L.-W. Chu, and M.-D. Ker, "ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process," *IEEE Trans. Microw. Theory Tech.,* vol. 60, no. 3, pp. 714–723, Mar. 2012.

[7] S.-Y. Tsai, C.-Y. Lin, L.-W. Chu, and M.-D. Ker, "Design of ESD protection for RF CMOS power amplifier with inductor in matching network," in *Proc. IEEE Asia Pacific Conf. on Circuits and Systems,* 2012, pp.467–470.

[8] C. Fu, H. Lakdawala, S. Taylor, and K. Soumyanath, "A 2.5GHz 32nm 0.35mm2 3.5dB NF -5dBm P1dB fully differential CMOS push-pull LNA with integrated 34dBm T/R switch and ESD protection," in *ISSCC Dig. Tech. Papers*, 2011, pp. 56–57.

[9] C.-Y. Lin, R.-H. Liu, and M.-D. Ker, "ESD self-protection design on 2.4GHz T/R switch for RF application in CMOS process," in *Proc. IEEE Int. Reliability Physics Symp.,* 2016, pp. EL-1-1–EL-1-4.

[10] X. Shawn *et al.,* "Concurrent design analysis of high-linearity SP10T switch with 8.5kV ESD protection," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1927–1941, Sep. 2014.

[11] F.-J. Huang and O. Kenneth, "A 0.5-μm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 486–492, Mar. 2001.

[12] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K. Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 31–39, Jan. 2006.

[13] A. Poh and Y. P. Zhang, "Design and analysis of transmit/receive switch in triple-well CMOS for MIMO wireless systems," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 458– 466, Mar. 2007.

[14] M. Ahn, H.-W. Kim, C.-H. Lee, and J. Laskar, "A 1.8-GHz 33-dBm *P* 0.1-dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated well structure," *IEEE Trans. Microw. Theory Tech.,* vol. 57, no. 11, pp. 2661–2670, Nov. 2009.

[15] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices,* vol. 47, no. 4, pp. 734–740, Apr. 2000.