ESD-Induced Latchup-Like Failure in a Touch Panel Control IC

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***Abstract*— With on-chip ESD protection design, the I/O pins of a touch panel control IC can pass the chip-level ESD tests of HBM 4kV and MM 400V. However, such a touch panel control IC mounted onto a display panel suffered the latchup-like failure after the system-level ESD zapping in the air-discharge mode. Some high-voltage power pin began to generate a large leakage current after the system-level ESD test, which demonstrated a symptom of latchup failure. By failure analyses with TLP-measurement, EMMI, and SEM, the root cause has been found on the power-rail ESD clamp circuit of the high-voltage power pin. The holding voltage of the power-rail ESD clamp circuit in the high-voltage power pin, that was lower than its normal operating voltage, caused such a latchup-like failure. Some modified solutions to rescue this latchup-like failure in the touch panel control IC are presented.**

I. Introduction

Among various touch panel sensing technologies, the most common method is the mutual-capacitance sensing, because it allows unambiguous touching with higher resolution [1]. The schematic of touch panel with mutual-capacitance sensing is shown in Fig. 1. The transmitter (TX) provides driving signals to TX electrode, and the driving signals also inject the relative signals into the receiver (RX) electrode through the mutual-capacitance array, then the controller system processes the signals sensed from RX interface to recognize the touched positions. But, the capacitance change due to finger touched would be smaller than the parasitic capacitance, it results in the touch sensing system to have a low signal-to-noise ratio (SNR) and to be sensitive to noise couple. To solve this issue, the TX signal voltage level was enlarged, and the amplitude of RX signal was increased in turn to raise the signal processing margin. Therefore, the TX interface should be implemented with high-voltage CMOS processes to provide higher voltage driving signals, and this method has been widely adapted in the touch panel control ICs.

In the end-user applications, the electrostatic discharge (ESD) induced damage had become one of the major reliability issues to the consumer electronics which are mainly controlled or operated by the integrated circuits (IC's). Therefore, on-chip ESD protection designs are essentially requested to be built into the IC products [2]-[5]. As a result, the ESD protection circuits were implemented for all input/output (I/O) and power (V_{DD}/V_{SS}) pins in this touch panel control IC against ESD damage. For evaluating the robustness of ICs against ESD events, two chip-level ESD tests are often used, human-body-model (HBM) test [6] and machine-model (MM) test [7]. Besides, a different type of system-level ESD test is established for the end products to confirm the robustness of electronic systems [8].

In this work, a touch panel control IC mounted onto a display panel suffered the latchup-like failure after the system-level ESD zapping in the air-discharge mode. By failure analyses, the root cause has been found on the power-rail ESD clamp circuit of the high-voltage power pin. The holding voltage of the power-rail ESD clamp circuit in the high-voltage power pin was lower than its normal operating voltage to cause such a latchup-like failure. Some modified solutions to rescue this latchup-like failure in the touch panel control IC are presented.

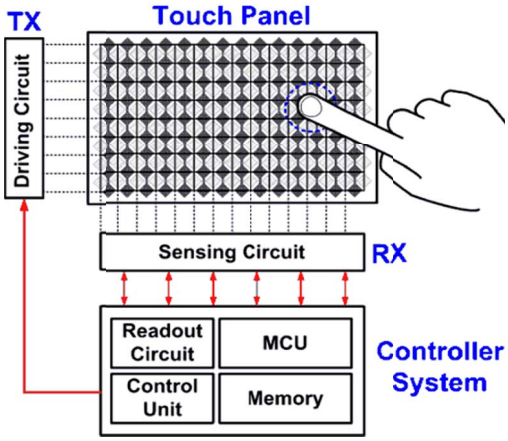

Fig. 1. Schematic of touch panel with mutual-capacitance sensing.

II. ESD Protection Design in the Touch Panel Control IC

To comprehensively protect IC against ESD stresses, efficient current paths to discharge ESD energy at all I/O pins are necessary. Due to electrostatic charges would be either positive or negative, there are four ESD-stress modes at each I/O pin with respect to the grounded V_{DD} or V_{SS} (GND) pins under chip-level ESD testing [6], which are PS (positive-to-V_{SS}), PD (positive-to-V_{DD}), NS (negative-to-V_{SS}), and ND (negative-to-V_{DD}) modes. The typical on-chip ESD protection scheme is often designed with the power-rail ESD clamp circuit. Because the power-rail ESD clamp circuit is especially designed with a large ESD protection device (M_{NESD}), it is effective to discharge ESD energy between the V_{DD} and V_{SS} power lines [9]. Moreover, with the turn-on efficient power-rail ESD clamp circuit, the ESD clamp devices at the I/O pads can be realized with smaller device dimensions but still to achieve good enough ESD robustness [10], [11].

A. ESD Protection Design for RX and TX Pins

In the touch panel control IC, the most part of I/O pins are RX and TX. Figs. 2(a) and 2(b) show the schematics of ESD protection design for RX and TX pins in the touch panel control IC. The ESD clamp devices for RX pin are realized by pure diodes D_{P1} and D_{N1}, as well as the power-rail ESD clamp circuit is consist of a RC-based ESD-detection circuit (R_1, M_{NC1}, M_{P2} and M_{N2}) and a large n-type MOSFET (M_{NESD1}) as the ESD protection device. In the TX pin, the ESD protection structure is similar to RX pin. But, in order to sustain in a high operating voltage of 12 V, the diodes (D_{HP1} and D_{HN1}) are realized by high-voltage diodes and the power-rail ESD clamp circuit is composed of high-voltage MOSFETs (M_{HNC1}, M_{HP2}, M_{HN2}, and M_{HNESD1}). In the touch panel control IC, the 12-V high-voltage power supply for TX interfaces is provided by on-chip charge pump circuit. To protect the pin of high-voltage power output (V_{HV}) against ESD stresses, the same high-voltage power-rail ESD clamp circuit is also added to the V_{HV} pin, as that shown in Fig. 3.

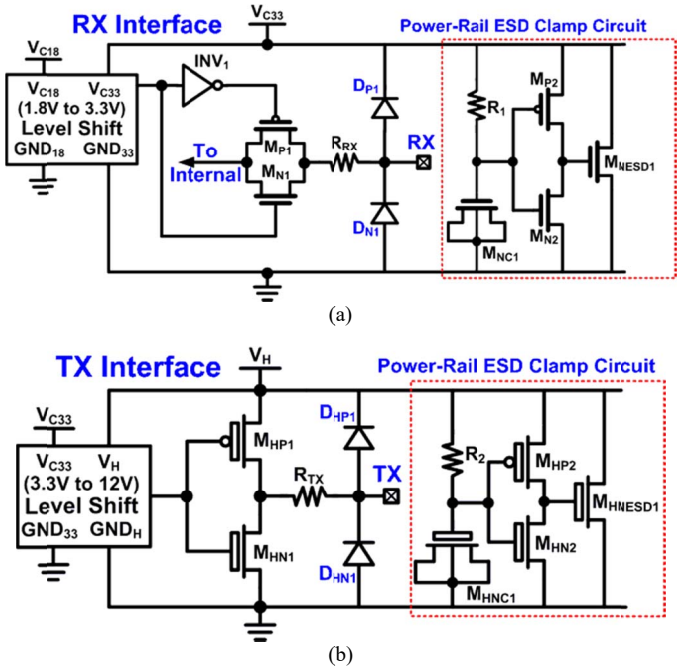

Fig. 2. Schematics of ESD protection design for (a) RX and (b) TX pins.

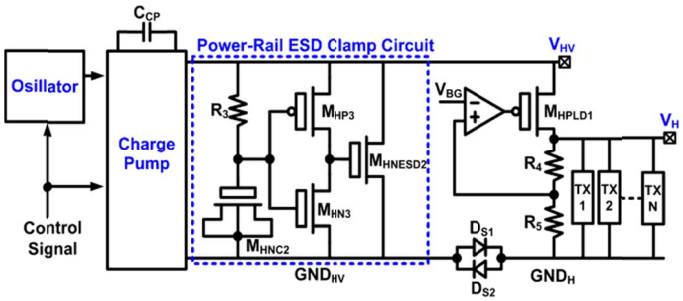

Fig. 3. Power-rail ESD clamp circuit for the pin of high-voltage power output (V_{HV}).

B. ESD Robustness

For the commercial IC products, the typical chip-level ESD robustness is required 2 kV in HBM test and 200 V in MM test. The touch panel control IC had been fabricated in a 1.8-V/3.3-V/12-V CMOS process with 12-V DDDMOS device. All device dimensions used in ESD protection circuits are listed in Table I. Table II shows the measured chip-level ESD robustness of the touch panel control IC. From the measured results, all of RX pins, TX pins, low-voltage (1.8-V/3.3-V) power pins, and high-voltage (12-V) power pins can achieve at least 4 kV in HBM test and 400 V in MM test. With such robust ESD levels, the IC products can have good production yield during the product assembly.

Table I
Device dimensions of ESD protection circuits used in RX/TX pins

ESD Protection Design	ESD Clamp Device		Power-Rail ESD Clamp Circuit				
RX	D_{P1}	D_{N1}	R_1	M_{NC1}	M_{P2}	M_{N2}	M_{NESD1}
	W=18.5 μm L=66 μm	W=18.5 μm L=57 μm	100 kΩ	W=20 μm L=5 μm	W=42 μm L=0.4 μm	W=16 μm L=0.4 μm	W=864 μm L=0.44 μm
TX	D_{HP1}	D_{HP1}	R_2	M_{HNC1}	M_{HP2}	M_{HN2}	M_{HNESD1}
	W=20 μm L=74 μm	W=18.4 μm L=57 μm	100 kΩ	W=70 μm L=21.5 μm	W=200 μm L=1.67 μm	W=40 μm L=1.67 μm	W=840 μm L=1.67 μm

Table II
Measured HBM/MM ESD robustness of the RX/TX pins in the Touch Panel Control IC

ESD Test Model	PS-mode		PD-mode		NS-mode		ND-mode		V_{DD}-to-V_{SS}	
	RX	TX	RX	TX	RX	TX	RX	TX	Low-Voltage Power Pins	High-Voltage Power Pins
HBM (kV)	5	4	5	4	5	4	5	4	8	6
MM (V)	500	400	500	400	500	400	500	400	800	500

Quite different to the chip-level ESD test on IC products, the system-level ESD test is established for electronic systems [8], including the demo equipments or complete end products. In IEC 61000-4-2, two test modes have been specified, which are air-discharge test mode and contact-discharge test mode. Without the direct conducting surfaces in the demo equipment, the air-discharge mode was adapted for the touch panel control IC when the equipment was powered on. After the touch panel control ICs assembled into the demo equipment, each function was correctly presented in the display system. However, when the ESD gun applied a zapping voltage of ±15 kV at the panel edge (near the touch panel control IC) in the air-discharge mode, the display panel system started to have some malfunctions, which occurred in the touch panel control IC. The high-voltage power pin began to conduct a large leakage current. Moreover, the high-voltage output (V_{HV}) which provided by the charge pump circuit could not reach the correct voltage level of 12V.

III. Failure Analysis in Touch Panel Control IC

As comparing the chip layout pattern with the hot-spot image of the emission microscopy (EMMI) photograph, the leakage location was found in the high-voltage circuit blocks. To further observe the certain failure point, the scanning electron

microscope (SEM) experiment was used. The SEM photograph on the touch panel control IC after the system-level ESD test with the air-discharge mode of ±15 kV is shown in Fig. 4. In the SEM photograph, the failure point was found in the high-voltage power-rail ESD clamp circuit. Comparing to the layout top view of the power-rail ESD clamp circuit shown in Fig. 5, the failure point was only focused on the drain sides of the M_{HNESD2} with multiple-finger layout style.

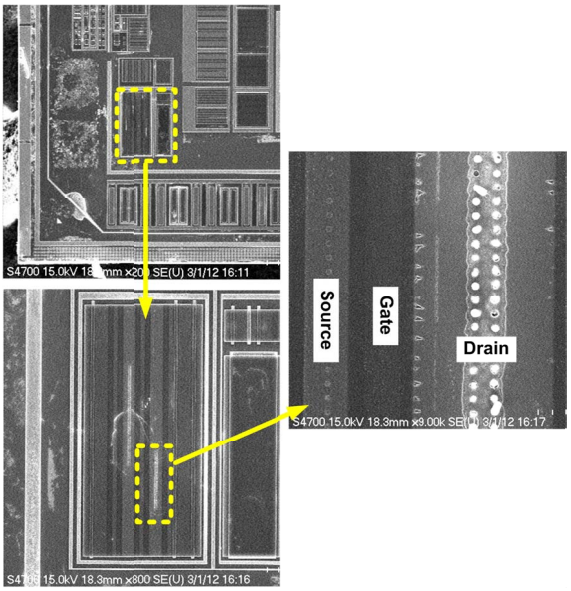

Fig. 4. SEM photograph of the high-voltage power-rail ESD clamp circuit after the system-level ESD test with the air-discharge mode of ±15 kV.

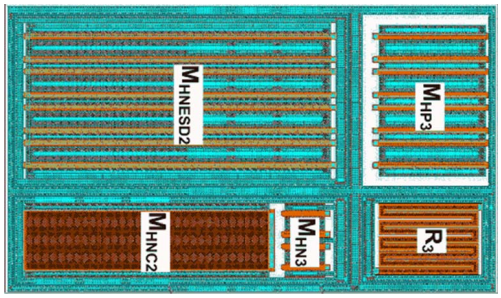

Fig. 5. Layout top view of the high-voltage power-rail ESD clamp circuit.

For analyzing the characteristics and turned-on behavior of ESD protection device under ESD stress, the transmission line pulse (TLP) system with 100-ns pulse width and 10-ns rise time has been widely used to observe the parameters, such as trigger voltage (V_{t1}), holding voltage (V_h), and secondary breakdown current (I_{t2}) [12]. Moreover, the HBM ESD level can be roughly estimated by the TLP-measured I_{t2} value [13], [14].

The TLP-measured I-V curve of the low-voltage power pin from V_{C33} to GND_{33} is shown in Fig. 6. With several power pads arranged in RX interfaces, the TLP I_{t2} is as high as ~6 A. In addition, the TLP-measured I-V curve of the high-voltage power pin from V_{HV} to GND_{HV} is shown in Fig. 7. As the TLP voltage exceeded the trigger voltage V_{t1} of ~15 V, the snapback is occurred when the parasitic bipolar junction transistor (BJT) was triggered on. The snapback voltage is dropped and kept at a voltage level of only ~8.8 V, as the holding voltage V_h indicated in Fig. 7. Although the I_{t2} can achieve ~4 A, the V_h of 8.8 V is lower than the normal operating voltage of 12 V. With a holding voltage smaller than the operating voltage, it has been reported that the system will suffer the latchup-like issue in CMOS ICs [15]-[20]. This phenomenon often leads to IC function failure or even destruction by burning out. Due to the failure point was only focused on the drain sides of M_{HNESD2}, the parasitic NPN BJT Q_1 inherent in the high-voltage n-type MOSFET M_{HNESD2}, as shown in Fig. 8, was turned on after the system-level ESD test, and finally burning out the M_{HNESD2} device.

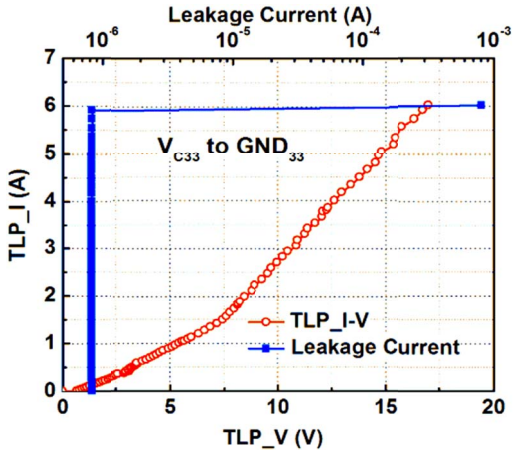

Fig. 6. TLP-measured I-V curve of the low-voltage power pin from V_{C33} to GND_{33}.

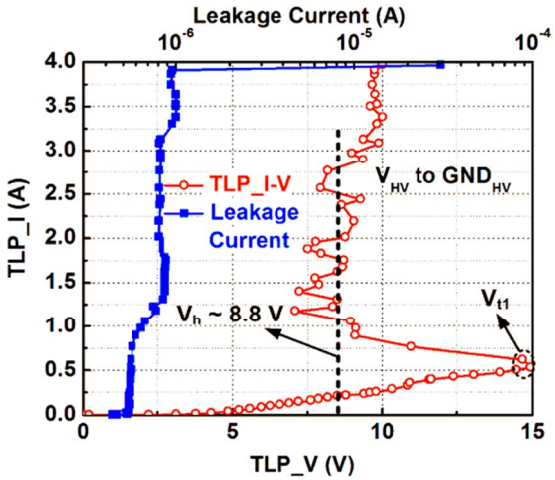

Fig. 7. TLP-measured I-V curve of the high-voltage power pin from V_{HV} to GND_{HV}.

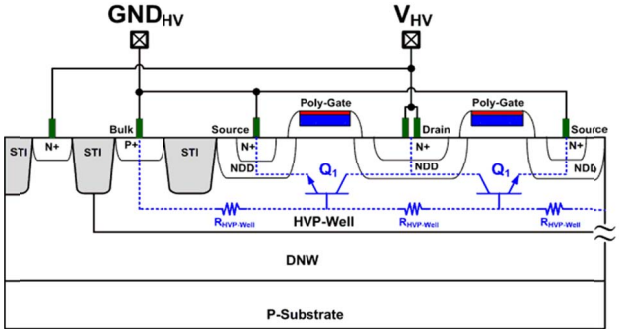

Fig. 8. Device cross-sectional view of M_{HNESD2} with the parasitic NPN BJT Q_1.

IV. Modification on High-Voltage Power-Rail ESD Clamp Circuit

To effectively provide ESD protection capability, Fig. 9 shows the ESD protection design window with the required conditions. In the region III, the V_{t1} should be smaller than the gate-oxide breakdown voltage (V_{BD}) to ensure successful protection without damage at internal circuits. In the region I, the V_h should be higher than the operating voltage (V_{DD}) to accomplish a latchup-free design. Thus, an efficient ESD protection device's I-V curve must be located within the region II of Fig.9. In this failure case, the high-voltage power-rail ESD clamp circuit suffered the latchup-like issue. As the latchup phenomenon occurred in normal circuit operating conditions, the circuit could not be recovered to normal functionality. Therefore, the modified design on the high-voltage power-rail ESD clamp circuit to meet latchup immunity is needed in the touch panel control IC.

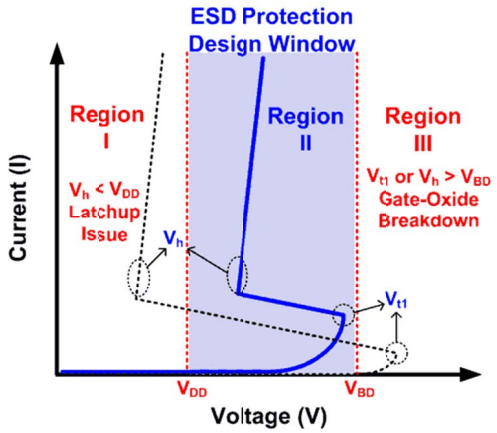

Fig. 9. I-V characteristics of the ESD protection design window.

A circuitry modification was attempted to remedy the latchup-like issue. Because the latchup-like phenomenon was caused by the turned-on parasitic NPN BJT, the simple way is changing the metal connections to isolate the NPN BJT path within the M_{HNESD2}. By using the focused-ion-beam (FIB) to cut the source-side metal connection, the main ESD discharging path is only formed with a reverse diode (D_1) from V_{HV} to GND_{HV}, as shown in Fig. 10. The TLP-measured I-V curve of the modified solution in the high-voltage power-rail ESD clamp circuit after the FIB cutting is shown in Fig. 11. Without the parasitic NPN BJT connecting from V_{HV} to GND_{HV}, the snapback condition is disappeared in the measured I-V curve. In addition, the clamping voltage is always larger than the operating voltage of 12 V after the D_1 broke down. Thus, it did not suffer the latchup-like issue. However, using the reverse diode to realize the ESD protection could not obtain good ESD protection. The I_{t2} is only 1.06 A in the TLP measurement. Without an effective ESD current discharging path, the ESD robustness did not meet the basic specifications of 2 kV in HBM test and 200 V in MM test. Therefore, a re-design on the high-voltage power-rail ESD clamp circuit to have both of latchup-free immunity and good enough ESD robustness is strongly needed.

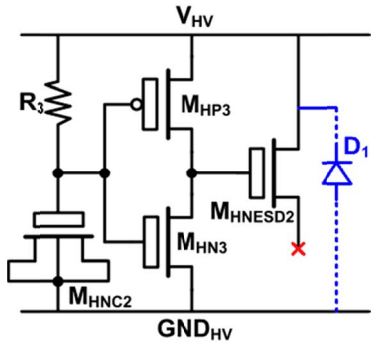

Fig. 10. Modified solution in high-voltage power-rail ESD clamp circuit.

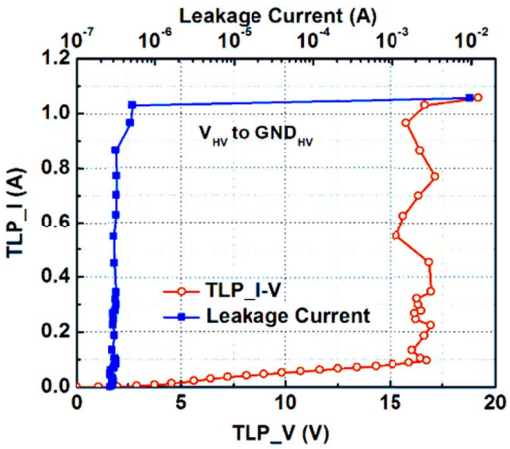

Fig. 11. TLP measured I-V curve of the modified high-voltage power-rail ESD clamp circuit.

V. Discussion

In a single ESD protection n-type MOSFET, the holding voltage of the turned-on parasitic NPN BJT can be estimated by

$$V_{H1} = V_{P1} + V_{CEQ1}. \quad (1)$$

The V_{P1} is the voltage generated by the turned-on current (I_{ON}) through the parasitic resistance within the junction and metal connections. The V_{CEQ1} is the voltage potential inherent in the turned-on BJT from collector to emitter, as shown in Fig. 12(a). To increase the holding voltage of the high-voltage power-rail ESD clamp circuit, the ESD protection n-type MOSFET could be modified to have a stacked structure. As shown in Fig. 12(b), two parasitic NPN BJTs are stacked to increase the total holding voltage. Ideally, the holding voltage of stacked structure will be twice of a single structure. The holding voltage of the stacked structure can be given by

$$V_{H2} = V_{P1} + V_{CEQ1} + V_{P2} + V_{CEQ2}. \quad (2)$$

In some prior studies, the high-voltage-tolerant ability of power-rail ESD clamp circuit can be achieved by using the stacked structure to overcome gate-oxide overstress issue [21], [22]. However, the increased holding voltage by using the stacked structure would degrade its ESD robustness, due to the higher power generated from ESD stress ($V_h \times I_{ESD}$). Therefore, to increase the holding voltage by the stacked structure, the dimension of each ESD device in the stacked structure should

be enlarged to avoid the degradation of ESD robustness, especially in high-voltage CMOS processes. To solve the aforementioned problems, some prior works also reported alternative solutions to achieve latchup-free immunity without causing degradation on ESD robustness [15], [17]-[19].

For the touch panel control IC, the design with two high-voltage n-type MOSFETs in stacked configuration would degrade its ESD protection ability due to the higher overshooting voltage during ESD stresses. With a high-voltage n-type MOSFET stacked with a low-voltage n-type MOSFET together, a successful design modification that had the holding voltage higher than 12 V and also performed a good enough ESD robustness was reported in [23] to achieve the purpose of free to latchup-like issue in the touch panel application.

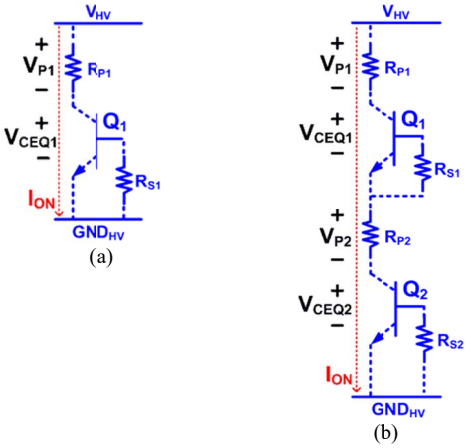

Fig. 12. Estimation of holding voltage with (a) single n-type MOSFET and (b) two stacked n-type MOSFETs.

VI. Conclusion

The holding voltage of the power-rail ESD clamp circuit realized with the high-voltage device has been investigated by TLP measurement. In this case, with the holding voltage lower than the normal circuit operating voltage, it caused the touch panel control IC suffering the latchup-like failure after the system-level ESD gun test. A re-design on the high-voltage power-rail ESD clamp circuit to have both of latchup-free immunity and good enough ESD robustness was analyzed and discussed. Successful solution with high-voltage and low-voltage MOSFETs stacked in the high-voltage power-rail ESD clamp circuit is recommended for this touch panel application.

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