Low-Trigger ESD Protection Design with Latch-Up Immunity for 5-V CMOS Application by Drain Engineering

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***Abstract*- According to previous work about PESD optimization [1], there are some potential risks such as low breakdown voltage (V_{BD}) and low holding voltage (V_h) can be improved for power-rail ESD application. Through drain region design with P-type concentration engineering, the enclosed P-Well in Deep N-Well (EW) in drain region was proposed with high ESD performance (HBM>8kV) and good turn-on efficiency (V_{t1}=8.1V) without suffering from low V_{BD} and latch-up issues.**

I. Introduction

For high voltage input-output (IO) interface ESD application, Laterally-Diffused MOSFET (LDMOS) is widely utilized and embedded in low voltage logic CMOS technology. A traditional N-type LDMOS (N-LDMOS) cross-sectional schematic is shown in Fig. 1 (a). In previous work [1], drain-back (DB) structure [2]-[4] and PESD implant [5], [6] layer are utilized for better ESD performance, as shown in Fig. 1 (b). However, for 5V power-rail ESD application, the low holding voltage of 4.5V will suffer latch-up under overshooting voltage/current on power line. Besides, low breakdown voltage (V_{BD}) of 6.0V indicates the potential reliability risk under 5V operation, as shown in Fig. 2 and table. 1. In this work, a new drain engineering ESD N-LDMOS is proposed without latch-up and reliability danger for 5V whole chip ESD design in 110nm CMOS logic process.

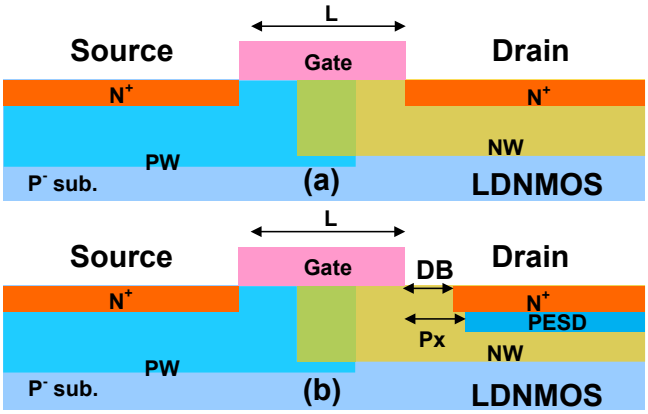

Figure 1. T he cross-sectional view of (a) Traditional N-LDMOS and (b) N-LDMOS with the DB and PESD.

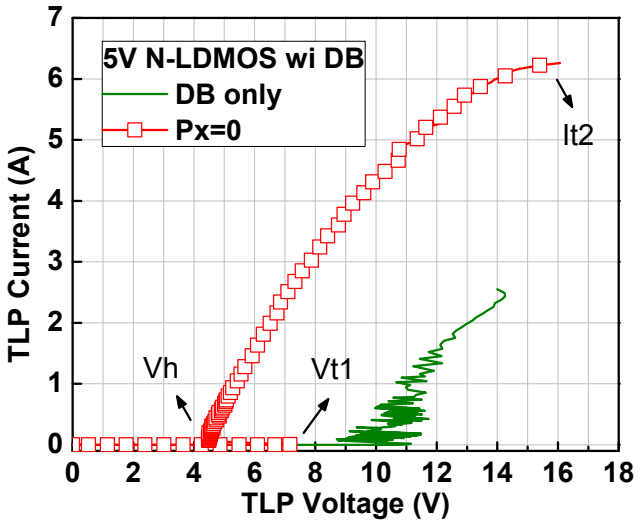

Figure 2. The TLP-measured IV curves of N-LDMOS with DB and with DB+PESD (P_x=0).

TABLE I. THE ESD CHARACTERISTICS OF N-LDMOS WITH (A) DB AND (B) DB+PESD. (HBM 8KV IS TESTER LIMIT.)

Scenario	LDNMOS ESD characteristics (W=600um)				
	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM (kV)	V_{BD} (V)
Traditional	10.9	8.0	*0.3*	*1.4*	10.1
DB only	11.2	8.8	2.6	4.0	10.1
P_x=0	7.2	4.5	6.3	>8.0	*6.0*

II. Device Evolution

For better ESD robustness, P-type doped region (PESD layer in last work [1]) is inserted in drain side to create a parasitic SCR [7]-[9] in N-LDMOS. Meanwhile, the P-type region provides a punch through path toward PW nearby source side, which improves the turn-on efficiency. Consequently, high ESD level and better turn on efficiency ESD N-LDMOS was obtained [1].

The cross-sectional view of new proposed ESD design is shown in Fig. 3. A lighter doping of P-Well (PW) was substituted for PESD to mitigate the low V_{BD} effect without extra mask cost. Besides, a deep N-well (DNW) was adopted to enclose the drain region of N-LDMOS and to create parasitic SCR path, as shown in Fig. 3(a). The new design was named as enclosed PW (EW) in this work. Prior work and N-LDMOS with P^+ doped region at edge of drain close to gate, which are compatible with standard process for cost concern, are also studied for comparison, as shown in Fig. 3(b) and (c). Notice that DB structure wasn't adopted in this work.

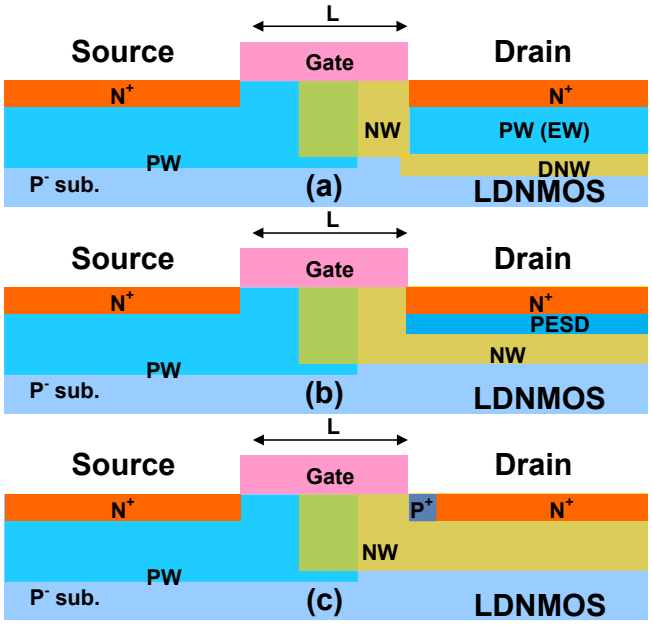

Figure 3. The cross-sectional view of N-LDMOS with (a) New design enclosed PW in DNW (EW) (b) PESD and (c) P^+ doped region at edge of gate in drain.

III. Results and Discussion

The ESD results of proposed EW design and other scenarios are shown in Fig. 4 and Table 2. Noted that the more concentration of the drain p-type region is (P^+>PESD>EW), the lower V_h and V_{t1} are obtained, as shown in Fig.4. There are two mechanisms in the correlation of drain P-type concentration and V_h. First, ESD path is stacked by a reverse diode and a SCR in series (N^+/PNPN). Higher V_h was observed in EW since the drain P-type concentration of PW is less than that of PESD and P^+, so the V_{BD} of the reverse junction N^+/P in EW is higher than that of N^+/PESD and N^+/P^+.

Second, V_h characteristic after SCR turns on is correlated to the product of β gain of parasitic BJT PNP and NPN. In proposed structure, the drain P-type doped region indicates the emitter of PNP. While doping concentration of emitter becomes heavier, the β gain of PNP in SCR is enhanced and then V_h becomes lower. Therefore the correlation of V_h is EW>PESD>P^+.

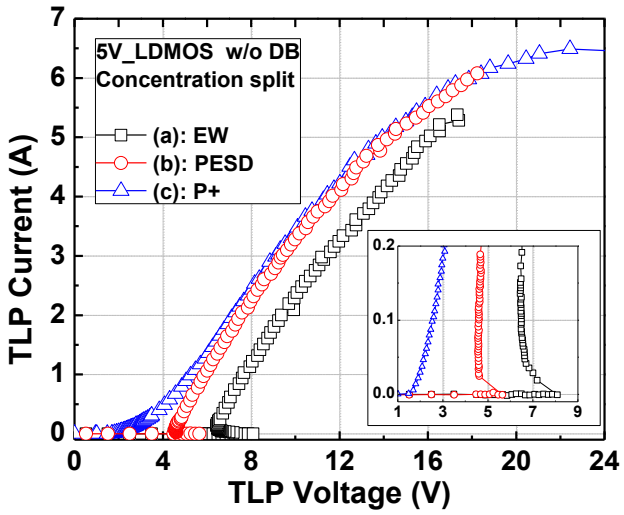

Figure 4. The TLP-measured IV curves of N-LDMOS with (a) EW, (b) PESD and (c) P^+.

TABLE II. The ESD characteristics of N-LDMOS with (a) EW, (b) PESD and (c) P^+. (HBM 8kV is tester limit.)

Scenario (w/o DB)	LDNMOS ESD characteristics (W=600um)				
	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM (kV)	V_{BD} (V)
EW	8.1	6.4	5.3	>8.0	8.9
PESD	5.7	*4.6*	6.0	>8.0	*5.0*
P^+	-	-	6.5	-	*<0.5*

The mechanism of V_{t1} trend is also correlated to the concentration of drain P-type doped region. The more concentration is, the lower V_{t1} is observed because of the worse punch through behavior toward source side PW region. Therefore V_{t1} of EW is higher than that of PESD and P^+ suffers minor punch through without snapback behavior. The mechanism of V_{BD} trend is identical as shown in Table 2.

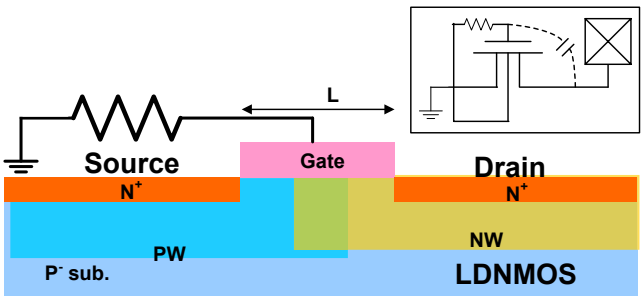

Figure 5. T he cross-sectional view and circuit sketch of traditional N-LDMOS with gate-coupled by resistor (GR) design.

On the other hand, a traditional low-trigger N-LDMOS with gate-coupled by resistor (GR) design [10]-[11] is also compared in the same process, as shown in Fig. 5. The results are presented

in Fig. 6 and Table 3. Higher ESD robustness is observed in EW design because the additional parasitic SCR sinks more ESD current than parasitic BJT of GR N-LDMOS. The new proposed EW design is verified with high ESD performance and efficient turn-on speed in addition to latch-up free V_h behavior without low V_{BD} risk and extra cost.

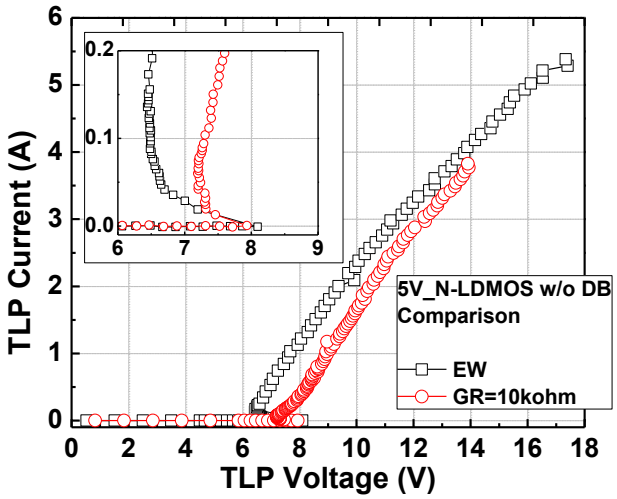

Figure 6. The TLP-measured IV curves of N-LDMOS with EW and GR.

TABLE III. THE ESD CHARACTERISTICS OF N-LDMOS WITH EW AND GR. (HBM 8KV IS TESTER LIMIT.)

Scenario (w/o DB)	LDNMOS ESD characteristics (W=600um)				
	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM (kV)	V_{BD} (V)
EW	8.1	6.4	5.3	>8.0	8.9
GR=10kΩ	7.9	7.2	3.8	5.2	10.1

IV. CONCLUSION

New proposed drain engineering design of 5V N-LDMOS is successfully verified in 110nm 5V CMOS process. With enclosed PW in DNW (EW), the ESD performance is robust (HBM>8kV) with efficient turn-on speed (V_{t1}=10.9→8.1V). Breakdown voltage can be also improved (V_{BD}=6V→8.9V) and holding voltage is adjusted for better latch-up immunity (V_h= 4.5V→6.4V) in power-rail ESD application compared with previous IO ESD design [1]. The new drain engineering EW design is an excellent solution for 5V power-rail ESD application in CMOS technology without extra cost.

ACKNOWLEDGMENT

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REFERENCES

[1] Chun Chiang, Ping-Chen Chang, Pei-Shan Tseng, Po-Ya Lai, Tien-Hao Tang, and Kuan-Cheng Su, "Optimization of PESD Implant Design for ESD Robustness of 5V Drain-Back N-LDMOSFET," *IEEE IRPS 2016*, EL-3-1 - EL-3-4.

[2] D. -G. Lin, S. L. Tu, Y.-C. See, and P. Tam, "A novel LDMOS structure with a step gate oxide," in *Proceedings of International Electron Devices Meeting*, 1995, pp. 963–966.

[3] R. S. Wrathall, B. J. Baliga, K. Shenai, W. Hennesey, and T. P. Chow, "Charge controlled 80 volt lateral DMOSFET with very low specific on-resistance designed for an integrated power process," in *International Technical Digest on Electron Devices*, 1990, pp. 954–957.

[4] L. B. Technology, P. G. Y. Tsui, P. V Gilbert, and S. W. Sun, "Integration of power LDMOS into a low-voltage 0.5 mu m BiCMOS technology," in *International Technical Digest on Electron Devices Meeting*, 1992, no. 512, pp. 27–30.

[5] D. Alvarez et al., "Analysis of ESD failure mechanism in 65nm bulk CMOS ESD NMOSFETs with ESD implant," in *Microelectronics Reliability*, vol. 46, Issues 9–11, 2006, pp. 1597–1602.

[6] K. Chatty, D. Alvarez, R. Gauthier, C. Russ, M. Abou-Khalil and B. J. Kwon, "Process and design optimization of a protection scheme based on NMOSFETs with ESD implant in 65nm and 45nm CMOS technologies," in *29th Electrical Overstress/Electrostatic Discharge Symposium, 2007,* pp. 7A.2-1–7A.2-10.

[7] Mayank Shrivastava, Harald Gossner, and Christian Russ, "A drain-extended MOS device with spreading filament under ESD stress," in *IEEE Electron Device Letters*, vol. 33, no. 9, Sep. 2012, pp. 1294–1296.

[8] P. Zhang, Y. Wang, S. Jia, X. Zhang, "Analysis of LDMOS-SCR ESD Protection Device for 60V SOI BCD Technology," in *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, 2010, pp. 1–4.

[9] Y. Wang, G. Lu, L. Zhang, J. Cao, S. Jia, and X. Zhang, "Comprehensive study and corresponding improvements on the ESD robustness of different nLDMOS devices," in *Proceedings of the 21th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2014, vol. 2, no. c, pp. 304–307.

[10] Sridhar Ramaswamy, Charvaka Duvvury and Sung-Mo Kang, "EOS/ ESD Reliability of Deep Sub-Micron NMOS Protection Devices,", *IEEE IRPS 1995*, pp.284–291.

[11] Charvaka Duvvury, Carlos Diaz, and Tim Haddock, "Achieving Uniform nMOS Device Power Distribution for Submicron ESD Reliability,", *IEEE IEDM 1992*, pp.131–134.