New On-Chip Transient Detection Circuit to Improve Electromagnetic Susceptibility of Microelectronic Systems

Xiao-Rui Kang and Ming-Dou Ker
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan

Abstract

A new on-chip transient detection circuit for system-level electrostatic discharge (ESD) protection is presented in this work. The circuit simulation and experimental results with silicon testchip in a 0.18-μm CMOS process have confirmed that the new proposed circuit can successfully detect the occurrence of system-level ESD-induced electrical transient disturbance. The detection output can be used as system recovery index to restore the system from frozen or upset state to a stable and known state. Therefore, the immunity of microelectronic products against the system-level ESD test can be effectively enhanced.

Keywords*:* transient detection circuit, electrostatic discharge (ESD), system-level ESD, electromagnetic susceptibility (EMS).

Introduction

The traditional EMC (electromagnetic compatibility) works are mainly to reduce the EMI (electromagnetic interference) level of the printing circuit boards equipped with the integrated curcuits (ICs) and discreet components. Nowadays, the present EMC challenge is mainly focusing on how to improve the immunity of micro- (or nano-) electronics systems against the EMS (electromagnetic susceptibility) test. SoC (system on a chip) integration used the advanced CMOS technology to improve circuit speed and also to save the power consumption by using the scaled-down transistors with reduced VDD voltage level. With the smaller device dimension and the reduced voltage level, the logic states stored at the output nodes of logic gates would be easily destroyed by the transient noises during EMS events. With the reduced VDD voltage, the "logic threshold" (defined as VDD/2) of logic gates is lower. The immunity of logic gates against to EMS-induced noises becomes much sensitive. Thus, the SoC chips fabricated by the advanced CMOS technology are highly sensitive to EMS events, especially the ESD-induced transient disturbance.

The typical EMS tests to cause the failure or malfunction of microelectronics systems are the series of IEC 61000-4, especially the system-level electrostatic discharge (ESD) test. Under the system-level ESD test, specified in the standard of IEC 61000-4-2, the ESD-induced electrical transients can be randomly coupled into the power (V_{DD}) and ground (V_{SS}) lines of CMOS ICs equipped in microelectronic product [1]. These electrical transients can cause a hardware damage or system malfunction of CMOS ICs even if they have already passed the component-level ESD specifications [2]-[4]. In order to rescue the system from the abnormal state after system-level ESD tests, the on-chip circuit solution had been developed in some previous works [5]-[8]. It has been proven that an on-chip transient detection circuit co-designed with system operating firmware can help microelectronic products automatically executing recovery procedure without operator intervention to meet the immunity level of "Class B [1]", that has been widely requested by the commercial and consumer microelectronics products.

In this work, a new on-chip transient detection circuit is designed to detect system-level ESD-induced transients and verified in a 0.18-μm CMOS process with 1.8 V devices. The detection ability of the proposed circuit has been investigated by HSPICE simulation and evaluated by system-level ESD gun operated in indirect contact-discharge test mode.

New Transient Detection Circuit

A. Circuit Implementation

The circuit diagram of new proposed on-chip transient detection circuit is shown in Fig. 1. The circuit comprises with a resistor (R), an inverter structure (M_{p2} and M_{n2}), a feedback NMOS (M_{n1}), and a reset device (M_{nr}). M_{nr} is designed to provide the initial state and reset function of the proposed circuit. The resistor R, M_{n1}, and the inverter (M_{p2} and M_{n2}) compose a latch circuit as the memory cell of transient detection circuit. The RC delay structure is constituted by R and the total parasitic capacitors (C_P) at the node V_X.

Under initial state, the voltage level of the node V_O is set to logic "0" by M_{nr}. The output state of the proposed detection circuit is therefore kept at logic "0" through buffers. When the electrical transient disturbance is coupled to power lines under system-level ESD tests, due to the RC delay, the voltage of node V_x will respond much slower than the voltage coupled to V_{DD}. The device M_{p2} will be turned on to pull up the voltage level of node V_O. With the positive feedback device M_{n1}, the voltage level of node V_X will be pulled low to logic "0". Finally, M_{p2} will be turned on and M_{n2} will be turned off. Thus, when the system-level ESD events end, the output node V_{OUT} will be latched to logic "1" through two stage buffers. Therefore, the occurrence of electrical transient disturbance can be detected and stored.

The detection output is used as system recovery index to trigger the system operating firmware that can restore the system from frozen or upset state caused by system-level ESD events to a stable and known state. Therefore, the immunity of microelectronic products against the system-level ESD test can be effectively enhanced.

B. Simulation

The sinusoidal time-dependent voltage sources in HSPICE simulation are used to simulate the coupling transients on the power lines during system-level ESD tests. The simulated V_{DD}, V_{SS}, V_{RESET}, and V_{OUT} waveforms of the proposed transient detection circuit with a positive-going and negative-going underdamped sinusoidal voltage sources are shown in Fig. 2(a)

and Fig.2 (b), respectively. Under such conditions that the simulated positive (negative) system-level ESD transient disturbances coupled to V_{DD} and V_{SS} lines, V_{OUT} also acts with a corresponding positive (negative) underdamped sinusoidal voltage waveform. When the system-level ESD event ends, V_{DD} (V_{SS}) will return to 1.8 V (0 V), while V_{OUT} can remain to 1.8 V until the next V_{RESET} comes. As a result, the proposed transient detection circuit successfully detects and stores the occurrence of electrical transients which induced by system-level ESD events.

C. Experimental Results

The new proposed on-chip transient detection circuit has been fabricated in a 0.18-μm CMOS process with 1.8-V devices. Fig. 3 showed the micro photo of fabricated circuit, which only occupied a silicon area of 40μm × 50μm. The Vout signal after two buffers is sent to the PAD for experimental measurement.

The measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the new proposed on-chip transient detection circuit under system-level indirect contact-discharge test mode with +0.2 kV (-0.2 kV) zapping voltage are shown in Fig. 4(a) [Fig. 4(b)]. The voltage level of V_{DD} and V_{SS} are disturbed by the system-level ESD-induced transients, and rapidly increasing (decreasing) from 1.8 V and 0 V, respectively. The voltage level of V_{OUT} also increases (decreases) simultaneously. Finally, V_{OUT} of the proposed transient detection circuit transits from 0 V to 1.8 V. The detection sensitivity (as low as better) in the experiment is limited to the lowest voltage level (±200V) that can be generated by the ESD gun [1]. With a much higher ESD voltage, the huge transient disturbance during ESD test can be of course detected by the proposed detection circuit. The detection function of the proposed transient detection circuit is successfully verified by the positive and negative system-level ESD tests.

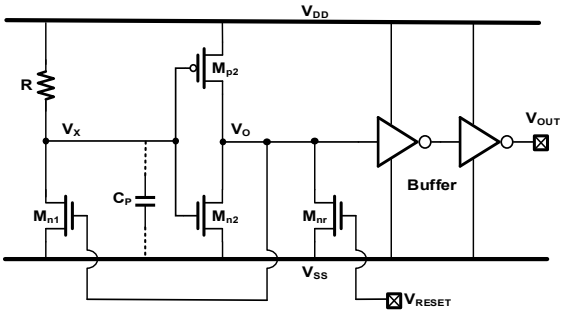
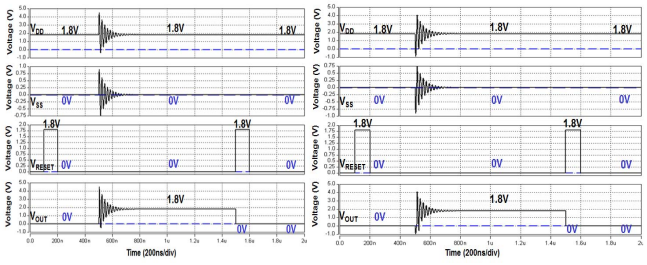


Fig. 1 The new proposed on-chip transient detection circuit.



(a) (b)

Fig. 2 Simulated V_{DD}, V_{SS}, V_{RESET}, and V_{OUT} waveforms of the proposed transient detection circuit under (a) positive, and (b) negative, system-level ESD-induced transients.

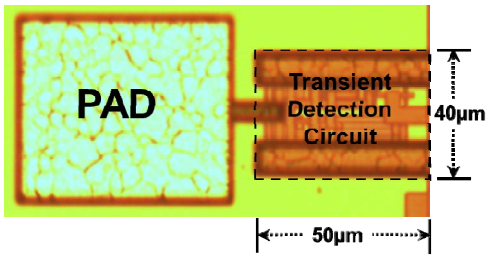
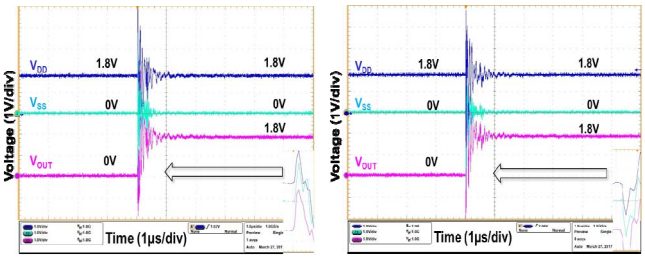


Fig. 3 Die photo of the new proposed on-chip transient detection circuit, which is fabricated in 0.18-μm CMOS process.



(a) (b)

Fig. 4 Measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the new proposed transient detection circuit under system-level ESD test with ESD zapping voltage of (a) +0.2 kV and (b) -0.2 kV.

Conclusion

A new on-chip transient detection circuit has been proposed and successfully verified in a 0.18-μm CMOS process with 1.8-V devices. The detection sensitivity is low to ±200V, under positive and negative system-level ESD tests. The proposed transient detection circuit can be co-designed with system operating firmware to provide a useful and effective solution, which can rescue the microelectronic products against malfunction after the electromagnetic susceptibility tests.

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