A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing

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Abstract

In this paper, a bone-guided cochlear implant (BGCI) SOC microsystem is proposed and designed. The BGCI microsystem uses four or more electrodes placed on the bone surface of the cochlea and one on the round window to preserve partially the acoustic hearing. The external SOC of the BGCI processes the acoustic signals and generates stimulation patterns and command that are transmitted to the implanted chip through the 13.56MHz wireless power and bidirectional data telemetry. The implanted chip with 4-channel high-voltage-tolerant stimulator generates biphasic stimulation currents up to 800µA and sends back the power indication and electrode impedance error signals to the external SOC. Electrical tests on the fabricated BGCI has been performed. The in-vivo animal tests on guinea pigs has shown the evoked Wave III of EABR waveforms. The proposed BGCI can be applied to patients with high-frequency hearing loss, tinnitus, and dizziness.

Introduction

Cochlear implants (CIs) or cochlear prostheses have been successfully used to help patients with serious sensorineural hearing loss by electrically stimulating the auditory nerves through an array of electrodes deployed inside the cochlea. But this raises the risks of meningitis or loss of residual acoustic hearing [1]. In this work, a bone-guided CI (BGCI) SOC microsystem with the electrodes deployed outside the cochlea are proposed to eliminate the aforementioned risks. In the proposed BGCI, four or more electrodes are placed on the bone surface of the cochlea and one is on the round window. The external unit of the BGCI is realized by a CMOS SOC. Through a pair of coils, data/power are transmitted to the CMOS chip of the implanted unit. The auditory nerves are stimulated by constant biphasic current pulses. While providing electrical hearing, acoustic hearing is partially preserved since the round window is not pierced during the surgery. Thus the proposed BGCI could be used to eliminate the symptoms for patients with high-frequency hearing loss, tinnitus, and dizziness. The functionality of the proposed BGCI microsystem has been verified in animal tests.

Architecture and Circuits

Fig. 1 shows the overall architecture of the proposed BGCI microsystem. In the external unit realized by a SOC, the acoustic signals are processed by a microphone and amplified and digitized by an acoustic signal acquisition circuit. Then the digitized signal is processed by an acoustic DSP to obtain the desired stimulation patterns. The patterns and the command are further processed and transmitted with power through the primary coil into the secondary coil and the implanted unit. The external SOC also contains a LSK demodulator and a decoder to handle the backward data from the secondary coil.

In the implanted unit, a power regulator with forward data decoding and backward data encoding circuits are implemented to obtain the wireless power and realize the bidirectional data telemetry. A 4-channel high-voltage-tolerant stimulator is designed to generate biphasic stimulus currents.

The acoustic signal acquisition circuit and the measurement results are shown in Fig. 2. The circuit consists of a configurable pre-amplifier and a 10-bit successive-approximation register (SAR) ADC. The pre-amplifier provides 4 levels of gains (1x, 1.5x, 2x, and 6x) for the input signal from 10Hz to 200kHz with constant group delay for auditory input. The pseudo-resistor (PR) is used to realize large resistance. The SAR ADC uses a monotonic capacitor switching algorithm. It can achieve an SNDR of 60.09dB and consume only 20.94µW, resulting in a figure of merit (FOM) of 528.4fJ/conversion-step in the audio band.

Fig. 3 shows the acoustic DSP and its signal processing flow. A spectral-change enhancement algorithm [2] is realized to enhance the speech intelligibility. The acoustic signals are transformed to frequency domain through real-value 64-ponit FFT, which has 44% power reduction compared to complex-value FFT. The magnitude of the frequency spectrum is re-shaped by auditory excitation pattern through a series of filtering, which is modeled as a peripheral auditory system. The outputs are then fed into a spectral change function to calculate the difference. The difference of the spectrum of interest is amplified by a Difference-of-Gaussians (DoG) function and the result is denoted as succeeding enhancement function (ENF). A weighting function is then applied to generate the desired frequency spectrum for the combined channels. The frequency range is adjustable to support the high-frequency hearing noise loss. Operated at 25MHz, the acoustic DSP dissipates 7.78mW from a 1V supply. The overall latency of the signal processing link is 1.33ms. The stimulation patterns are packed for wireless transmission. A packet contains a PN (Pseudo-random Noise) sequence for synchronization, a command (magnitude, polarity, duration) for the 4-channel high-voltage-tolerant stimulator, and appended CRC for error check.

Fig. 4 shows the wireless power and bidirectional data transmission system which consists of a programmable output power amplifier (POPA), a pair of coils, a power regulator, BPSK forward data modulator/demodulator, and LSK backward data modulator/demodulator. A pair of coils that resonates at 13.56MHz is used to transfer power and bidirectional data simultaneously. The wireless power is received by the secondary coil, rectified by the integrated 2X/3X active rectifiers. The regulated voltage of 2V (3V) is used to provide an input voltage for LDOs [3] (high voltage generator of the stimulator). A power detection circuit is used to detect the regulated voltage of 3V (stable between 3.01V and 3.18V) and sends back the power indication signal to the external SOC. The measured maximum efficiency of POPA is 62.5%. The measured power conversion efficiency (PCE) of the power regulator, composed of active rectifier and LDOs, is 59% for 25mW output power. The PLL-based BPSK demodulator is used to detect the frequency changes during data transmission. The LSK back telemetry provides a backward pathway to transfer back the power control signal of implanted chip and the error signal from electrode-impedance detectors.

The 4-channel high-voltage-tolerant stimulator [4] consists of a high voltage generator, a reference voltage generator, a quick discharge circuit, and 4 stimulus channels each containing a pair of stimulus drivers in the H-bridge topology, a current-mode DAC, and an error detector as shown in Fig. 5. If the impedance is too large, the error detector sends out an error signal as a backward data to the external SOC to stop the stimulation at this electrode. To reduce the peak current problem, the high voltage generator uses phase-shift clocks to pump V_{DDH} (3.25V) to V_{CC} (11V). The measurement results show that the stimulator can deliver 200μA to 800μA (100μA/step) stimulus currents to the electrodes.

Implementation

Both external and implanted units of the proposed BGCI are designed and fabricated in 0.18μm CMOS technology. The SOC chip for the external (implanted) unit occupies 12.26mm^2 (7.26mm^2) and dissipates 131.35mW (41.11mW). In the bidirectional data telemetry, a BPSK demodulator with 332μW power consumption, 0.98nJ/bit, and maximum 339kbps data rate as well as a LSK modulator with 105kbps are fully integrated on chip with the power telemetry. Fig. 6 shows chip micrographs and performance summary.

Animal Tests

Besides the electrical test, the proposed BGCI microsystem is tested in-vivo on guinea pigs to verify its functionality. The electrodes used in animal tests were made by gold plates on a flexible Silastic carrier. Each plate is 300μm in width, 2000μm in length, and 50μm in thickness. As shown in right of Fig. 7, electrical evoked auditory brainstem responses (EABRs) were recorded under biphasic current stimulation with a pulse width of 100μs/phase and different current levels from 200μA to 600μA. The measured EABRs waveforms under stimulation currents generated by a commercial stimulator (red lines) and the proposed BGCI microsystem (black lines) are shown in Fig. 7. It is seen that the Wave III of EABR waveforms can be recorded when the stimulation currents higher than 300μA from the BGCI microsystem or the commercial stimulator. As the stimulation current is increased, the amplitude of Wave III is also increased. Right of Fig. 7 shows the measured ABR amplitudes versus sound power level (SPL) of the proposed BGCI which verify the partial preservation of acoustic hearing. Note that the threshold difference in SPL between pre-operative ABR and post-operative ABR is due to opening the bulla cavity of guinea pig [5].

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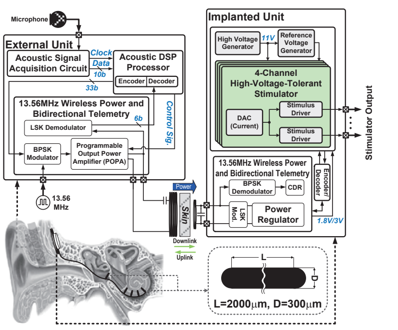


Fig. 1. Architecture of the proposed bone-guided cochlear implant microsystem.

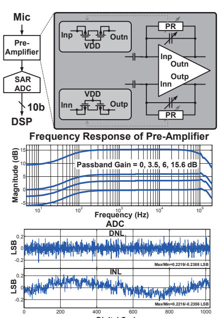


Fig. 2. Acoustic signal acquisition circuit.

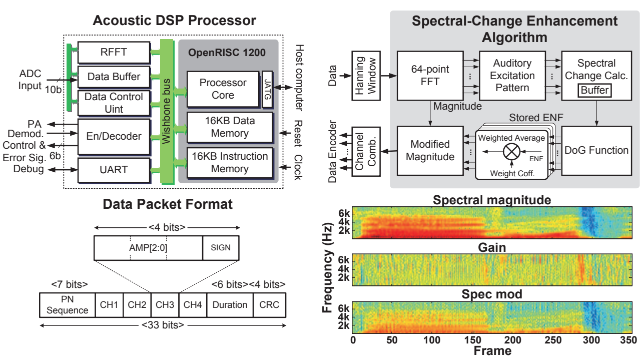


Fig. 3. Architecture and algorithm of acoustic DSP.

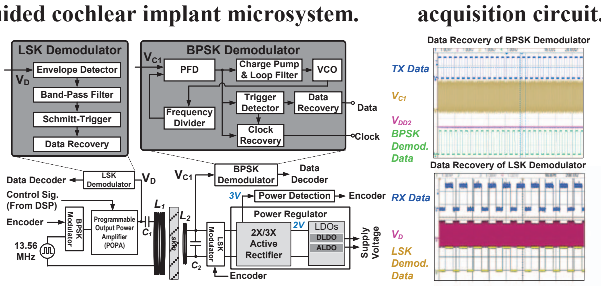


Fig. 4. Wireless power and bidirectional data telemetry system.

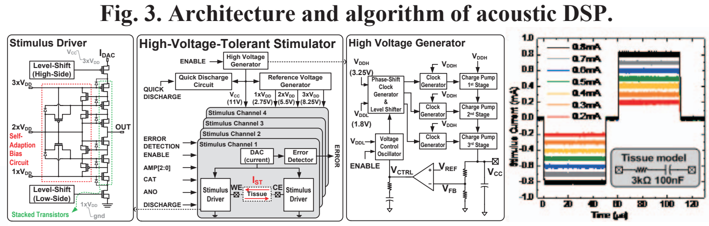
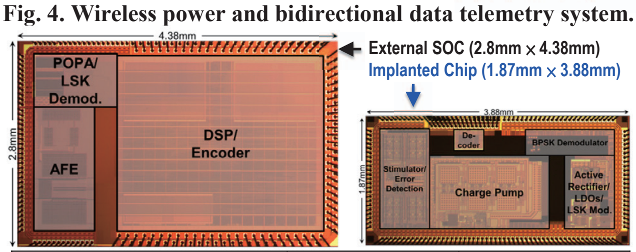


Fig. 5. High-voltage-tolerant stimulator.



		This work	Cochlear Ltd., Nucleus N6 [1]
Placement of Electrode Arrays		Bone surface of the cochlea, round window	Inside the cochlea
Core Voltage Supply (V)		1.8/3	NA
Acoustic Signal Acquisition Circuit	Frequency Range (kHz)	0.01-200	0.1-8
	Gain (dB)	0/3.5/6/15.6	NA
	SNDR (dB)	60.09	NA
	ENOB	9.69@48kS/s	NA
	INL/DNL (LSB)	0.24/0.24	NA
Data Telemetry	Carrier Frequency (MHz)	13.56	5
	Max. Data Rate (kbps)	339 (Downlink), 105 (Uplink)	500 (Downlink)
Stimulator	Number of Electrodes	4	22
	Supply from Charge Pump (V)	11	NA
	Pulse Width (μs/phase)	0~146@212kbps	9.6~400
	Max. Stimulation Current (mA)	0.8	1.75
	Total Stimulation Rate (pps)	3000	32000

Fig. 6. Chip micrographs and performance summary of the proposed BGCI microsystem.

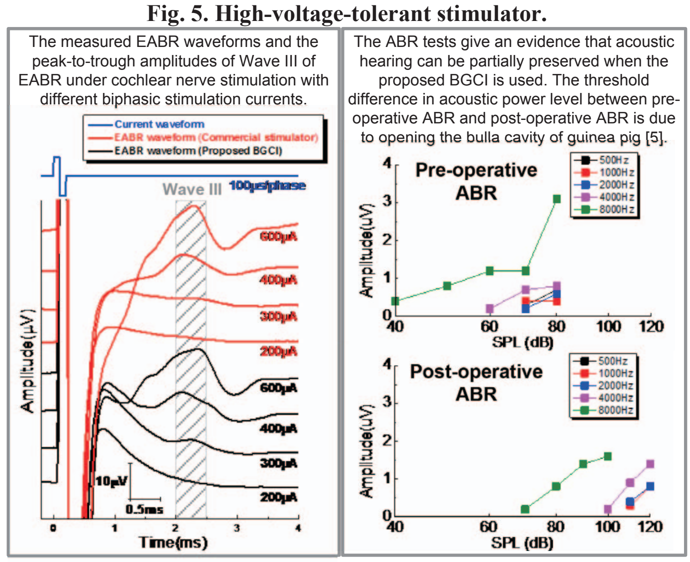


Fig. 7. Measurement results of in-vivo animal tests on guinea pigs.