A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-directional Data Telemetry for Real-Time Human Epileptic Seizure Control

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Abstract

This paper presents a 16-channel closed-loop neuromodulation SoC for human seizure control. The SoC includes a 16-ch signal acquisition unit, a bio-signal processor, a 16-ch adaptive stimulator, and wireless telemetry. The signal acquisition unit achieves 3.78 NEF and shares electrodes with stimulator. The seizure detection latency is 0.76s and delivered 0.5-3mA biphasic current stimulation. The SoC is powered wirelessly and bidirectional data telemetry is realized through the same pair of coils in 13.56MHz.

Introduction

Epilepsy, the common neurological disorder, afflicts about 1% of world's population. As shown in clinical data [1], up to 3mA electrical stimulation on cortical surface at seizure onset sites is required to control human epileptic seizures. Recently, implantable devices with closed-loop electrical stimulation for seizure control have been presented [2], [3] as a potential and efficient clinical treatment. However the electrical stimulations in [2]-[4] could not satisfy the above requirement. This paper presents a closed-loop neuromodulation SoC with adjustable 0.5−3mA biphasic current stimulation. The SoC is powered wirelessly and bidirectional telemetry is realized through the same pair of coils in ISM band (13.56MHz). The functionality of the fabricated chip is verified by using human epileptic seizure waveforms.

Proposed Closed-Loop Neuromodulation SoC

Fig. 1 shows the architecture of the neuromodulation SoC, where a neural-signal acquisition unit (NSAU), a bio-signal processor (BSP), a high-voltage-tolerant stimulator (HVTS), and a wireless power and bidirectional data telemetry are integrated. The NSAU amplifies and digitizes the sensed electrocorticogram (ECoG) signals. The digitized data are then processed by BSP for seizure detection. Once the seizure is detected, the HVTS generates biphasic stimulation currents to suppress seizure onset. The external control system consists of a class-E power amplifier (PA) and a bidirectional data transceiver. The control parameters in Binary Phase-Shift Keying (BPSK) form and the power of SoC are transmitted from PA to SoC through the coil. The seizure detection result and the recorded ECoG in Load-Shift Keying (LSK) form are transmitted back from SoC to external control system through the same coil.

The 16-channel NSAU in Fig. 2 consists of 16 auto-reset chopper-stabilized capacitive-coupled instrumentation amplifiers (AR-CSCCIA), band-pass filters, programmable transconductance gain amplifiers, a multiplexer, a transimpedance amplifier, and a 10b SAR ADC. The AR-CSCCIA suppresses flicker noise with chopper circuit. Both ripple reduction loop (RRL) and offset reduction loop (ORL) are adopted to reduce chopper induced artifacts. The RRL is composed of 7-bit current DACs, a comparator, and a local RRL digital control. The DACs are controlled by the local RRL digital control to reduce output ripple by successive-approximation calibration. The ORL is composed of a low-pass filter and a differential pair to reduce output offset. As shown in Figure 2, the NSAU provides a 3-step gain (50, 60 and 70dB) for patient-specific signal scaling. The input-referred noise is reduced 63.6% by using chopper modulation and the NEF of AR-CSCCIA is 3.78.

During the seizure period, both signal entropy and FFT show significant changes in the band of 4−64Hz. Thus entropy and 15 mean band power are extracted as main features to detect the seizure onset. Fig. 3 shows the BSP hardware diagram and the simulation results with ECoG signal of seizure onset. 128 points are sampled in 1s and processed by 128-point decimation-in-frequency (DIF) FFT. The ridge regression classifier determines the seizure onset channel within 0.36ms calculation time. The accuracy, sensitivity, and specificity are 97.8%, 96.0%, and 100%, respectively, that are better than those in [4].

Fig. 4 shows the 16-channel HVTS with the shared pre-amp input circuit of NSAU, which consists of an adaptive regulated charge pump with 3-stage charge pump and 3V input, a current DAC with triode indicator, a decoder, and 16-ch stimulus drivers. The stimulation current pulses are adjustable from 0.5mA to 3mA. Transistors M_{B1} to M_{B6} act as a self-adaption bias circuit to keep the voltages across each MOS device in the stacked transistors within 3.3 V under 4xVDD (12V) power supply [5]. During the stimulating period, the NSAU is disconnected from the electrodes to prevent electrical overstress by the gate control signal to M_{D2}. After stimulation artifact vanishes, the NSAU is reconnected to the electrodes through M_5, M_6, M_7, and M_{D2} by the self-adaptive bias circuit and control signal to read out ECoG signals. A triode indicator is used to control the charge pump that provides an adaptive power supply at the 4xVDD node to ensure M_{C3} and M_{C4} in saturation region. The measurement results show that the proposed stimulator can step up or down following the electrode voltage from 8V to 11.5V without degrading the performance of charge balance. Using adaptive power supply can increase power efficiency of HVTS to 54% from the original 37% with a fixed 4xVDD of 12V, under the stimulus current of 3mA.

Fig. 5 shows the architecture of wireless power and bidirectional data telemetry, including a 2X/3X active rectifier, 2 LDOs, a BPSK demodulator, and a LSK modulator. The received AC signal in secondary coil is regulated by a 2X/3X delay compensation active rectifier. The regulated 2V is connected to LDOs for further regulating and the regulated 3V provides the input voltage of HVTS. The power conversion efficiency from PA through coil to rectifier is 48%. The downlink data is demodulated by the developed PLL-based edge-detection BPSK demodulator where BPSK data edge is detected by phase-frequency detector in PLL and processed for clock and data recovery. Furthermore, LSK is implemented to transmit the recorded ECoG signals and the seizure detection result to external device for monitoring purposes. The energy

consumption of BPSK demodulator and LSK modulator are 1.027nJ/b and 0.14nJ/b with 330Kbps and 100Kbps, respectively.

Animal Experimental Results

The functionality of the fabricated closed-loop neuromodulation SoC in 0.18µm CMOS technology was verified with the recorded ECoG seizure waveforms of a mini pig. Fig. 6 shows the measured ECoG and the generated stimulus pulses from the SoC. The seizure onset is detected and the stimulus current of 3mA is delivered to the electrode within 0.76s. Further animal in-vivo tests are undergoing. Comparison results with [2]-[3] are given. Fig. 6 also shows the chip micrographs of the SoC and the external control chip.

Conclusion

The SoC in 25mm^2 chip area fully integrates a 16-ch NSAU, a BSP, a 16-ch HVTS, and wireless power and data telemetry. The detection latency is 0.76s and up to 3mA biphasic current stimulation is used to suppress the human epileptic seizures. The closed-loop neuromodulation SoC is demonstrated to be a feasible solution for treating human epilepsy.

References

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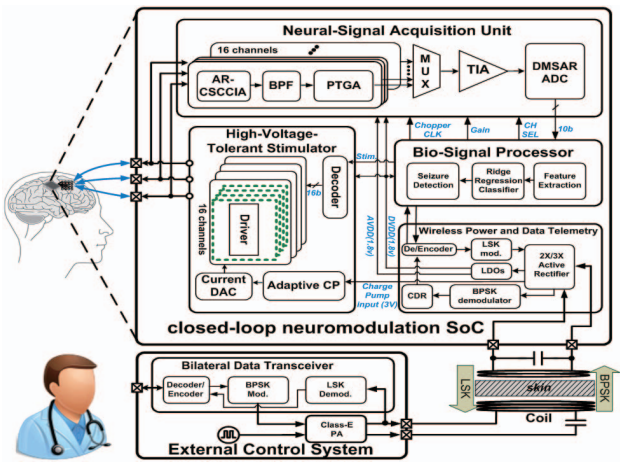


Fig. 1. Architecture of the closed-loop seizure-control SoC.

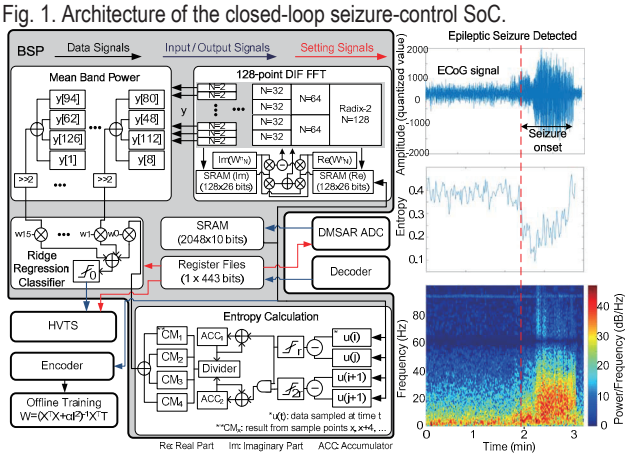


Fig. 3. Hardware implementation of BSP for epileptic seizure detection.

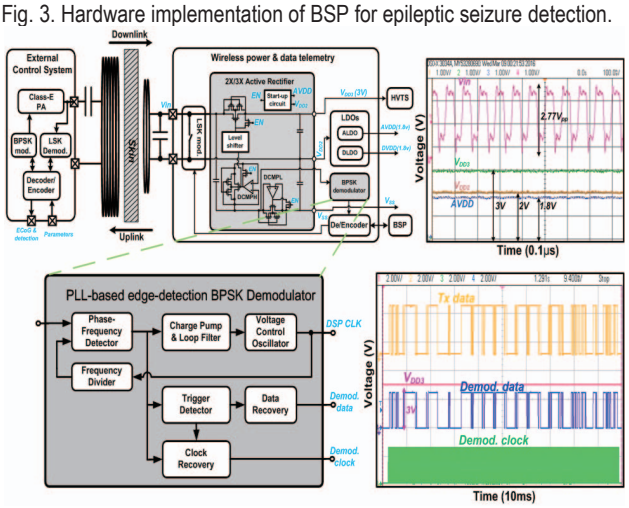


Fig. 5. Wireless power and bidirectional data telemetry.

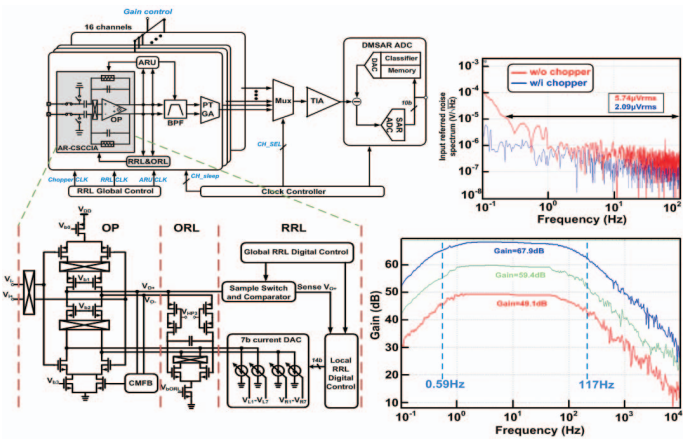


Fig. 2. Neural-signal acquisition unit (NSAU) with auto-reset chopper-stabilized capacitive-coupled Instrumentation Amplifier (AR-CSCCIA).

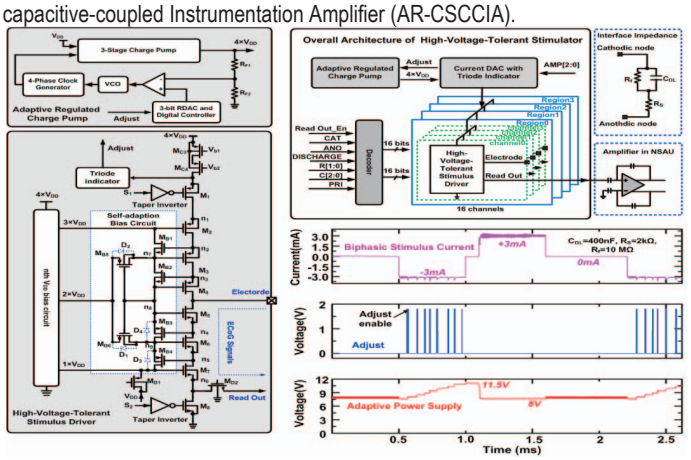
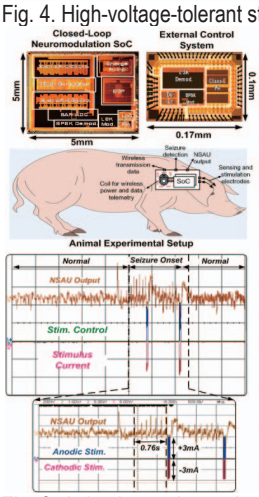


Fig. 4. High-voltage-tolerant stimulator with the shared input circuit of NSAU.



Comparison Table

	ISSCC'13 [2]	JSSC'16 [3]	This Work
Process	TSMC 0.18µm	IBM 0.13µm	TSMC 0.18µm
# of channels	8	64	16
Input referred noise (μV_{rms})	5.23	4.2	2.09
NEF	1.77	6.9	3.78
Accuracy	92%	88-96%	97.76%
Latency	0.8s	n.a	0.76s
BSP Efficiency	77.91µJ/ (feature ext. + classification)	n.a	62.5µJ/ (feature ext. + classification)
Charge pump stage (PCE)	5 (38%)	No	3 (54%)
Stimulation	30µA biphasic	10-1000µA biphasic	500-3000µA biphasic
Adaptive stimulation control	Yes	No	Yes
Power dissipation	2.8mW (standby)	2.17 mW (UWB) 5.8mW (FSK)	3.12mW (standby) 54mW (stimulation)
Wireless transmission	Dual-band (13.56M, 400MHz)	Quad-band (1.5M, 916.4M, <1G, 3.1-10G)	Single-band (13.56MHz)
Power transfer efficiency	~8.3% (Overall) * 84.8% (Only rectifier)	40% (overall)	48% (overall)

*:Using external buffer as power transmitter

Fig. 6. Animal experimental results of the fabricated closed-loop seizure control SoC and comparison table.