On-chip Transient Detection Circuit for Microelectronic Systems against Electrical Transient Disturbances due to ESD Events

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***Abstract*—A new on-chip transient detection circuit which can detect electrical disturbances of system-level electrostatic discharge (ESD) is proposed. The circuit is designed with reduced physical area by utilizing dual-latched structure. With hardware/firmware co-design method, auto-recovery procedure can be activated by the detection circuit when microelectronic systems suffer system-level ESD events. The immunity level of microelectronic products against the electromagnetic interference (EMI) of ESD events can be effectively improved. The proposed on-chip transient detection circuit has been verified in a 0.18-µm CMOS process with 1.8-V devices under system-level ESD tests.**

Keywords—electromagnetic compatibility (EMC); electrostatic discharge (ESD); system-level ESD; transient detection circuit.

I. INTRODUCTION

Electromagnetic compatibility (EMC) has become an important reliability issue in microelectronic systems equipped with CMOS ICs. CMOS ICs fabricated by the advanced CMOS technology are more vulnerable to the electromagnetic interference (EMI) due to ESD events, since the CMOS devices have been scaled down for high-speed and low-power applications with the reduced operating voltage level. As the voltage levels of logic gates are reduced, such as from 3.3 V to become 1.8 V or even lower, the noise margin (defined as $V_{DD}/2$) of logic gates against the transient noisy pulses is also degraded. It has been found that microelectronic systems equipped with CMOS ICs can be damaged or dysfunctional by system-level ESD events even though the CMOS ICs have passed the component-level ESD specifications [1], [2]. For IoT applications achieved by CMOS ICs, the IoT environments would be often the open fields without any ESD control. The silicon chips inside the IoT devices may be interrupted by ESD-induced transient disturbances to cause the micro-electronic system into a frozen or upset state .

Therefore, based on demand of reliability from IC industry, the international standard IEC 61000-4-2 has been established to specify the immunity level against system-level ESD events [3]. Under interferences of system-level ESD events, the fast electrical transients will randomly couple into power lines and I/O ports of CMOS ICs inside the microelectronic systems to disturb the system operation. Table I shows the evaluation of system-level ESD events, which is classified by the response of the equipment under test (EUT) after system-level ESD tests. Typically, a user-friendly microelectronic product has to pass the specification "Class B," which means the products have to be automatically recovered after the systems suffer from EMI/ESD issues. To meet the specification, the hardware/firmware co-design method had been introduced [4]. With the combination of a transient detection circuit and system programming, auto-recovery procedure can be activated without operator manual intervention.

Some transient detection circuits had been reported, which can detect fast electrical transients by RC network [5], [6]. Fig. 1 shows a typical on-chip transient detection circuit [7]. Two 500fF coupling capacitors are utilized to enhance detection sensitivity. However, no matter resistors or capacitors usually occupy large silicon area in IC layouts. It has been studied that the incorporation of a regenerative feedback network for detecting ESD transients is beneficial to the required RC time constant reduction by latching the detection output state after ESD events [8].

TABLE I. EVALUATION OF SYSTEM-LEVEL ESD TEST RESULTS [3]

CRITERION	CLASSIFICATION
CLASS A	Normal performance within limits specified by the manu-facturer, requestor or purchaser.
CLASS B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal perfromance, without operator intervention. **(Automatic Recovery)**
CLASS C	Temporary loss of function or degradation of performance, the correction of which requires operator interventions. **(Manual Recovery)**
CLASS D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

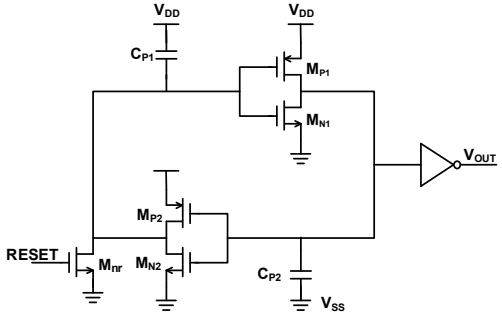


Fig. 1. Prior design of transient detection circuit [7].

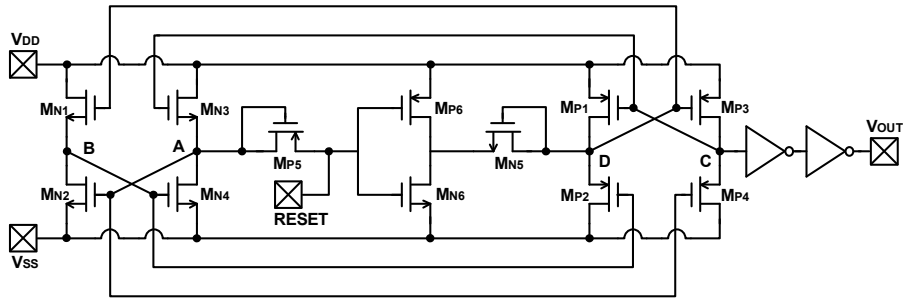


Fig. 2. The circuit diagram of the proposed on-chip transient detection circuit.

In this work, a new transient detection circuit with dual-latch structure is proposed, which is inspired by the previous memory design against the SEU hardened issues [9]. The proposed detection circuit can successfully memorize the occurrences of ESD-induced transient disturbances without using any coupling capacitor. The on-chip transient detection circuit has been fabricated in a 0.18-μm CMOS process with 1.8-V devices. The detection capability of the proposed circuit has been successfully verified by system-level ESD tests.

II. Transient Detection Circuit

A. Circuit Implementation

The proposed on-chip transient detection circuit is a dual-latch cell with initial control structure, as illustrated in Fig. 2. The two diode-connected MOSFETs (M_{P5} and M_{N5}) and an inverter (M_{P6} and M_{N6}) are used to initialize the output voltage of the detection circuit by a control signal "RESET" of V_{DD}. The dual-latch cell is composed by two groups of stacked NMOS (M_{N1}+M_{N2} and M_{N3}+M_{N4}) and the other two groups of stacked PMOS (M_{P1}+M_{P2} and M_{P3}+M_{P4}), which had been applied in RAM cell design against the Single Event Upset (SEU) issue [9]. In this work, this structure is used to memorize the occurrences of the transient interferences after system-level ESD events. The dimensions of transistors in dual-latch structure need to be well designed to enhance the sensitivity of the detection circuit. In order to effectively pull down the voltage levels of node A and node C, the size of transistors M_{N4} and M_{P4} are designed larger than that of M_{N3} and M_{P3}, respectively, to provide larger parasitic capacitance as coupling capacitance. On the contrary, M_{N1} and M_{P1} are designed larger than M_{N2} and M_{P2}, respectively, to pull up the voltage levels of node B and node D easily.

Under the normal power-on condition, after the reset operation on M_{P5} and M_{N6}, the node A will be charged to high potential of logic "1" and the node D will be discharged to low potential of logic "0." Hence, the voltage of the node B will be pulled down by M_{N2}, and the voltage of the node C will be pull up by M_{P3}. As a result, V_{OUT} will be biased at V_{DD} of logic "1." During system-level ESD events, power lines are randomly subjected to the coupling electrical transient pulses. The inverse logic states are stored owing to the equivalent resistance and capacitance of transistors in dual-latch cell. Therefore, the logic states at node A and node C are transferred to "0" from "1." On the contrary, the logic states at node B and node D are transited to "1" from "0." Consequently, the logic state of V_{OUT} will be changed to logic "0" from logic "1." As a result, the occurrences of system-level ESD events can be recorded by the proposed detection circuit. The parasitic resistors and capacitors of transistors in the detection circuit provide a RC time constant which can detect the fast electrical transients of the system-level ESD events. The double regenerative feedback networks of dual-latch structure not only improve the detection sensitivity but also enhance the robustness of logic state after detecting the induced interferences of system-level ESD events. This greatly reduces the requirement of time constant, therefore it can further shrink the physical area of the detection circuit in the chip layout.

B. Simulation

The function of the proposed transient detection

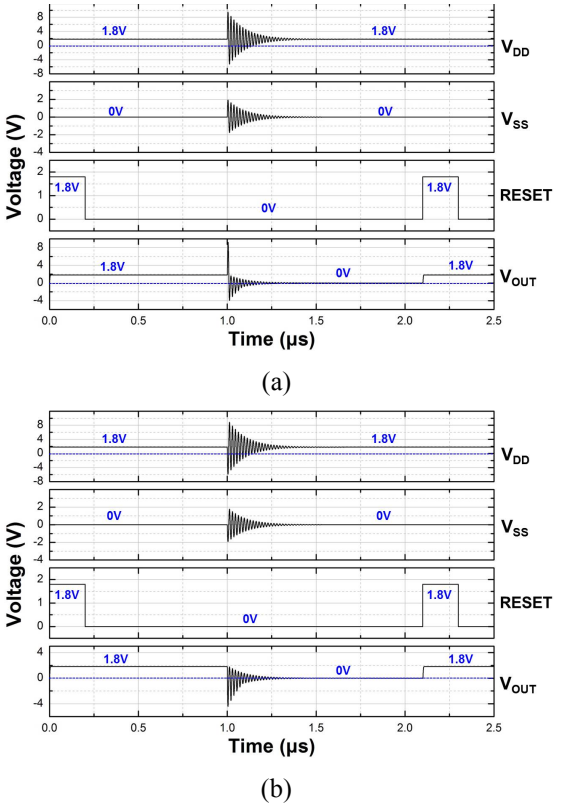


Fig. 3. Simulated V_{DD}, V_{SS}, RESET, and V_{OUT} waveforms of the proposed transient detection circuit under (a) positive and (b) negative system-level ESD transient tests.

circuit has been investigated by HSPICE simulation. An underdamped sinusoidal voltage source with a designed damping factor simulate electrical transients induced from the system-level ESD [5]. Figs. 3(a) and 3(b) present the simulated V_{DD}, V_{SS}, RESET, and V_{OUT} waveforms of the proposed transient detection circuit under positive and negative system-level ESD test, respectively. The initial dc voltages of V_{DD} and V_{SS} are biased at 1.8 V and 0 V under the normal power-on operation. With the positive-going ESD transient voltage in Fig. 3(a), a voltage amplitude of +8 V is applied on V_{DD} and a voltage amplitude +2 V is applied on V_{SS} at the same time.

When the power lines (V_{DD} and V_{SS}) are subjected to the simulated system-level ESD disturbances, the output voltage of the detection circuit (V_{OUT}) will be elevated to a high voltage and disturbed by transient noises simultaneously. After that, the voltage of V_{DD} and V_{SS} will recover to 1.8 V and 0 V, while V_{OUT} will be transferred to 0 V from 1.8 V until reset operation is executed by the "RESET" signal.

Fig. 3(b) presents the simulated waveforms under a negative system-level ESD test. Voltage amplitude as a negative-going ESD voltage which are applied on V_{DD} and V_{SS} are -8 V and -2 V, respectively. The transient responses of V_{OUT} rapidly ramp down while the detection circuit undergoes the injection of the negative system-level ESD disturbances. After the transients, V_{OUT} will be stably kept at 0 V before the "RESET" signal of 1.8 V reset the detection circuit. Therefore, from the both positive and negative system-level ESD simulation, the proposed transient detection circuit manages to detect the occurrences of system-level ESD events.

III. Experimental Results

The proposed on-chip transient detection circuit has been fabricated in a 0.18-µm CMOS process with 1.8-V devices. The die photo of the fabricated detection circuit is shown in Fig. 4, where the silicon area is 60 µm x 40 µm. The detection capability is verified under system-level ESD tests with indirect contact-discharge mode. The standard measurement setup of system-level ESD test has been specified in IEC 61000-4-2 standard [3]. Fig. 5 shows the measurement environment with test chip as EUT. The measured waveforms can be observed by an digital oscilloscope. A wooden table stands on the ground reference plane (GRP). The EUT is isolated from the horizontal coupling plane (HCP), which is placed on the table by an insulation pad. The

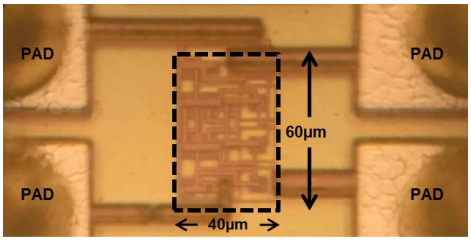


Fig. 4. Die photo of the proposed on-chip transient detection circuit which is fabricated in a 0.18-µm CMOS process.

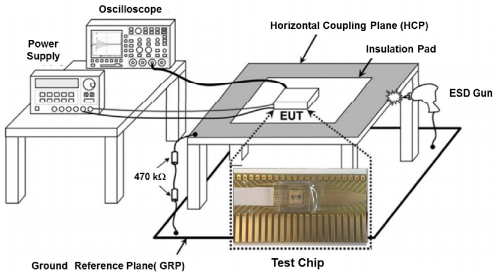
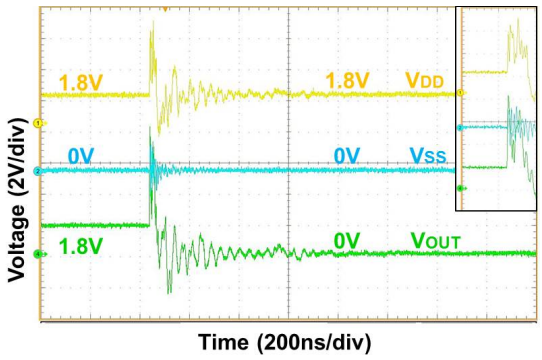


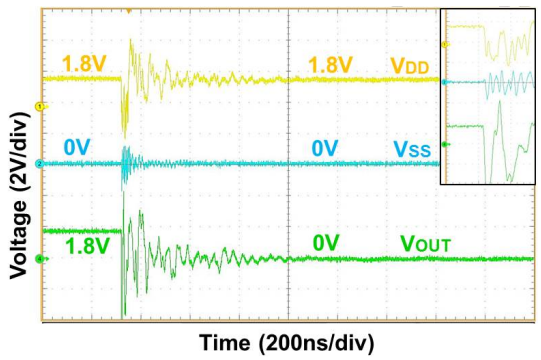
Fig. 5. Measurement environment for a system-level ESD test with indirect contact discharge mode [3].

HCP is connected to the GRP with two 470-kΩ resistors in series, and the discharge return cable of the ESD gun is connected to the GRP. With ESD gun as a system-level ESD generator, ESD-induced electrical transients can couple onto the power lines of the CMOS ICs inside the EUT.

Figs. 6(a) and 6(b) present the measured V_{DD}, V_{SS}, and V_{OUT} waveforms under positive and negative system-level ESD tests, respectively. The initial dc voltage of V_{DD} and V_{SS} are set at 1.8 V and 0 V by power supply. V_{OUT} is initialized to 1.8 V under normal circuit opertaing condition. The transient responses of V_{DD}, V_{SS}, and V_{OUT} under an ESD zapping voltage of +0.2 kV are presented in Fig. 6(a). As a system-level ESD event occurs, both power lines (V_{DD} and V_{SS}) are disturbed by the injection of fast transient noises. The potential on V_{DD}, V_{SS}, and V_{OUT} ramp up simultaneously. After system-level ESD ceases, the



(a)



(b)

Fig. 6. Measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit under system-level ESD tests with ESD voltages of (a) +0.2 kV

voltage levels on V_{DD} and V_{SS} recover to 1.8 V and 0 V, respectively. However, the potential on V_{OUT} is transited to 0 V from 1.8 V.

Fig. 6(b) shows the measured V_{DD}, V_{SS}, and V_{OUT} waveforms of the detection circuit under an ESD zapping voltage of -0.2 kV. When system-level ESD interferences inject onto the power lines ,V_{DD} and V_{SS} voltage levels rapidly decrease and the V_{OUT} potential is disturbed as well. After the disturbances of damping noises, the voltage levels of V_{DD} and V_{SS} will recover to 1.8 V and 0 V, whereas V_{OUT} is changed and retain to 0 V from 1.8 V. Therefore, the measurement results indicates that, under both positive and negative system-level ESD tests, the proposed on-chip transient detection circuit can successfully detect and record the occurrences of system-level ESD events.

IV. System Application

In order to improve the system stability of micro-electronic products, the proposed transient detection circuit works with firmware to perform auto-recovery procedures after the systems are disturbed by system-level ESD events [4]. Fig. 7 depicts the flowchart of the firmware design. The power-on reset operation will initialize the output of transient detection circuit to logic "1." The detection result (V_{OUT}) of the on-chip detection circuit can be temporarily stored as an index for firmware to check the safety of the microelectronic systems. The reset operation will proceed to normal operation after checking the safety index is "1," which means that there is no safety concern at the time.

When a system-level ESD event occurs, the output of the detection circuit will set the safety index to logic "0," and the reset procedure of firmware check will be activated to carry out auto-recovery procedures. After the recovery, a feedback signal will also conduct the reset procedure to reset the transient detection circuit. Therefore, the proposed transient detection circuit in cooperation with the firmware design is helpful to the functions of microelectronic products to free from the electrical disturbances induced by system-level ESD events. The micro-electronic system can be automatically recovered within only few milliseconds.

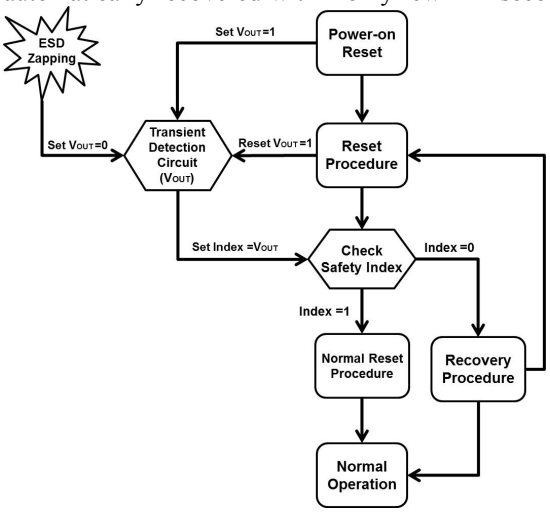


Fig. 7. The application flowchart of firmware co-design with the proposed detection circuit for system-level ESD protection.

With the hardware/firmware co-design, the detection circuit provides an efficient approach for microelectronic products against electromagnetic interferences, so as to meet the "Class B" specification of IEC 61000-4-2 standard.

V. Conclusion

A new on-chip transient detection circuit for micro-electronic systems against electrical transient disturbances due to ESD events has been proposed and verified in a 0.18-μm CMOS process with 1.8-V devices. With the cooperation between the detection circuit and system programming, auto-recovery procedure can be executed in a short clock cycles, when microelectronic system is suffering ESD-induced transient disturbances. Therefore, the immunity level of microelectronic products (especially, such as the IoT applications in the open fields) against the electrical transient disturbances due to ESD events can be efficiently enhanced.

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