Design of Multi-Channel Monopolar Biphasic Stimulator for Implantable Biomedical Applications

Chia-Chi Hsieh and Ming-Dou Ker
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
mdker@ieee.org

***Abstract*—Neuro-stimulators have been widely used in neural disorder control. This work presents a four-channel stimulator with adjustable positive and negative stimulus voltage from ±0.5V to ±8V. In the proposed stimulator, circuit operation with negative voltage has been successfully realized in a 0.25-μm 2.5-V/5-V/12-V CMOS process with the grounded p-type substrate, and without suffering the p-n junction breakdown or electrical overstress issues. The proposed stimulator has been also practically verified with *in-vivo* animal test. By integrating the stimulator circuit with other circuit blocks together, the close-loop neuromodulation treatment can be implemented by an implantable system-on-chip (SoC) with low-power consumption.**

Keywords—stimulator; neural stimulation; in-vivo animal test; SoC integration.

I. INTRODUCTION

Neurological disorder causes abnormal electrical activity in the brain that further affects the motor system, such as Parkinson's disease and epilepsy. Instead of drugs, deep brain stimulation (DBS) treatment is used recently. Stimulation therapies are also used in retinal layer for blind patients, or cochlear implant for the deaf. Moreover, stimulation methods can be divided into the voltage mode and the current mode, as well as the electrode configuration has the monopolar and the bipolar styles. No matter which stimulator structure is required, the biphasic (cathodic/anodic) pulse shown in Fig. 1 is needed for minimizing redundant charges in the body to avoid physiological harm [1]. For implantable biomedical application, electrode-tissue impedance vary with the size and position of the electrode. For current stimulator, output voltage is decided by the product of stimulus current and impedance value. However, if the loading impedance becomes larger due to tissue fluid between electrodes and tissue surface, the desired stimulus current will be limited by the voltage headroom of output driver. On the other hand, as long as the voltage stimulator can deliver an expected stimulus voltage to ideal impedance, when wide range of stimulus voltage is designed, it may be more suitable to cover impedance variation. The monopolar configuration typically needs two high voltage power supplies to realize the biphasic stimulation, where the positive one (+VCC) is for anodic pulses and the negative one (−VCC) is for cathodic pulses. Although one more power supply is needed as comparing to the bipolar configuration, the characteristic of one interconnect lead per site reduces the risk during surgery. Besides, monopolar system generates biphasic pulse through one channel that can be realized with half of the number of stimulator drivers and less the chip area, as comparing to the bipolar configuration. The therapeutic effects of bipolar or monopolar stimulation had been discussed in some articles [2], [3], and the monopolar configuration was a general usage in laparoscopic electrosurgery [4].

In this work, a four-channel monopolar voltage stimulator is designed to generate biphasic pulses for neuro-stimulation. The impedance of electrode-tissue to monopolar configuration can be measured and modeled as an equivalent circuit consists of parallel resistor (R_f) and capacitor (C_{dl}) with a series resistor (R_S) [5]. By integrated with several circuit blocks, including wireless power supply, multiple-charge-pump (MCP) system, bio-signal processor (BSP), analog front-end (AFE), and stimulator, a closed-loop neuromodulation treatment can be implemented in an implantable system-on-chip (SoC) [6].

The structure of monopolar configuration with load impedance is shown in Fig. 2, where the proposed stimulator can deliver full-scale stimulus voltage of ±8V for tissue impedance (R_S) above 500Ω. With negative voltages involved, p-n junction breakdown issue has to be taken into design consideration, when the p-type substrate is grounded, instead of the most negative voltage in the system.

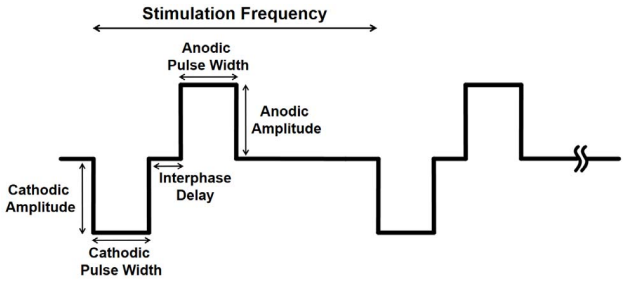


Fig. 1. Biphasic stimulus pulses.

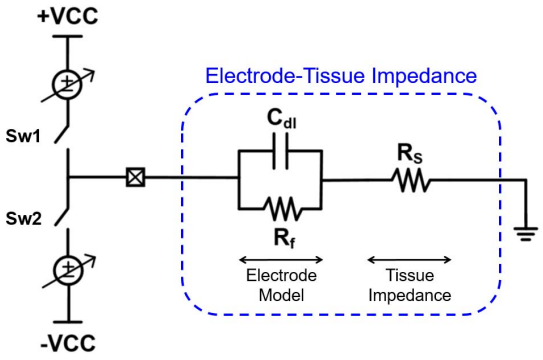


Fig. 2. A brief structure of monopolar configuation with equivalent circuit model of electrode-tissue impedance load.

II. Proposed Voltage Stimulator

The block diagram of proposed monopolar biphasic voltage stimulator is shown in Fig. 3. The stimulator is designed for biomedical applications with SoC integration, so the operating voltages of 1.8V and 3V are provided from power management unit. Negative DAC generates a negative reference voltage, thus a low negative voltage supply (−3V) is needed. A MCP system, consisted with a positive charge pump and two negative charge pumps, serves as voltage generator to provide the desired positive and negative voltages. Because +VCC and −VCC can exist simultaneously, the driver voltage compliance is as high as 20V. To minimize the leakage current, all stimulus drivers remain to high-Z state when enable signal (ST_EN) is logic low, i.e. the two switches Sw1 and Sw2 in Fig. 2. are open. During stimulation period, where ST_EN is logic high, the parameters such as frequency, pulse width, amplitude, and cathodic/anodic pulse order are programmable, and one of the four channels will be selected to deliver biphasic pulses. The stimulator includes discharge function for safety consideration, which lessen the residual charges in the tissue after biphasic stimulation is finished.

A. Control Circuit

Digital input signals will be processed through control circuit block, then those signals serve as one of the input signal to DAC or pass to the drivers for switch control. There are 2-bit channel choosing signals defined by C[1:0] in Fig. 3. The output waveform is decided by the input information of cathodic (CAT), anodic (ANO), and discharge (DIS) signals. Control circuit makes the operation interface more user-friendly with simple setup to produce the desired stimulus voltage.

B. Voltage Reference DAC

Fig. 4 presents the DAC circuit in detail. With 4-bit of amplitude input, the stimulus voltage can be provided from ±0.5V to ±8V with step amplitude of 0.5V. In order to deliver the target voltage, the positive and negative reference voltages (Pref and Nref) will be generated first. Different from traditional binary code DAC, thermometer code DAC is used [7] owing to the advantage of reducing glitch current. Besides, same weighted of MOSFETs in the thermometer code DAC is beneficial to layout matching and array arrangement, thus output accuracy is also improved. Another input signal called AMP_DIS in Fig. 4 is related to discharge. In discharge phase, AMP_DIS is logic high to turn off all switch transistors in the DAC.

1) Positive Voltage DAC: First of all, digital inputs transfer to 16-bit thermometer code by the decoder. However, low-side level shifter is required to shift 1.8V to 3V for correct logic control of DAC. Second, a reference current source is generated by a structure similar to LDO. Ouput voltage of the amplifier used as bias voltage of Mpb0 to Mpb15 (PMOS string). By sizing the ratio of Mpb to PMOS string and controling trun-on or turn-off operations of Mps0 to Mps15 (PMOS switches), a corresponding current is provided and converted to the positive reference voltage (Pref) by resistor.

2) Negative Voltage DAC: The operating principle of negative voltage DAC is similar to that of positive voltage DAC. The major difference is to change PMOS string by NMOS string (Mnb0 to Mnb15), and replacing PMOS switches by NMOS switches (Mns0 to Mns15). Under the circumstance of negative voltage operation, unlike the LV NMOS that can be surrounded by deep N-well, the PMOS device may suffer from N-well and P-substrate junction forward-leakage when P-substrate voltage is 0V. To aviod the leakage issue, all the bulk voltage of LV PMOS should be biasd at 0V, which has to be careful of overstress or junction breakdown issue with consideration of process limitation. Another reason for using NMOS of negative DAC is that NMOS switches turn on with gate bias at high, therefore voltage level of 0V and −3V act as logic high and logic low to negative DAC. On the contrary, PMOS switches turn on with a lower gate voltage which is more negative than −3V.

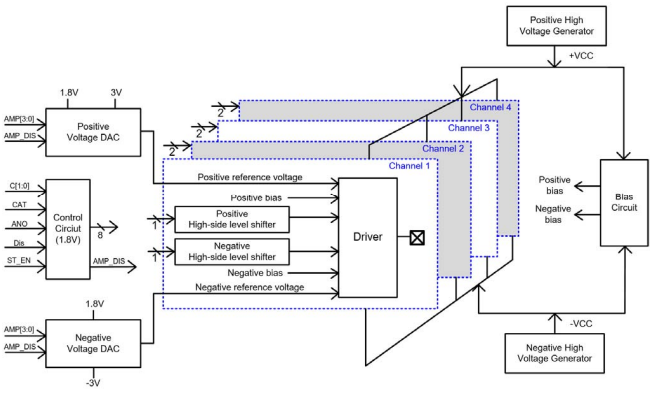


Fig. 3. Block diagram of the proposed stimulator with 4 channels.

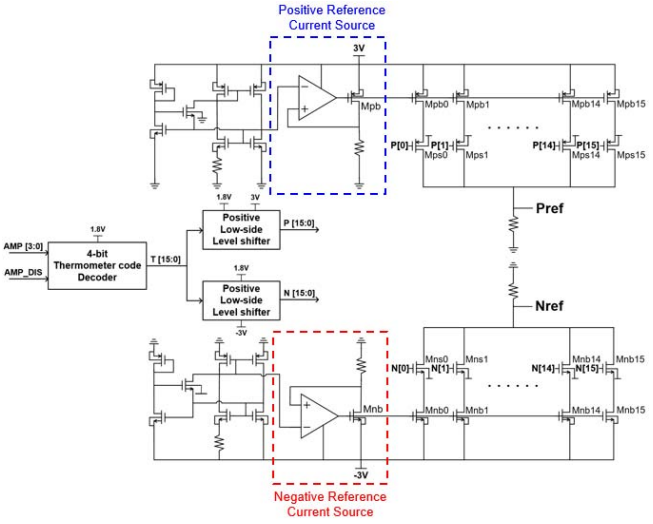


Fig. 4. Voltage reference DAC circuit including the positive voltage DAC (upper part) and the negative voltage DAC (lower part).

C. Stimulus Driver

There are four driver channels within the stimulator, where the driver circuit of one channel is shown in Fig. 5. The 12-V

HV PMOS and NMOS are used for 20-V high-voltage-tolerant design. Each driver comprises a pair of folded cascode Op-amps, switches (Mp1 and Mn1), power MOSFETs (Mp2 and Mn2), and stack transistors (Mp3 and Mn3). A feedback loop is built in the driver, and the ratio of feedback resistors is ten times of the reference voltages (Pref and Nref), that are connected to the input of Op-amps. Thus, the driver output voltage at the Vout node can be locked at the expected stimulus voltage.

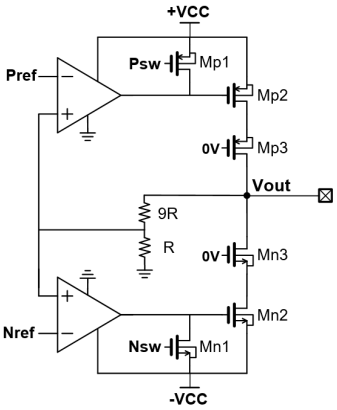
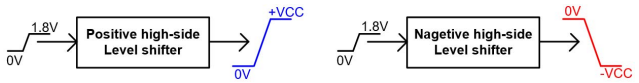


Fig. 5. Circuit implement of one-channel stimulus driver.



(a) (b)

Fig. 6. Control signals used in driver circuit control with (a) digital input 1.8V shifted to +VCC as logic high, and (b) digital input 1.8V shifted to –VCC as logic low.

Psw and Nsw are the input signals of driver those coming from control circuit. By passing through a positive high-side level shifter shown in Fig. 6(a), the voltage level of logic high shifts from 1.8V to +VCC while logic low remains 0V. On the contrary, a negative high-side level shifter reverses the logic state. It transfers logic high (1.8V) to logic low (–VCC), and 0V becomes logic high as shown in Fig. 6(b). When Psw of a specified channel is logic high, that implies this channel is selected for anodic stimulation. Mp1 is off due to gate voltage level equals to +VCC, thus the Pref at the input of Op-amp, Mp2, and resistors compose a complete LDO feedback loop. At the meantime, Nsw for cathodic stimulation is also logic high (CAT signal is logic low), which makes Mn1 on and Mn2 off because the gate of Mn2 is biased at –VCC. Therefore, break the loop of Nref at the input of Op-amp, Mn2, and feedback resistors. Cathodic stimulate operation is similar, but the logic states of Psw and Nsw are opposite to anodic stimulation. With the maximum output voltage of ±8V, the voltage difference between +VCC (–VCC) and Vout can be as large as 18V if the ±10V power supplies are given. To prevent device overstress, the Mp3 and Mn3 are stacked there and biased at 0V regardless of the positive or negative output. The drain voltage of Mp3 and Mn3 is changing either positive or negative, but with suitable HVPW/HVNW bias of 12-V devices, the driver can avoid p-n junction forward-leakage when the P-substrate is 0V. As aforementioned, all switches in DAC are turned off during discharge phase, and the Pref and Nref are biased at a voltage level of 0V to make sure that the Vout pad is grounded.

The four channels will not be enabled at the same time, in other words, biphasic pulse is delivered by one selected channel at a time period. For those channels that are not selected, Psw is logic low and Nsw is logic high (both ANO and CAT are logic low), which represents that the two power MOSFETs are off, and the driver circuit is in the high-Z state. Under high-Z circumstance, even if Vout of disable channels with some variation due to the stimulation voltage at the enabled neighborhood channel, driver devices still do not suffer from overstress issue due to Mp3 and Mn3.

III. Measurement Results

The chip microphotograph of the stimulator is shown in Fig. 7, which is fabricated in a 0.25-µm 2.5-V/5-V/12-V CMOS process. Adapting a wide range of loading impedance, the adjustable stimulus voltages of biphasic waveforms can be measured successfully in Fig. 8(a). In addition, the mismatching between cathodic/anodic output voltages is shown in Fig. 8(b), which is less than 2.5%. As the amplitude increases step by step, the output voltage remains linearity. Although the four channels cannot be chosen simultaneously, they can be programmed to change rapidly, as the function verified in Fig. 9. Considering the SoC integration with other circuit blocks together, the ±VCC power of the stimulator may not be so stable, thus power variation test is included. The fabricated chip can deliver a full-scale stimulus voltage of ±8V, as long as ±VCC larger than ±8.5V.

The performance of this work is summarized in Table I with comparisons to some related prior works [8]-[10].

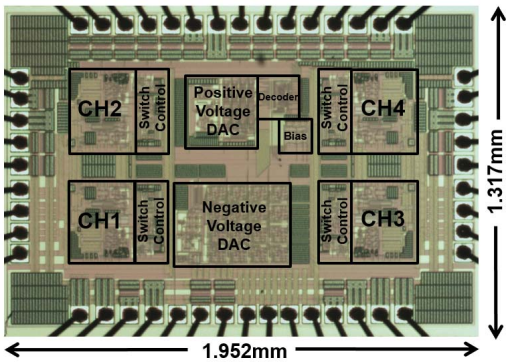
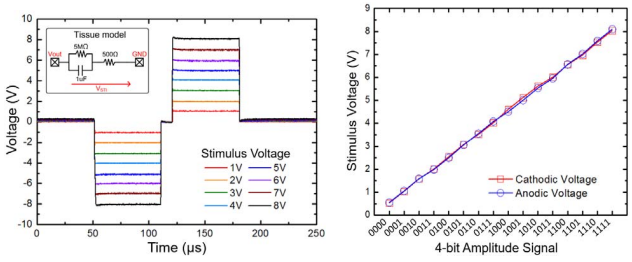


Fig. 7. Microphotograph of the 4-channel stimulator chip with a die size of 2.57mm^2, which was fabricted in a 0.25-µm 2.5-V/5-V/12-V CMOS process.



(a) (b)

Fig. 8. Output performance of stimulator. (a) Biphasic stimulus voltage under the load (Rs) of 500 ohm. (b) Comparison of voltage mismatch between cathodic/anodic voltage pulse at each output amplitude.

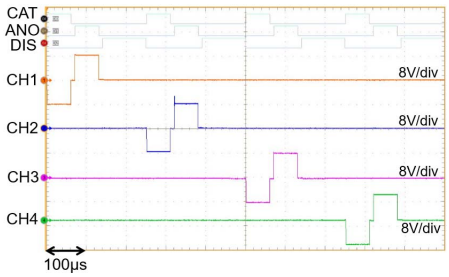


Fig. 9. Measured volatge waveforsms to demonstrate the changing opertaion among different output channels of the stimulator.

IV. Biomedical Applications

The in-vivo animal test with the proposed stimulator chip is shown in Fig. 10(a). The location of the plate electrodes onto the cochlear of a guinea pig is shown in Fig. 10(b), where the plate electrodes are placed on the surface of cochlear bone and round window. After deciding the stimulation channel and setting a proper stimulus voltage, the computer delivers continuous command to auditory brainstem response (ABR) system, and then the ABR system triggers the stimulator chip to generate biphasic stimulation pulses. Once the electrical stimulation is done, the action potentials are recorded by the ABR system. By observing the Wave IV of evoked ABR (EABR) waveforms [11], as shown in Fig. 11 with a stimulus voltage of ±4V, it can be proved that the proposed stimulator chip is as good as the commercial stimulus equipment for biomedical applications.

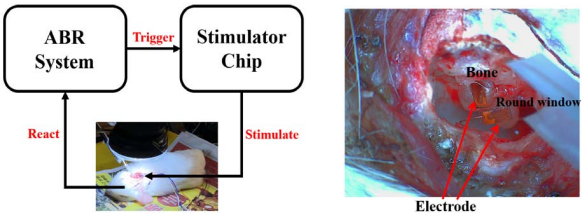


Fig. 10. (a) Experimental setup of in-vivo animal test with guinea pig. (b) The placement of plate electrodes on the cochlear of guinea pig.

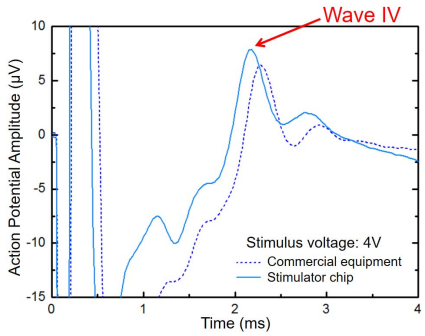


Fig. 11. The evoked Wave IV of EABR waveforms on guinea pig induced by the commercial stimulator and the proposed stimulator silicon chip.

V. Conclusion

A silicon chip for neuromodulation stimulation has been designed, fabricated, and verified successfully. Without device overstress issue or p-n junction breakdown problem under 20V compliance voltage, a maximum stimulus voltage of ±8V can be generated for biomedical applications with wide range of loading impedance. With flexible input control, tiny physical dimension, and low-power operation, the proposed stimulator chip can be integrated with other circuit blocks together into a SoC for implantable biomedical applications.

TABLE I. Performance Summary and Comparisons

	[8] 2011 MWSCAS	[9] 2017 TCAS II	[10] 2010 JSSC	This work
CMOS Technology	0.18-μm	0.5-μm	0.18-μm	0.25-μm
Voltage Compliance	3.3V	11.1V	24V	20V
Maximum Output	800pA	175nA	±10V	±8V (16mA)
Mismatch	<3%	2%	<2.9%	<2.5%
Chip Area (mm^2)	32	0.2	27.03	2.57
Animal Test	NA	NA	NA	*In-vivo*

Acknowledgment

This work was supported in part by the "Center for Neuromodulation Medical Electronics Systems" from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan. This work was also supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 106-2221-E-009-167-MY2 and MOST 106-3114-8-009-001. The chip fabrication was supported by National Chip Implementation Center (CIC), Taiwan.

References

[1] M. Sivaprakasam, W. Liu, G. Wang, J. Weiland, and M. Humayum, "Architecture tradeoffs in high-density microstimulators for retinal prosthesis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2629-2641, Dec. 2005.

[2] G. Deli *et al.*, "Comparison of the efficacy of unipolar and bipolar electrode configuration during subthalamic deep brain stimulation," *Parkinsonism Relat. Disorder*, vol. 17, pp. 50-54, Jan. 2011.

[3] S. Little *et al.*, "Adaptive deep brain stimulation in advanced Parkinson disease," *Ann. Neurol.*, vol. 74, pp. 449-457, Sep. 2013.

[4] G. A. Vilos and C. Rajakumar, "Electrosurgical generators and monopolar and bipolar electrosurgery," *J. Minim. Invasive Gynecol.*, vol. 20, pp. 279-287, May 2013.

[5] S. F. Cogan, "Neural stimulation and recording electrodes," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 275-309, Apr. 2008.

[6] C.-Y. Wu *et al.*, "Design considerations and clinical applications of closed-loop neural disorder control SoCs," *in Proc. IEEE Conference on Design Automation*, 2017, pp. 295-298.

[7] G. I. Radulov, P. J. Quinn, P. C. W. van Beek, J. A. Hegt, and A. H. M. van Roermund, "A binary-to-thermometer decoder with built-in redundancy for improved DAC yield," *in Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 1414-1417.

[8] B. Goldstein, K. Choe, F. J. Sigworth, and E. Culurciello, "A four-channel integrated patch-clamp amplifier with current-clamp capability," *in Proc. IEEE 54th Int. Midwest Symp. Circuits Syst.*, 2011, pp. 1-4.

[9] S. Dai and J. K. Rosenstein, "A 15-V bidirectional current clamp circuit for integrated patch clamp electrophysiology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 11, pp. 1287-1291, Nov. 2017

[10] K. Chen *et al.*, "An integrated 256-channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 1946-1956 Sep. 2010.

[11] S. Gallego, E. Truy, A. Morgon, and L. Collet, "EABRs and surface potentials with a transcutaneous mutielectrode cochlear implant, " *Acta Otolaryngologica*, vol. 117, no. 2, pp. 164-168, Mar. 1997.