Power-Rail ESD Clamp Circuit with Polysilicon Diodes Against False Trigger During Fast Power-on Events

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Abstract - A new power-rail ESD clamp circuit with both timing and voltage-level detection is proposed against false trigger events. A *RC* stage is used for dv/dt detection and a diode string is used to detect the over-stress voltage level during ESD events. By using fully isolated polysilicon diodes, the standby leakage current of the proposed power-rail ESD clamp can be effectively reduced.

I. Introduction

In advanced CMOS technology, the electrostatic discharge (ESD) protection has become one of the important reliability issues of IC products. To sustain good ESD robustness, the *RC*-based power-rail ESD clamp circuit has been popularly used in IC industry [1]. A typical *RC*-based power-rail ESD clamp circuit is shown in Fig. 1(a). During the ESD event with a positive ESD voltage applied to V_{DD} node, the *RC*-delay technique keeps the voltage of V_{rc} at a low voltage level while V_{DD} rise up, and then turns on the main ESD clamping MOSFET (M_{ESD}) through an inverter to discharge ESD current from V_{DD} to V_{SS} (ground). Under the normal power-on condition (a slow rise time of milliseconds), the *RC* trigger circuit is unable to turn on the M_{ESD}. But with the hot plug-in condition, the rise time of V_{DD} voltage may be fast enough to cause some mis-triggering on this ESD clamping M_{ESD}. When this mis-triggering event occurs, the M_{ESD} with bigger device dimension will cause a large leakage which may affect the function of internal circuits or circuit reliability. Fig. 1(b) shows the false-triggering event on the *RC*-based power-rail ESD clamp circuit during a fast power-on operation with a rise time of 10 ns. To overcome the fast power-on issue, several solutions had been reported to improve the traditional design [2]–[4]. The goal is to trigger the ESD clamp only during a fast transient (like the ESD events) but only if the stress exceeds the specified over-voltage level. The diode string (with multiple diodes in stacked configuration) is the typical circuit method used to detect the over-stress voltage level during ESD events. However, the standby leakage effect along the diode strings in the ESD detection circuit should be carefully considered [5]–[7]. Standby leakage is due to the parasitic Darlington and its current amplification within the diode string under high temperature.

In this work, a new power-rail ESD clamp circuit with better false triggering immunity is proposed and verified in a 0.18-μm 1.8-V CMOS process.

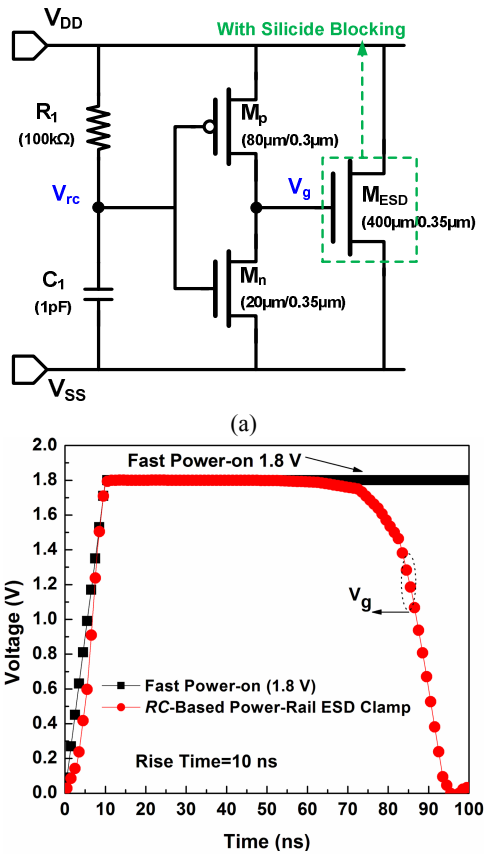


Figure 1: (a) Traditional *RC*-based power-rail ESD clamp circuit and (b) the simulated voltage waveform on the node V_g during a fast power-on condition with a rise time of 10ns and V_{DD} of 1.8 V.

II. New ESD Power Clamp

A. Circuit Design

The power-rail ESD clamp circuit should be designed not only for the desired specification, but also with the simplified circuit structure to save area.

A power-rail ESD clamp circuit with double detection mechanisms to overcome the false trigger issue is proposed and shown in Fig. 2. In addition to the *RC* stage, a diode string stage made of polysilicon diodes as voltage detector is added to the trigger circuit. The selected number of diodes is dependent on the normal operating voltage of V_{DD} (typically four stacked diodes for 1.8-V application). Under the normal circuit operating conditions, the operating voltage on V_{DD} must be lower than the turn-on voltage of the diode string, even at high temperature. A *RC* time constant of 100 ns is selected with a resistor (R_1) of 100 kΩ and a capacitor (C_1) of 1 pF. The stacked PMOS M_{p1} and M_{p2} are used to control the gate of M_{ESD} to ensure that it can be triggered on quickly under ESD stress condition. Finally, M_{ESD} is designed with 400 μm width and using silicide blocking to sustain bipolar operation under higher voltage conditions, such as 2-kV HBM or 5A CDM.

In the simulation of ESD-like waveform, the rise time of 10 ns and the pulse width of 100 ns are selected as a TLP-like event. The drain-substrate junction breakdown voltage of NMOS in this process is about 8 V. The voltage of this TLP-like waveform is selected as 5 V, which is used to investigate the triggering operation of the ESD detection circuit before the bipolar activation of the M_{ESD}. On the contrary, the normal power-on voltage waveform has a rise time in the order of millisecond (ms) and a lower voltage (1.8-V). For fast power-on operation due to hot plug-in specific applications, a rise time of 10ns is selected. The simulated voltages on each node of the proposed circuit during transient ESD pulse are shown in Fig. 3(a). Due to the *RC* delay keeping the voltage low on the node V_{rc}, the M_{p1} is turned on. The high voltage level of the TLP-like pulse will also trigger the diode string keeping the V_{rd} node lower than V_{DD}, which results in the turn-on of M_{p2}. With both M_{p1} and M_{p2} triggered, the node V_g will be biased up switching on the M_{ESD}. The simulation results of normal power-on condition are shown in Fig. 3(b). Since M_{p1} and M_{p2} are kept in off state, the voltage level on the node V_g is kept at 0 V and M_{ESD} remains off. The simulation results of the proposed circuit under fast power-on condition at 25°C are shown in Fig. 4(a). The fast transient waveform will turn on the M_{p1} device due to the *RC* network activation, but under the 1.8-V power supply level, it will not activate the diode string made of four stacked diodes keeping the M_{p2} off. Therefore, the voltage level on the node V_g remains at 0 V, so keeping the M_{ESD} switching in off state. The transient leakage current (I_{Leak}) during the rise time is due to the coupling effect through the parasitic capacitance of M_{ESD}. The influence of the number of diodes in the diode string stage on the voltage detection level is shown in the Fig. 4(b). By changing the number of stacked diodes in the ESD detection circuit, the minimum starting voltage of ESD clamp circuit can be adjusted to meet the applications of different supply voltages against false trigger during fast power-on events.

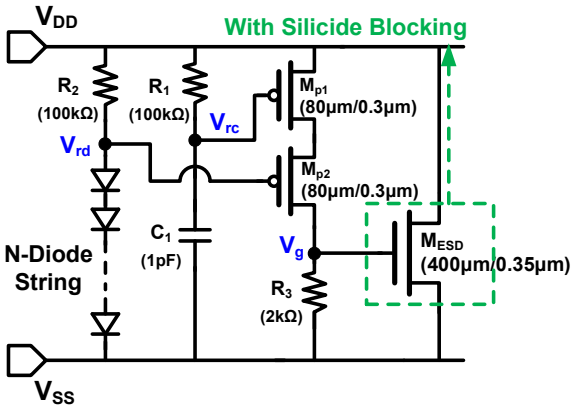
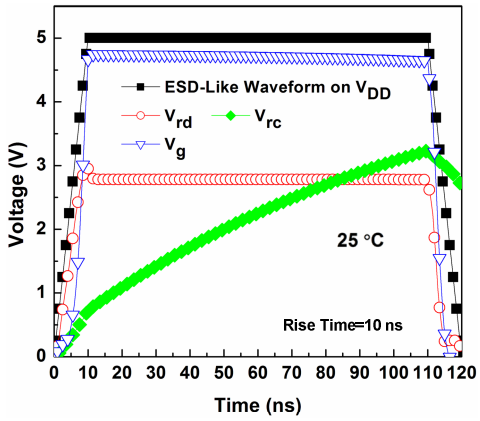
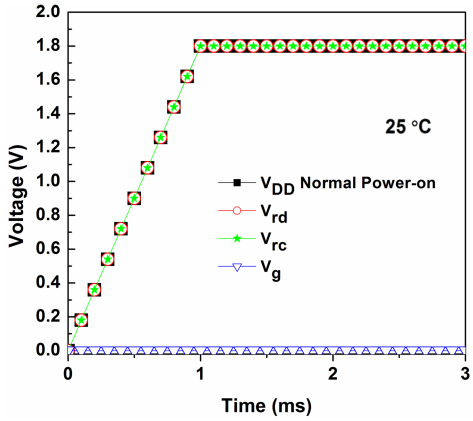


Figure 2: Proposed power-rail ESD clamp circuit.

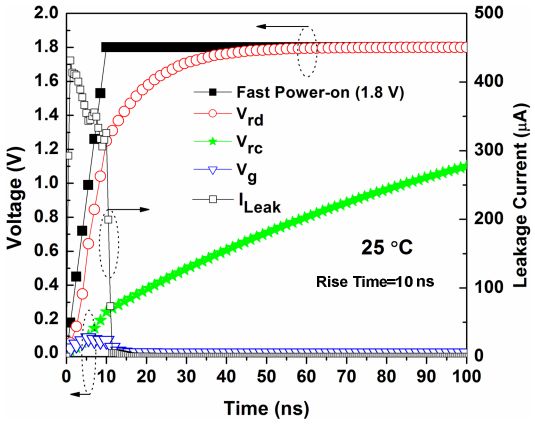


(a)

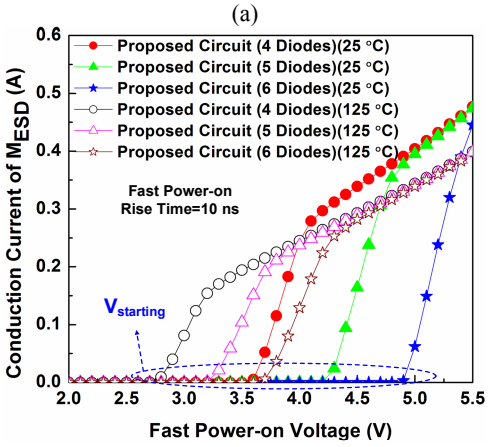


(b)

Figure 3: Simulation results of the proposed circuit (a) during ESD pulse condition and (b) under normal power-on condition.



(a)

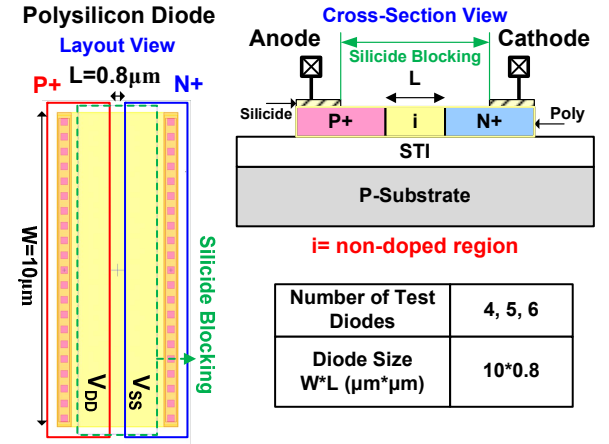


(b)

Figure 4: Simulation results of the proposed circuit (a) under fast power-on condition and (b) to investigate the $V_{starting}$ with different number of diodes in different temperature.

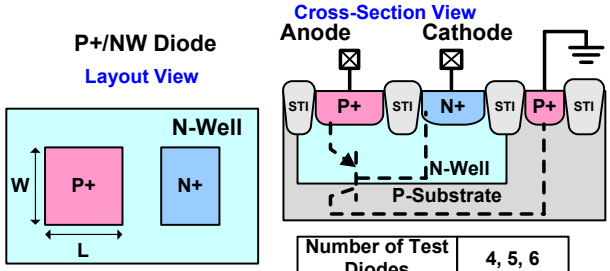
B. Diode String Structure

A diode string connected to V_{DD} often suffers standby leakage issue, especially the traditional P+/NW diode string in bulk CMOS technologies [8], [9]. The traditional P+/NW diode has a parasitic vertical P-N-P BJT structure, which will increase the overall leakage of a diode string. To minimize the standby leakage current of the proposed power-rail ESD clamp circuit, two types of diode structures are studied in this work (i.e. traditional P+/NW diode and polysilicon diode). Fig. 5 shows the device structures and layouts of a traditional P+/NW diode and a polysilicon diode. The polysilicon diode is realized by the poly layer with both P+/N+ doping areas. The electrical isolation between the anode and cathode of the polysilicon diode is made of the silicide blocking mask. To insure that the node V_{rd} will be charged up to the normal power-on voltage level (1.8-V) during power-up, the diode string is designed with four stacked diodes. To investigate the influence of diode dimension, the layout size of each diode in the diode string is tested with anodes of 2*2 and 10*10 μm^2 for the P+/NW diodes and a width of 10 μm for the polysilicon diodes. Then in order to verify the voltage detection function ($V_{starting}$), diode strings with four-, five-, and six-stacked diodes are also implemented in the silicon testchip. The influence of the number of diodes in the diode string stage made of P+/NW diode is shown in the Fig. 6. Surprisingly, when adjusting the number of diodes, the $V_{starting}$ among the proposed circuits with P+/NW diode string has no significant difference.



Number of Test Diodes	4, 5, 6
Diode Size W*L (μm*μm)	10*0.8

(a)



Number of Test Diodes	4, 5, 6
Diode Size W*L (μm*μm)	2*2, 10*10

(b)

Figure 5: Cross-section and layout view of (a) polysilicon diode and (b) traditional P+/NW diode.

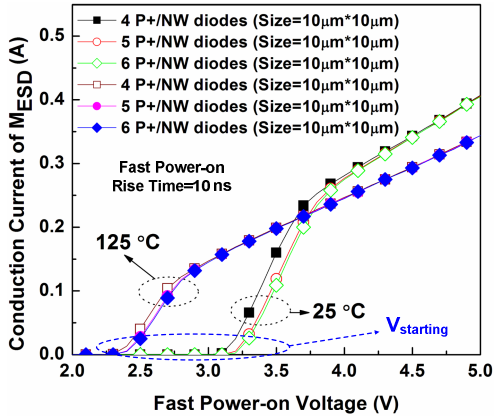


Figure 6: Simulation results of the proposed circuit to investigate the $V_{starting}$ with different number of P+/NW diodes in different temperature.

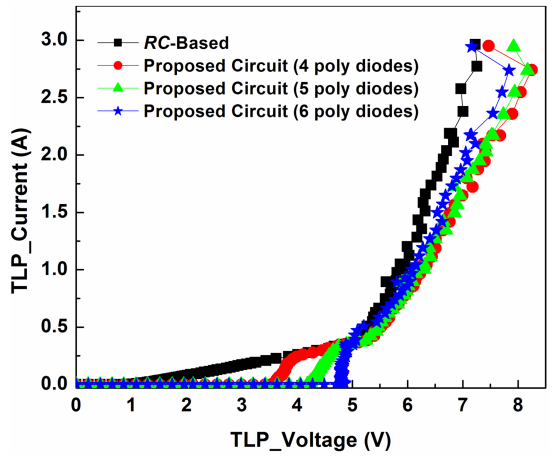
III. Experimental Results

A. TLP Measurement

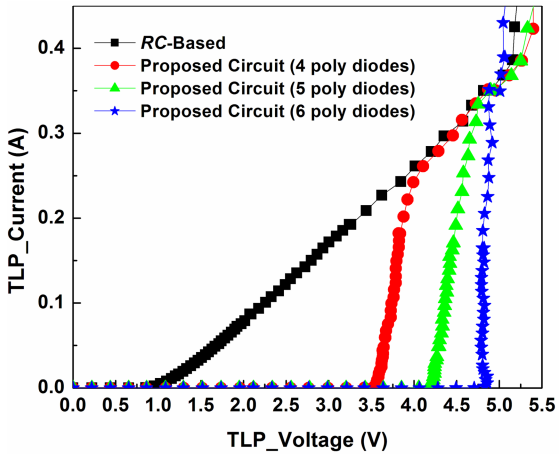
To investigate the turn-on behavior and the I-V characteristics of the circuits under HBM ESD events, a transmission-line-pulsing (TLP) generator is used to provide an ESD-like waveform with pulse width of 100 ns and rise time of 10 ns. The TLP-measured I-V curves of all test circuits are shown in Figs. 7 and 8. The minimum starting voltage ($V_{starting}$) was defined to be the voltage at which the device can conduct 20-mA current. Thus, the $V_{starting}$ of the *RC*-based ESD clamp circuit (Fig. 1(a)) is only 1.2 V, but for the proposed power-rail ESD clamp circuit (Fig. 2) the $V_{starting}$ with polysilicon diodes string is increased proportionally with the number of stacked diodes: up to 3.5, 4.2, and 4.8V for the four-, five-, and six-stacked polysilicon diodes respectively. The $V_{starting}$ among the proposed circuits with P+/NW diode string has no significant difference, as shown in Fig. 8(b). It is due to the parasitic leakage path through the vertical P-N-P BJT in the P+/NW diode string. Obviously, the $V_{starting}$ of *RC*-based power-rail ESD clamp circuit is lower than normal operating voltage (1.8-V), which has a high risk of the false triggering under fast power-on condition. The ESD robustness is mainly dependent on the dimension of M_{ESD}. Here a single M_{ESD} size is used on the testchip, therefore all every structures are demonstrating about the same second breakdown current (I_{t2}). All of these measurement results are summarized in Table 1, including the HBM ESD level and clamping voltage under 1-A TLP current.

B. Fast Power-on Test

For the fast power-on events due to the hot plug-in applications with the rise time in the nanosecond range that is close to the typical timing of HBM ESD events and RC detection stage only won't be able to differentiate power-on from ESD event. To verify the turn-on behavior of the ESD clamp circuits under the fast power-on event, a transient pulse (with pulse width of 300 ns, rise time of 10 ns, and voltage level of 1.8-V) was applied to the V_{DD} node of the test circuits. As shown in Fig. 9, the V_{DD} voltage waveform on *RC*-based ESD clamp circuit is clamped at 1.2 V for about 120 ns. This is due to the *RC* network triggering circuit and its 100 ns time constant. As expected, the V_{DD} voltage waveform on the proposed ESD clamp circuit (Fig. 2) with 4 stacked polysilicon diodes doesn't show any clamping or waveform disturbance, because the $V_{starting}$ of the proposed circuit is higher than the V_{DD} operating voltage of 1.8-V. Therefore, the proposed power-rail ESD clamp circuit is successfully verified for false triggering immunity under fast power-on condition.



(a)



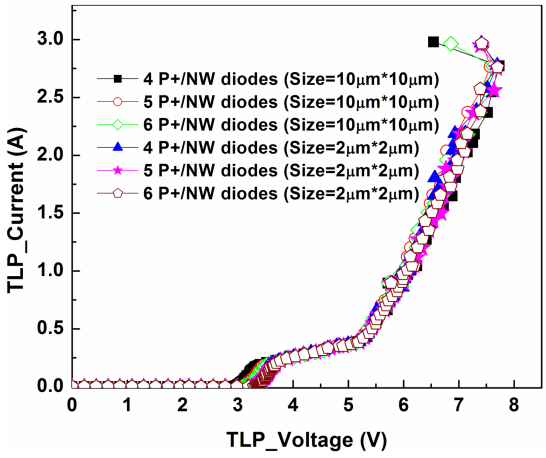
(b)

Figure 7: TLP-measured I-V characteristics of (a) the *RC*-based power-rail ESD clamp circuit and the proposed circuit with polysilicon diodes, and (b) a zoom-in illustration.

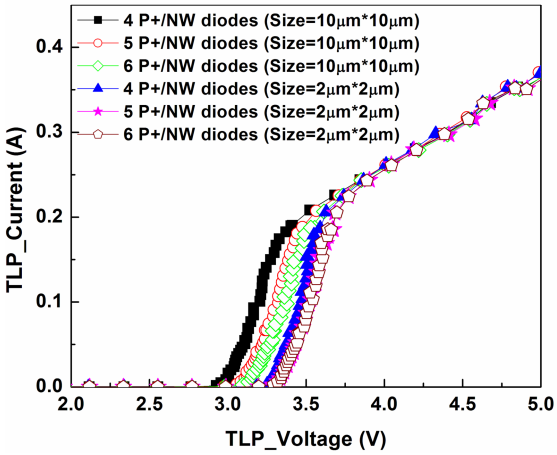
C. Standby Leakage

To check the trigger circuits influence on standby leakage, the dc I-V characteristics of the test circuits were measured (Fig. 10) at high temperature (125°C) under 1.8-V V_{DD} bias. The measured results, the leakage currents of the proposed power-rail ESD clamp circuit with polysilicon diode (4, 5, or 6 stacked diodes) are all below 1μA. Despite shrinking the layout size of the P+/NW diode down to 2*2 μm^2, the leakage current of the power-rail ESD clamp circuit with P+/NW diode is still higher than the proposed clamp with polysilicon diodes and even above 1μA in case of the 4 diodes string. Thus, the diode string realized with polysilicon diode is more suitable for the

proposed power-rail ESD clamp circuit with false triggering immunity under fast power-on event.



(a)



(b)

Figure 8: TLP-measured I-V characteristics of (a) the proposed circuit with P+/NW diodes, and (b) a zoom-in illustration.

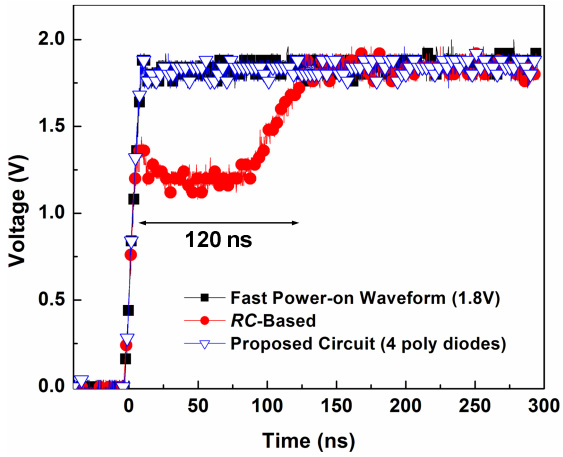


Figure 9: Measured transient voltage waveforms under fast power-on event (1.8-V V_{DD} level with 10ns rise time) for two power-rail ESD clamp circuits to verify their false triggering immunity.

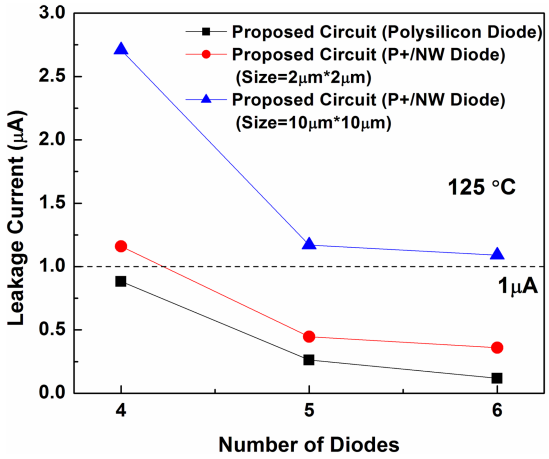


Figure 10: Measured DC leakage current among the proposed power-rail ESD clamp circuits (with polysilicon diode or P+/NW diode) at 125°C under 1.8-V bias.

D. ESD Robustness

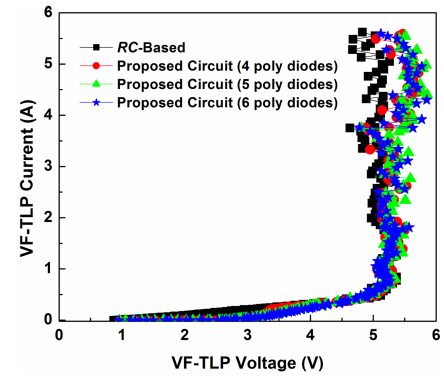
The component-level human-body-model (HBM) ESD robustness of the fabricated ESD circuits has been tested. The failure criterion is defined as the *I–V* characteristics of the device shifting more than 10 % from its initial curve. The HBM ESD robustness of each power-rail ESD clamp circuit is all the same at 4.8 kV (Table 1), as expected since the same device dimension is used for M_{ESD}.

E. Very-fast TLP Measurement

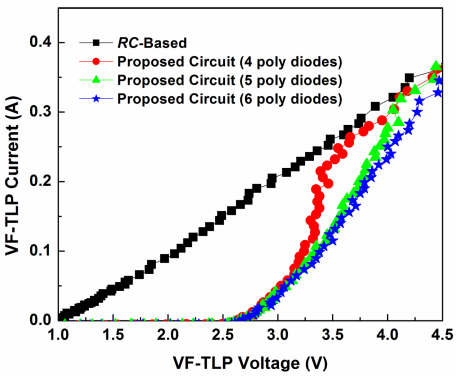
The power-rail ESD clamp circuit is also needed to discharge the ESD current of charged-device-model (CDM) event. To characterize the CDM robustness of the ESD protection circuits, a very fast TLP (VF-TLP) system with pulse width of 5 ns and rise time of 200 ps has been used to verify their performance. Figs. 11 and 12 show the comparison of VF-TLP I-V curves among all test circuits. The second breakdown current of VF-TLP among all the test circuits is about 5.5 A, which means that the proposed power-rail ESD clamp circuit can sustain good CDM level. Then, as shown in Figs. 11(b) and 12(b), the starting voltage of the proposed power-rail ESD clamp circuit under VF-TLP stress is not much influenced by the number of stacked diodes. The only influence on the starting voltages is the size of the diode. One explanation for this phenomenon is that the diode acts as a capacitor during very fast rising pulse: The current that flows through the resistor R_2 is dependent on C*(dv/dt). With four-, five-, and six-stacked diodes, the capacitance seen at the node V_{rd} has minor influence (1/4, 1/5 and 1/6 capacitor reduction respectively).

Table 1: Measurement results of *RC*-based power-rail ESD clamp circuit and the proposed power-rail ESD clamp circuits

Circuits under test	$V_{starting}$ (V)	V_{clamp} (V) (@I_{TLP}=1A)	I_{t2} (A)	I_{Leak} (μA)	HBM (kV)
RC-Based Circuit (Fig. 1a)	1.2	5.9	2.9	0.01	4.8
Proposed Circuit (4 poly diodes)	3.5	6.2	2.9	0.8	4.8
Proposed Circuit (5 poly diodes)	4.2	6.2	2.9	0.3	4.8
Proposed Circuit (6 poly diodes)	4.8	6.1	2.9	0.1	4.8
Proposed Circuit (4 P+/NW diodes) (10μm*10μm)	3.07	6.1	2.9	2.7	4.8
Proposed Circuit (5 P+/NW diodes) (10μm*10μm)	3.12	6.0	2.9	1.2	4.8
Proposed Circuit (6 P+/NW diodes) (10μm*10μm)	3.16	6.1	2.9	1.1	4.8
Proposed Circuit (4 P+/NW diodes) (2μm*2μm)	3.29	6.1	2.9	1.2	4.8
Proposed Circuit (5 P+/NW diodes) (2μm*2μm)	3.35	6.1	2.9	0.4	4.8
Proposed Circuit (6 P+/NW diodes) (2μm*2μm)	3.36	6.1	2.9	0.3	4.8

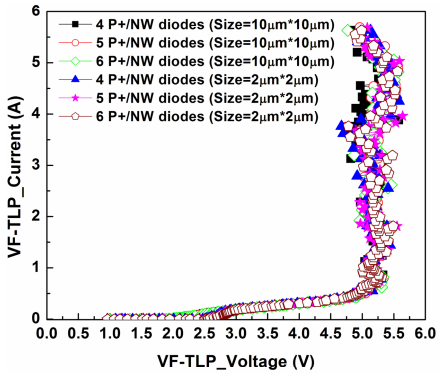


(a)

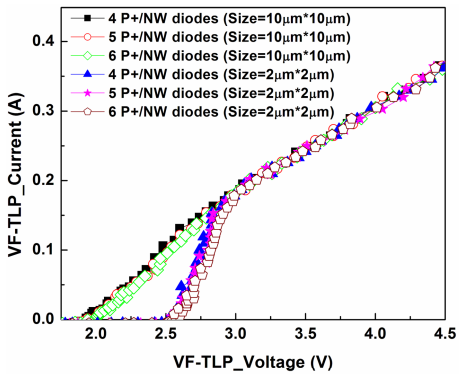


(b)

Figure 11: VF-TLP-measured I-V characteristics of (a) the *RC*-based power-rail ESD clamp circuit and the proposed circuit with polysilicon diodes, and (b) a zoom-in illustration.



(a)



(b)

Figure 12: VF-TLP-measured I-V characteristics of (a) the proposed circuit with P+/NW diodes, and (b) a zoom-in illustration.

So changing the size of the diode has a clear influence on the capacitance to influence the starting voltage. In summary, using a diode string as the voltage detector under CDM ESD events doesn't disturb much the power clamp current dissipation capability and still allow V_{t1} reduction to V_h. However, the starting voltage will not change by adjusting the number of diodes, such as four-, five-, and six-stacked diodes.

IV. Conclusion

By using both the *RC* delay mechanism to detect the fast transient and the stacked polysilicon diodes to detect the specified over-stress voltage level, the new proposed power-rail ESD clamp circuit can provide effective ESD protection and also has high immunity against false trigger during fast power-on conditions. In addition, using polysilicon diodes can efficiently reduce the standby leakage current in the power-rail ESD clamp circuit compared to bulk P+/NW diodes, even in a high temperature of 125°C.

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