Study on Latchup Path between HV-LDMOS and LV-CMOS in a 0.16-µm 30-V/1.8-V BCD Technology

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Abstract - The latchup path between high-voltage (HV) PMOS and low-voltage (LV) PMOS in a 0.16-µm 30-V/1.8-V bipolar-CMOS-DMOS (BCD) technology is studied. From the experiment results on silicon chip, this path can be easily induced into latchup state during the current-trigger latchup test. Therefore, the related layout rules should be carefully specified to avoid such HV-to-LV cross-domain latchup issue.

I. Introduction

When more complicated implementations of CMOS integrated circuits (ICs), such as mixed-signal, multiple power supplies, RF, system-on-chip, are integrated together, those CMOS devices will suffer considerable noises coming from both internal and external of CMOS ICs. Robust reliability design is strongly needed for CMOS ICs used in the harsh operating environments. Latchup is one of the important reliability issue in CMOS IC products, especially in the high-voltage (HV) applications [1], [2]. Because of the high circuit-operating voltage and structure complexity of HV devices, HV CMOS ICs would be seriously damaged by the latchup-generated heat if latchup is induced by the external glitches or inductive load. To eliminate the occurrence of latchup, many techniques had been reported, including process optimization, modified layout structure, or even circuit design of active guard ring [3]–[8].

The methods and test procedures to investigate the latchup immunity of IC product had been specified in the Joint Electron Device Engineering Council (JEDEC) standards [9]. The latchup immunity level for the current-trigger latchup test in the up-to-dated standard (JESD78E) has been specified to be greater than 100 mA.

With the integration of both HV and low-voltage (LV) devices in the same chip, the voltage levels of HV domain are often significantly greater than the voltage levels of LV domain. Some unpredictable latchup failures or ESD protection issues would happen around the interfaces between different power domains, as those reported in [10]–[13]. Though cross-domain latchup issue did not occur because of the multi-layer structures of HV devices in [13], such latchup or latchup-like issue may still possibly happen when a process with simplified HV device structures is used.

In this work, the cross-domain latchup path between HV and LV transistors has been investigated in a 0.16-µm 30-V/1.8-V bipolar-CMOS-DMOS (BCD) technology. In order to verify the holding voltage of latchup path, the dc curve tracer (Tek370B) and 1000-ns transmission-line-pulsing (TLP) system are used [14]. The characteristics of latchup path between the HV and LV devices are further verified through the current-trigger latchup test. A silicon chip with split device conditions and the trigger node was drawn and fabricated.

II. Test Structures

Latchup path traditionally exists between the PMOS (connected to V_{DD} or V_{CC}) and the NMOS (connected to V_{SS} or GND), when these two devices are close together to each other in the chip, as illustrated in Fig. 1. Therefore, some layout rules to prevent latchup between PMOS and NMOS had been specified and provided by foundry for a given CMOS process.

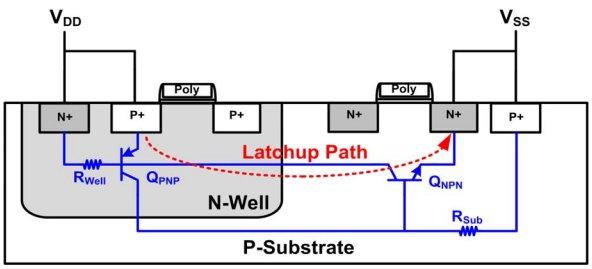


Figure 1: Traditional latchup path between PMOS and NMOS transistors in a CMOS technology.

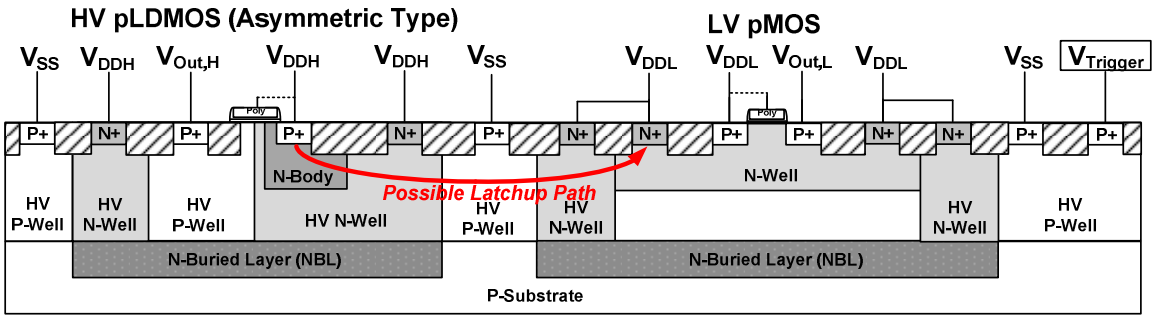


Figure 2: Test structure A with 30-V asymmetric pLDMOS and 1.8-V pMOS in the HV BCD technology, where the possible latchup path exists from the source of HV pLDMOS (connected to V_{DDH}) to the n-well of LV pMOS (connected to V_{DDL}).

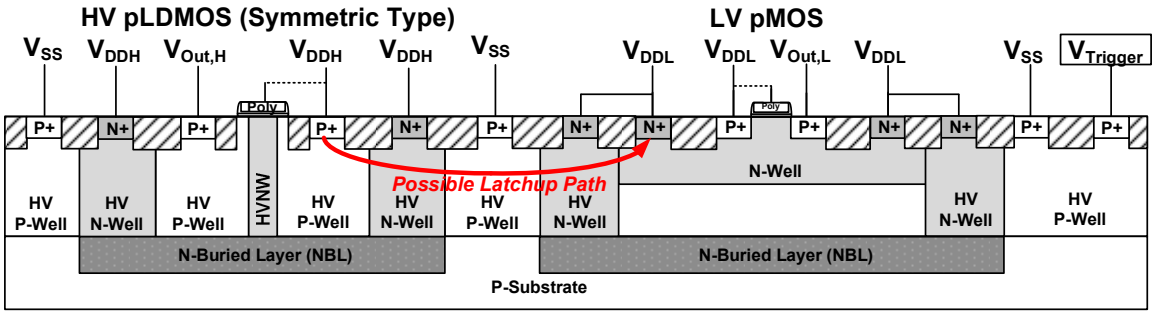


Figure 3: Test structure B with 30-V symmetric pLDMOS and 1.8-V pMOS in the HV BCD technology, where the possible latchup path exists from the source of HV pLDMOS (connected to V_{DDH}) to the n-well of LV pMOS (connected to V_{DDL}).

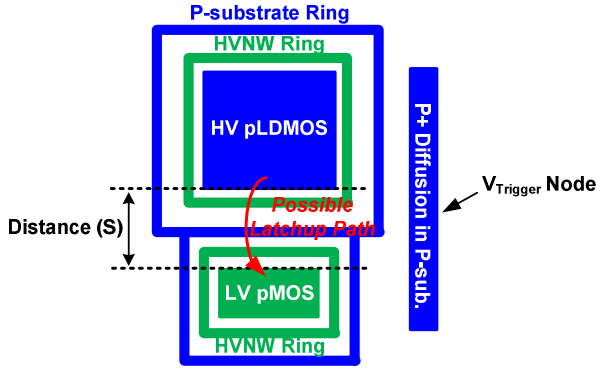


Figure 4: Simplified layout top view to show the possible latchup path between HV pLDMOS and LV pMOS.

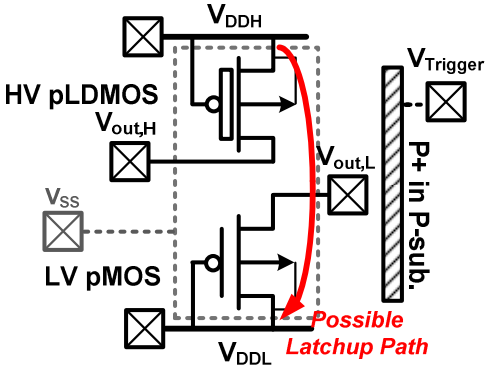


Figure 5: Simplified circuit scheme to show the possible latchup path between HV pLDMOS and LV pMOS.

However, there was no design rule specified for the possible latchup path that parasitically exists between the HV PMOS (connected to V_{DDH} or V_{CC}) and the N-Well of LV PMOS (connected to V_{DDL}). The test structures studied in this work are fabricated in a 0.16-μm 30-V/1.8-V BCD technology with two different HV device structures, including the asymmetric and symmetric 30-V pLDMOS transistors. Fig. 2 shows the test structure A implemented with 30-V asymmetric pLDMOS and 1.8-V pMOS transistors. According to the foundry-provided layout rules, the LV pMOS is surrounded by HV n-well (HVNW) and N-buried layer (NBL) for the isolation, which can reduce the substrate noise and separate the p-well (PW) bias of LV domain from the common p-substrate.

The cross-domain latchup path may possibly exist from the V_{DDH}-connected source of HV pLDMOS, through HV n-body, HVNW, HV p-well (HVPW), and p-substrate, to the V_{DDL}-connected n-well (NW) pickup of LV pMOS. Test structure B is implemented with 30-V symmetric pLDMOS and 1.8-V pMOS transistors, as drawn in Fig. 3. Compared with the asymmetric pLDMOS, the source side of symmetric one is composed of p-type diffusion (p+) and HVPW.

The simplified layout top view of the test structure with HV pLDMOS and LV pMOS is drawn in Fig. 4, where the $V_{Trigger}$ node with additional p+ diffusion added in p-substrate region will be used in the current-trigger latchup test. The distance (S) of the possible latchup path is 20 μm in the silicon chip.

The simplified circuit scheme to show the possible latchup path in these test structures is illustrated in Fig. 5, where the channels of both devices are kept in off state by gate-source short circuit to study the effect of layout structure on latchup. The HV and LV devices are drawn with channel widths of 400 μm and 30 μm, respectively.

III. Experimental Results

A. DC I–V Characteristics

To investigate the latchup characteristics of the test structures, the latchup dc I–V curves are measured by dc curve tracer (Tek370B) at room temperature (25 °C). Unfortunately, all the test structures were directly burned out before entering their snapback state in this dc measurement. The curve tracer might damage the device under test (DUT) because of the high electric power generated during the long measurement duration.

B. 1000-ns TLP I–V Characteristics

To avoid electrical overstress (EOS) events and to successfully detect the fired latchup state of the test structures, long-pulse TLP system is exploited. As reported in [14], TLP system with long pulse width can help to judge the holding voltage of DUT, which is sometimes regarded as reference data to latchup sensitivity. Accordingly, the latchup I–V curves of the test structures are measured by TLP system with different pulse widths. Fig. 6 shows the 1000-ns TLP-measured I–V curves of test structures from V_{DDH} to V_{DDL}, with V_{SS} grounded. The test structures A and B both entered their own snapback state with holding voltage of ~15 V. Furthermore, Fig. 7 shows the TLP-measured holding voltages of test structures with different pulse widths of 100, 200, 500, and 1000 ns, respectively.

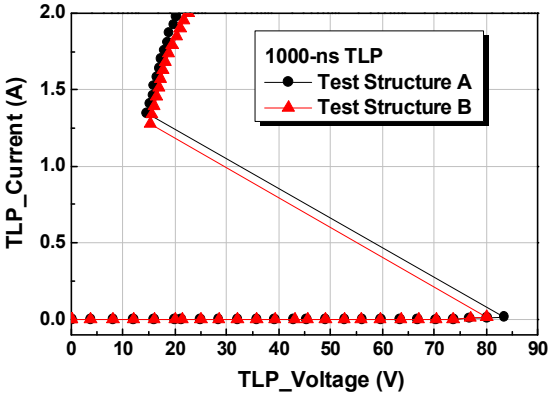


Figure 6: I–V characteristics of test structures A and B, measured by 1000-ns TLP system.

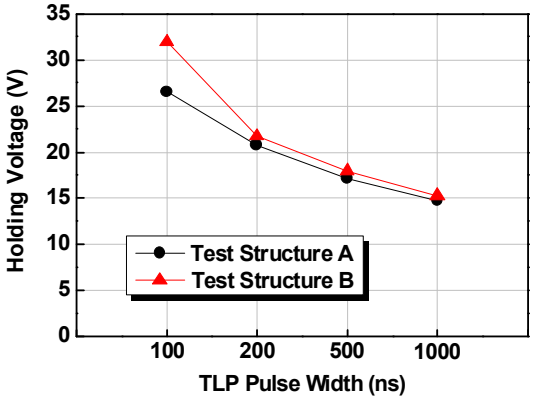


Figure 7: TLP-measured holding voltages of test structures with different pulse widths of 100, 200, 500, and 1000 ns, respectively.

The measured holding voltages gradually decreased as the pulse width increased from 100 to 1000 ns. It implies that the holding voltage of these test structures would be much lower under dc measurement, whereas latchup is a reliability issue with the time duration longer than milliseconds. With a lower holding voltage, the latchup path would be easily triggered on by the external injected noise pulses.

C. Current-Trigger Latchup Test

Since latchup state of these test structures can be detected from the 1000-ns TLP measurement results, current-trigger latchup test specified in the JEDEC standard (JESD78E) is used to further verify their latchup immunity. Fig. 8 shows the measurement setup of JEDEC latchup test applied to the test structures, with a HV dc supply at V_{DDH}, a LV dc supply at V_{DDL}, a current pulse generator applied to the $V_{Trigger}$ node, and an oscilloscope to monitor the waveforms at V_{DDH}, V_{DDL}, and $V_{Trigger}$ nodes. The trigger current pulse with a pulse width of 10 ms injected at $V_{Trigger}$ node is to simulate a transient noise penetrating into the p-substrate around the HV and LV devices to induce latchup.

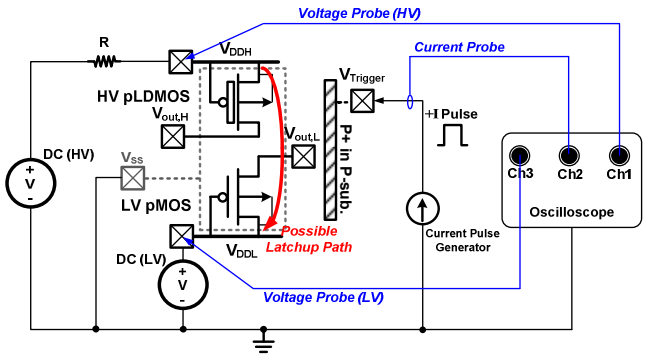


Figure 8: Latchup measurement with the positive current pulse applied at $V_{Trigger}$ node.

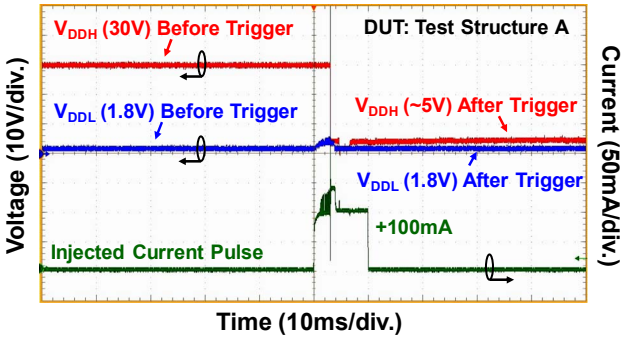


Figure 9: Measured time-domain voltage and current waveforms on the test structure A, with V_{DDH} of 30 V and V_{DDL} of 1.8 V.

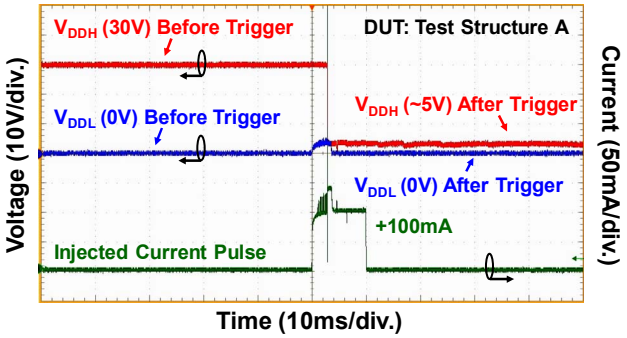


Figure 10: Measured time-domain voltage and current waveforms on the test structure A, with V_{DDH} of 30 V and V_{DDL} of 0 V.

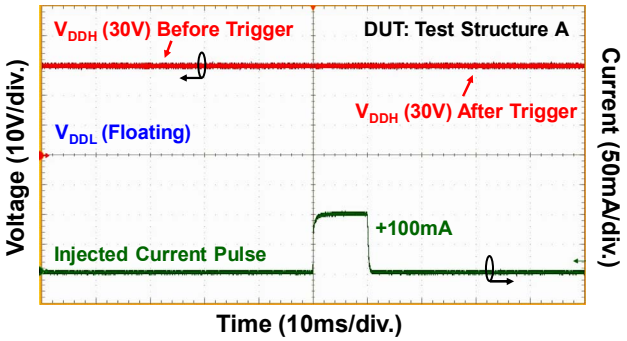


Figure 11: Measured time-domain voltage and current waveforms on the test structure A, with V_{DDH} of 30 V and V_{DDL} floating.

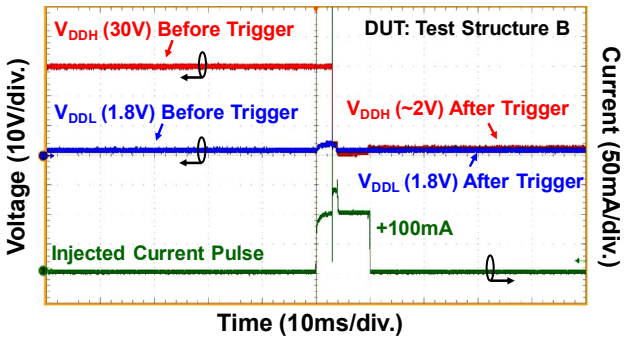


Figure 12: Measured time-domain voltage and current waveforms on the test structure B, with V_{DDH} of 30 V and V_{DDL} of 1.8 V.

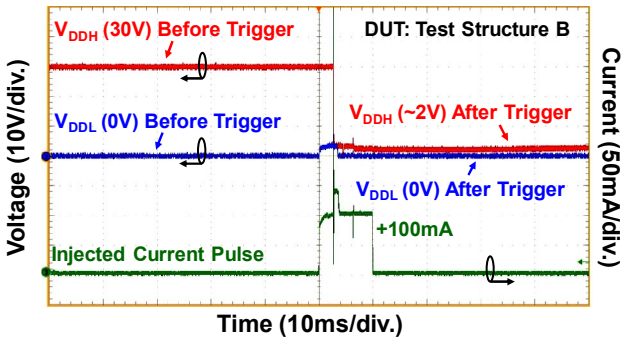


Figure 13: Measured time-domain voltage and current waveforms on the test structure B, with V_{DDH} of 30 V and V_{DDL} of 0 V.

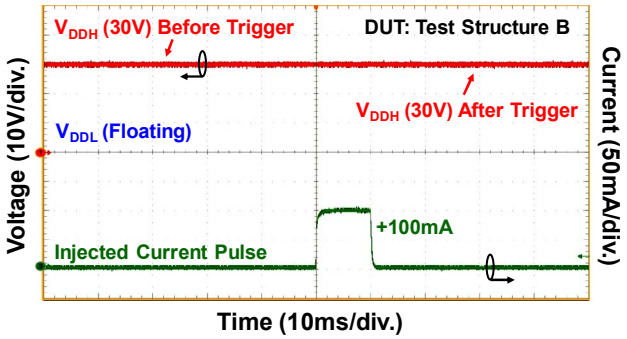
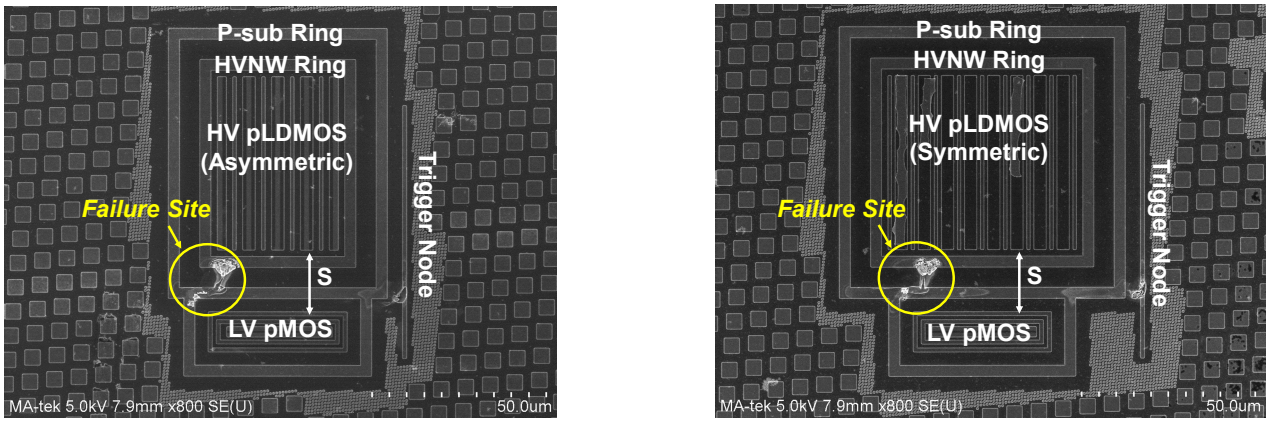


Figure 14: Measured time-domain voltage and current waveforms on the test structure B, with V_{DDH} of 30 V and V_{DDL} floating.

In Fig. 9, test structure A is given with initial bias voltages of 30 V at V_{DDH}, 1.8 V at V_{DDL}, and 0 V at V_{SS}. After the injection of 100-mA current pulse at $V_{Trigger}$ node, V_{DDH} of test structure A is clamped down to ~5 V and then burned out. Some transient glitches are induced on the current pulse. Afterwards, a large leakage current is detected from V_{DDH} to grounded V_{SS}. However, there is no leakage current found between V_{DDH} and V_{DDL} nodes. It was suspected that the injected current pulse may directly damage the test structure without inducing latchup. In order to verify whether such latchup path is fired or not, it is measured once again by changing V_{DDL} to 0 V or to be floating.

Fig. 10 shows the measured waveform with V_{DDL} of 0 V, which is similar to the test result in Fig. 9. In Fig. 11, the measured waveform with V_{DDL} floating does not show any voltage roll-off at V_{DDH} node after the same injection of 100-mA current pulse. From these measurement results, the latchup path between V_{DDH} and V_{DDL} nodes in Figs. 9 and 10 are exactly fired, and then directly burned out at V_{DDH} node with a leakage path induced between V_{DDH} and grounded V_{SS}.

As shown in Figs. 12, 13, and 14, the latchup path of test structure B is also fired and burned out with 100-mA current pulse. In addition, the voltage level of V_{DDH} is pulled down to only ~2 V on the test structure B after the current pulse trigger.



(a) (b)

Figure 15: SEM photographs of (a) test structure A and (b) test structure B to show the latchup-induced damage after the injection of latchup trigger current at trigger node, with a distance (S) of 20 μm in the latchup path.

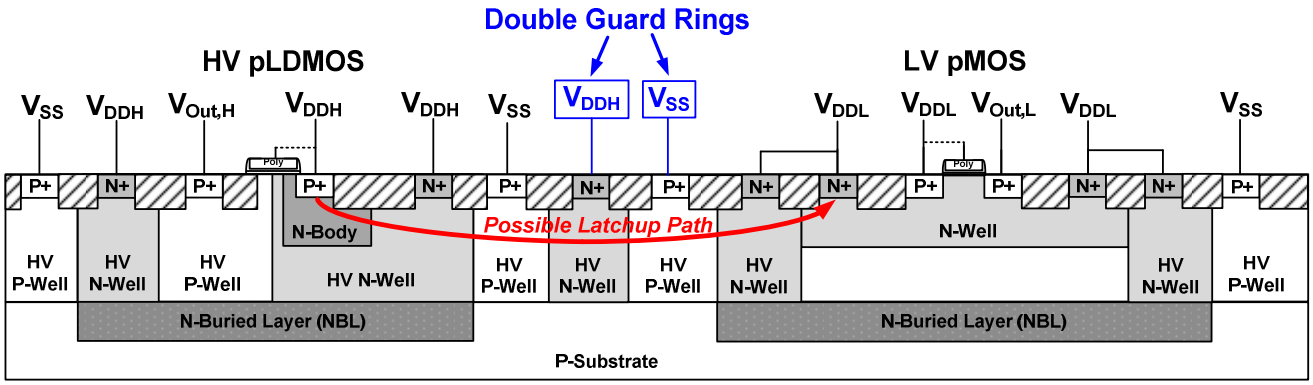


Figure 16: Double guard rings inserted within the parasitic latchup path between HV pLDMOS and LV pMOS.

In consequence, the current-trigger latchup test has verified that the cross-domain latchup path in both test structures can occur and induce the unexpected failures.

D. Failure Analysis

Figs. 15(a) and 15(b) show the SEM photographs of the test structures A and B, respectively, with the latchup-induced damage after the injection of positive latchup trigger current at trigger node. It is clearly found that the test structures A and B were damaged with some burn-out traces within the adjacent region between HV pLDMOS and LV pMOS. The failure sites shown in the SEM pictures are mainly located at the interface of HVNW and P-sub rings. It can explain why there is no leakage current detected at V_{DDL} node of LV pMOS. Though the expected burn-out trace from p+ source side of HV pLDMOS to V_{DDL}-connected NW of LV pMOS was not observed, the parasitic path between HV pLDMOS and LV pMOS indeed occurred and caused the unpredictable damages. In addition, some burn-out trace near trigger node is found, because the narrow diffusion region of trigger node was unable to sustain the joule heating induced by the injected current pulse of +100 mA.

IV. Discussion

From the 1000-ns TLP measurement results, it is likely that the holding voltage of parasitic latchup path could be much lower under the dc power-on condition, and even become more serious at the high ambient temperature (e.g., 125°C). To prevent such unexpected latchup failure between different power domains, the suggested solutions are (1) to extend the layout spacing between HV and LV parts and then to increase the holding voltage of the parasitic path, or (2) to add double guard rings to surround the HV pLDMOS for reducing the current gains of the parasitic BJTs, as illustrated in Fig. 16. Based on the previous study [4], different guard ring structures with different spacing between HV and LV domains can be studied to extract the design rules. Furthermore, it is recommended to develop the design rules for latchup prevention by double guard ring structure with

consideration of high-temperature condition and layout area efficiency in such a HV-to-LV boundary.

V. Conclusion

The characteristics of latchup path between HV pLDMOS and LV pMOS have been investigated and confirmed through the silicon chip fabricated in a HV BCD technology. With experimental verification under current-trigger latchup test, the cross-domain latchup path can be exactly induced by injecting a current pulse into p-substrate. According to the JEDEC standard, the test structures cannot pass the required latchup immunity level of 100 mA, even though it has been drawn with a foundry-suggested distance of 20 μm between HV and LV devices. Therefore, the layout rules between HV pLDMOS and LV pMOS should be further defined to avoid the occurrence of such HV-to-LV cross-domain latchup path in the given BCD technology.

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