Design of Multiple-Charge-Pump System for Implantable Biomedical Applications

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***Abstract*—Circuit design to implement a multiple-charge-pump (MCP) system in a low-voltage standard CMOS process is proposed, that can successfully support the desired power sources for implantable monopolar biphasic stimulator. A negative charge pump (CP) circuit with the four-phase cross-couple structure is introduced to suppress return-back leakage, and thus its power efficiency is improved. This MCP system provides the stimulator with three power sources of +9V, –9V, and –2.7V, simultaneously. Closed-loop operation helps for regulating the output voltage sources (+9V and –9V) with a maximum loading current of 5.5mA for stimulus drivers, and 1-mA current for the control circuits of the stimulator. The proposed MCP system has been fabricated in a 0.18-µm 1.8-V/3.3-V CMOS process, as well as successfully verified in *in-vivo* animal tests with stimulator together.**

Keywords— high voltage generator, multiple charge pump, positive charge pump, negative charge pump, power efficiency.

I. Introduction

In biomedical electronics, implantable stimulators are widely utilized to deliver voltage/current pulses as electrical stimulation treatment. For example, cochlear implants can preserve acoustic hearing [1], retinal prostheses can treat blindness [2], and neural stimulation can suppress epileptic seizures [3]. Related to stimulus patterns, a pair of positive and negative stimulus pulses is defined as biphasic stimulation. According to electrode configuration, the stimulus methodology is divided into two groups: two leads per site (bipolar stimulation) and one lead per site (monopolar stimulation) [2]. For bipolar biphasic stimulation, bidirectional current flows through tissues between two selected electrodes, as shown in Fig. 1(a). Thus, only one supply voltage is required. But for monopolar architecture in Fig. 1(b), dual supply voltage configuration is preferred to generate the anodic and cathodic stimulation. Hence, with respect to the ground potential, both positive and negative voltage sources are needed. Regardless of stimulus methods, the calculated output voltage of a voltage-mode stimulator is the approximate product of the electrode/tissue impedance and the equivalent current. For the purpose of implantation, physical dimension is one of the ley limiting factors. Therefore, on-chip capacitive converters (i.e. CP) are preferred to serve as voltage sources for stimulators rather than off-chip inductive converters.

Applied on proprioceptive prostheses, a reconfigurable switched-capacitor network was presented to generate 3V, 9V, and 12V in [4]. However, these voltages cannot exist simultaneously. In order to support monopolar biphasic stimulators, the Pelliconi CP was used to generate positive and negative voltages in a 0.8-µm high-voltage CMOS process [5], [6]. In each serial stage, charges are transferred through NMOS and PMOS switches. Unfortunately, PMOS, biased to negative voltage, would suffer body effects and substrate leakage in the triple-well CMOS process. NMOS switches with a four-phase sequence was advantaged to minimize leakage current and prevent these issues in [7]. Nonetheless, the maximum voltage stress on NMOS is as high as twice voltage (V_{DDH}), which may risk gate-oxide reliability issues on the low voltage devices.

Without using off-chip element, the charge pump (CP) to boost high positive/negative voltage is beneficial to system-on-chip (SoC) integration. In this work, a multiple-charge-pump (MCP) to provide the required supplies (+9V, –9V, and –2.7V) for monopolar biphasic stimulators is proposed. Cross-couple topologies ensure only one-times V_{DDH} deliveries in each cascaded stages. Four-phase operation prevents circuit from return-back leakage. Circuit implementation with all low-voltage transistors are carefully designed to avoid overstress concerns, which is fully integrated in a 0.18-µm 1.8-V/3.3-V CMOS process with deep n-well.

II. Proposed Multiple-Charge-Pump System

The proposed MCP system to support the desired power sources for a monopolar biphasic voltage-mode stimulator [8], configured to be an implantable stimulus scheme, is shown in Fig. 2. This system contains one positive CP and two negative CPs. Separately, one negative CP provides power (V_{SSH}) for the control circuits of stimulator, and the others are used to

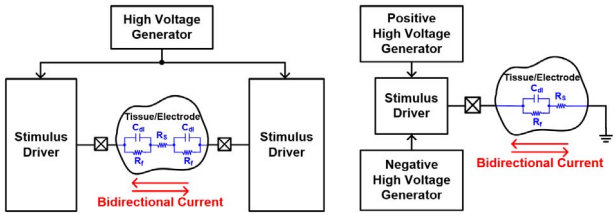

Fig. 1. (a) Bipolar stimulation. (b) Monopolar stimulation.

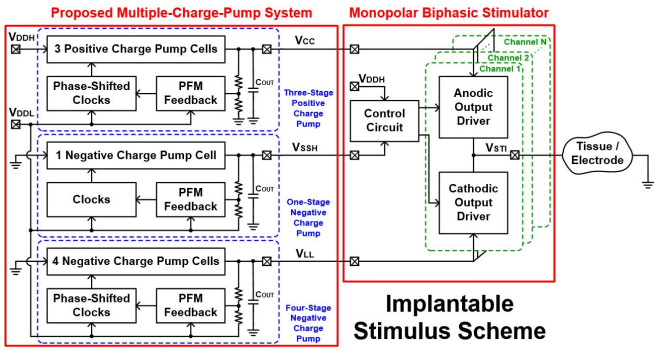

Fig. 2. Block diagram of the implantable stimulus scheme (this work).

generate the high voltage sources (V_{CC} and V_{LL}) for stimulus drivers. Only one negative cell is required for the former (V_{SSH}), yet the latter (V_{CC} and V_{LL}) is constructed of three serial positive cells and four cascaded negative cells, respectively. With phase-frequency-modulation (PFM) feedback control, each CP is seen as a self-regulated closed-loop unit to sustain extensive output loading conditions and further maintain efficiency. Furthermore, peak current reduction on V_{DDH} is also taken into account in biomedical SoC. It can improve transient response of the front power source and reduce injected noise into other circuit blocks. Therefore, the phase-shifted clock technique is applied to reduce the input peak current [9].

A. Positive Charge Pump

A positive CP cell [10] with two identical branches is shown in Fig. 3(a). Each branch is composed of two main transistors (M_{P1}, M_{N1} or M_{P2}, M_{N2}), an auxiliary transistor (M_{S1} or M_{S2}), a main pumping capacitor (C_P), and an auxiliary capacitor (C_{aux}). To minimize return-back leakage resulted from the transition of clocks, main transistors are switched sequentially by auxiliary transistors and four-phase clocks. Assume that the input node V_{IN} is $n \cdot V_{DDH}$ and the output node V_{OUT} is $(n+1) \cdot V_{DDH}$, respectively.

The four-phase clock splits the operation of this positive CP into eight steps (t_1 to t_8), as illustrated in Fig. 4(a). The concepts of the first four steps (from t_1 to t_4) and the last four steps (from t_5 to t_8) are the same. At the first interval t_1 (the fifth interval t_5), the voltages of node g1 and node n2 (node g2 and node n1) are $(n+1) \cdot V_{DDH}$, while the voltages of node n1 and node g2 (node n2 and node g1) are $n \cdot V_{DDH}$. Charges are mainly transferred through the conducted M_{P2} and M_{N1} (M_{P1} and M_{N2}). Because of the off-state M_{S2} (M_{S1}), M_{P2} and M_{N1} (M_{P1} and M_{N2}) are turned off at the second interval t_2 and the third interval t_3 (the sixth interval t_6 and the seventh intervals t_7), respectively. Thus, all of the main transistors are free from simultaneous conduction to avoid return-back leakage issue. A slight charge sharing concerns between C_P and C_{aux} is minimized by the short time interval t_3 (t_7). Then, at the fourth interval t_4 (the eighth interval t_8), M_{N2} (M_{N1}) is turned on whereas M_{S1} (M_{S2}) is turned off. The off-state M_{S1} (M_{S2}) ensures that the node g1 (node g2) will only turn M_{P1} (M_{P2}) on at the fifth interval t_5 (the first interval t_1). Meanwhile, the main charge transfer paths are smoothly changed to the on-state M_{P1} and M_{N2} (M_{P2} and M_{N1}).

B. Negative Charge Pump

Referred to [11], the new proposed negative CP cell is a four-phase cross-couple structure but involves all NMOS switches, as depicted in Fig. 3(b). Besides, the main pumping capacitor is represented as C_P and the auxiliary capacitor is represented as C_{aux}. Since P-substrate is often connected to the ground potential in SoC integration, PMOS is forbidden to be operated in negative voltage. Thus, a negative CP circuit consists of only NMOS switches with deep N-Well (marked with gray area) to isolate the P-well of each NMOS from P-substrate. On the other hand, the bulk and source terminals can be connected together in each NMOS, therefore the NMOS switches are kept from body effect as well as substrate leakage.

The waveforms of the four-phase clock and the corresponding internal nodes are shown in Fig. 4(b). Suppose that the input node V_{IN} and the output node V_{OUT} are 0V and $-V_{DDH}$, respectively. The transient behaviors of the proposed circuit are separated into eight time intervals (t_1 to t_8). Due to a mutually symmetrical structure, the first-half period (from t_1 to t_4) and the second-half period (from t_5 to t_8) are similar. At the first interval t_1 (the fifth interval t_5), the voltages of nodes g1, n1, g2, and n2 (nodes g2, n2, g1, and n1) are $-V_{DDH}$, $-V_{DDH}$, $V_{DDH}-V_{TH}$, and 0V, respectively. Thus, M_{N2} and M_{N4} (M_{N1} and M_{N5}) are on-state to transfer charges while M_{N1} and M_{N5} (M_{N2} and M_{N4}) are off-state. By the way, M_{N3} (M_{N6}) is turned on to ensure M_{N1} and M_{N5} (M_{N2} and M_{N4}) being fully turned off. At the second interval t_2 (the sixth interval t_6), node g2 (node g1) drops to $-V_{TH}$ to turn off M_{N4} (M_{N1}), and besides M_{N6} (M_{N3}) is slightly turned on. At the third interval t_3 (the seventh interval t_7), all the internal nodes are $-V_{DDH}$, so that both M_{N3} and M_{N6} are on-state to ensure the rest of switches being fully turned off. Thus, there is no return-back leakage path during the circuit operation. At the fourth interval t_4 (the eighth interval t_8), owing to an on-state M_{N3} (M_{N6}), node n1 (node n2) rises to 0V but only brings node g1 (node g2) to $-V_{TH}$. Accordingly, M_{N3} (M_{N6}) is conducted until the fifth interval t_5 (the first interval t_1). At this moment, node g1 (node g2) is raised to $V_{DDH}-V_{TH}$ and M_{N3} (M_{N6}) is turned off. To simplify, M_{N5} and M_{N1} (M_{N4} and M_{N2}) are conducted sequentially to transfer charges.

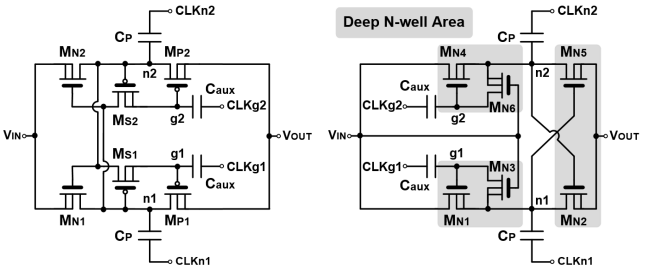

Fig. 3. Circuit schematics of (a) a positive CP cell and (b) a negative CP cell.

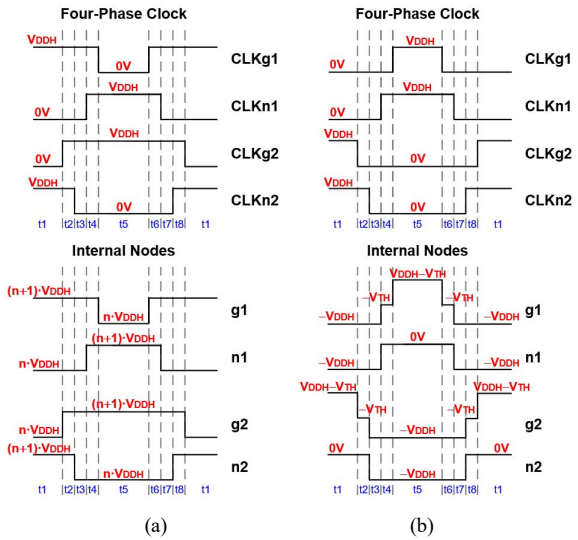

Fig. 4. Four-phase clocking waveforms for (a) a positive CP cell and (b) a negative CP cell. All the desired clocks are generated on chip.

Any two terminals of all MOSFETs in the new proposed negative CP circuit do not exceed V_{DDH} (3V). Due to the suppression of return-back leakage, the power conversion efficiency is improved with the four-phase clock. In summary, the output voltage can be pumped to positive or negative high voltage without return-back leakage and gate-oxide overstress.

III. Experimental Results

The die microphotograph of MCP chip fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process is shown in Fig. 5. It occupies a silicon area of 4.09 mm^2, including all the on-chip pumping capacitors (C_P), auxiliary capacitors (C_{aux}), and output capacitors (C_{OUT}). Capacitances are determined in view of the parasitic effect and loading condition.

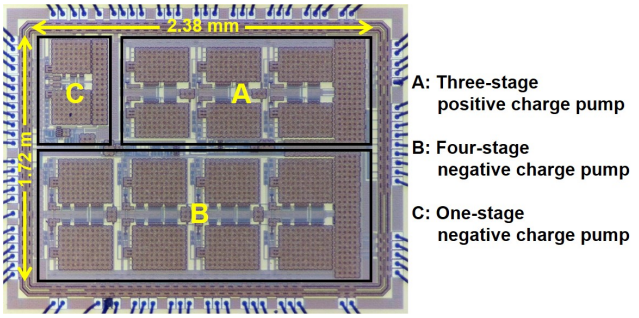

Fig. 5. Die microphotograph of the MCP system.

With the supplied input voltages of 1.8V (V_{DDL}) and 3V (V_{DDH}), the MCP system is expected to generate three voltage sources of +9V, −9V and −2.7V. The characteristics of these three CPs are measured and illustrated in Fig. 6. At a maximum 5.5-mA loading current, the output voltages of the three-stage positive CP (V_{CC}) and the four-stage negative CP (V_{LL}) can be regulated at +8.956V and −8.954V, respectively. Under different loading current, power efficiency is maintained above 60% for the three-stage positive CP and 50% for the four-stage negative CP, respectively. When the three-stage positive CP provides +8.956-V voltage and 3-mA current, it has the greatest power efficiency of 66.34%. With a peak efficiency of 53.88%, V_{LL} is stabilized at −9.004V when the loading current is 2mA. To reach the target voltage (V_{SSH}) of −2.712V, the one-stage negative CP can supply maximum 1-mA loading current with power efficiency of 41.32%. Since the MCP system is one of circuit blocks in neuron stimulation SoC, it contributes power sources towards monopolar stimulators. Clearly, ±9V are for stimulus driver and −2.7V is for control circuits. The MCP system only consumes power during stimulation periods. Additionally, none of off-chip components is favorable to implantation.

Based on these measured results, specifications of the fabricated MCP system are shown in Table I and compared with other previous works. Moreover, the performance comparisons between the proposed negative CP and the related prior arts are listed in Table II. In this work, multiple outputs and large loading current are the major realization in a low-voltage process.

IV. Biomedical Applications

As the illustration of measurement setup inset into Fig. 7 for *in-vivo* animal test, the MCP chip was used to support power sources for a monopolar biphasic stimulator chip in the stimulus scheme. The stimulator is able to deliver biphasic stimulus voltages of ±6V as the MCP supplies voltage sources. Among *in-vivo* tests on guinea pig, electrodes are placed at the bone surface and the round window of its ear. According to the evoked auditory brainstem response (EABR) waveforms [12], this stimulus scheme elicits neural responses efficiently. Fig. 7 also exhibits the comparisons of EABR waveforms evoked by the commercial stimulator (red line) and the implantable stimulus scheme (blue line) of this work (shown in Fig.2). The proposed MCP system is sufficient to meet the power demands of this stimulator.

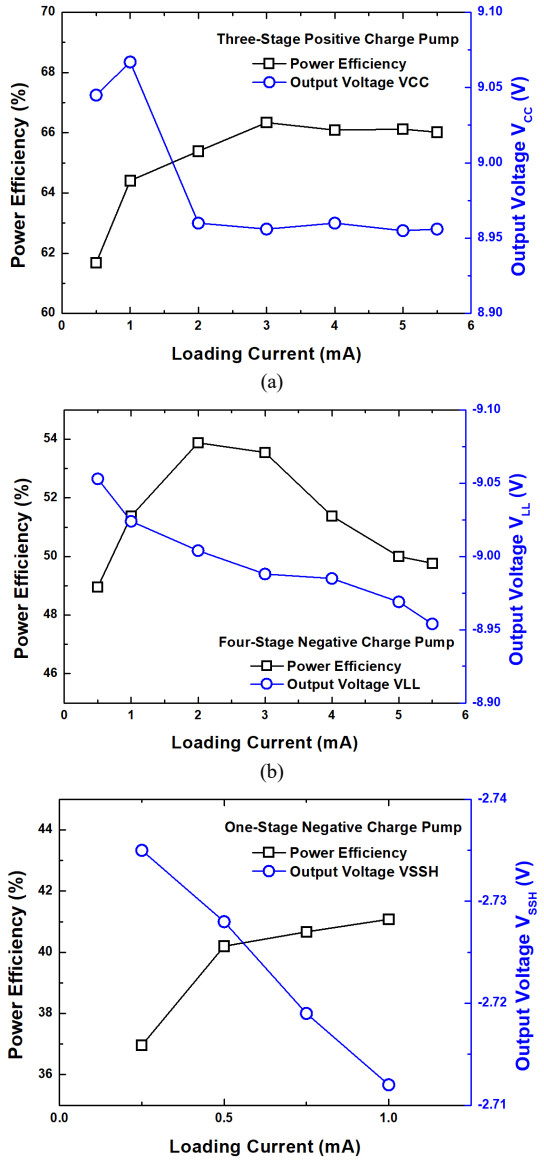

Fig. 6. The power efficiency and output voltage level of each CP versus the loading current. (a) Three-stage positive CP for V_{CC}. (b) Four-stage negative CP for V_{LL}. (c) One-stage negative CP for V_{SSH}.

V. Conclusion

Since both positive and negative voltage sources are necessary for a monopolar stimulator to deliver biphasic stimulation, a MCP system is presented and realized in a 0.18-µm 1.8-V/3.3-V CMOS process. The fully integrated MCP system has been characterized to successfully generate three voltage sources of +8.956V, −8.954V, and −2.712V. A PFM closed-loop operation dedicates to improve efficiency against loading variation. The overall power efficiency is kept between 41% and 66%. Power would only dissipate during stimulation to achieve an energy-efficient stimuli. Adopting cross-couple topologies as the voltage doublers would release overstress concerns. Besides, a negative CP is proposed and aims to be integrated in a low-voltage process. With four-phase clock operation, the return-back leakage is minimized and the power conversion ratio of the new negative CP is further increased. The *in-vivo* animal tests have clearly proved that the proposed MCP system is robust to support stimulators.

TABLE I. Comparisons among Multiple-Charge-Pump Systems

Parameters		**This work**	**2009 [5]**	**2012 [6]**	**2013 [4]**
Techonology		0.18-µm (standard, LV)	0.8-µm (HV)	0.8-µm (HV)	0.18-µm (HV)
Input voltage		3V / 1.8V	3.3 V	N/A	6 V
Output voltage		Multiple (±9V, −2.7V)	Multiple (±9V)	Multiple (±13V)	Single (3V, 9V, 12V)
Maximum loading current		5.5 mA	0.2 mA	1 mA	0.5 mA
Peak power efficiency	All	41% to 66%	35% to 42%	84.32%	60% to 80%
	+9V	66.34%	41.77%	N/A	80%
	−9V	55.38%	35.88%	N/A	N/A
	−2.7V	41.32%	N/A	N/A	N/A
Off-chip capacitors		NO	NO	YES	NO
Silicon area		4.09 mm^2	8.38 mm^2	9 mm^2	5.4 mm^2
Verification		Experimental *in-vivo* animal test	Post-layout simulation	Post-layout simulation	Experimental *in-vitro* animal test

TABLE II. Comparisons among Negative Charge Pumps

Parameters	**This work**	**2009 [5]**	**2012 [7]**	**2016 [13]**
Techonology	0.18-µm (standard)	0.8-µm (HV)	0.18-µm (standard)	0.13-µm (standard)
Input voltage	3V / 1.8V	3.3 V	1.8 V	1.2 V
Output voltage	−8.954 V	−8.348 V	−8.04 V	−9.4 V
Maximum loading current	5.5 mA	0.2 mA	0.32 mA	0.05 mA
Peak power efficiency	55.38 % @ 2 mA	35.88 % @ 0.2 mA	42.26 % @ 0.2 mA	67.43 % @ 0.01 mA
Pumping capacitances	100 pF	25 pF	25 pF	1 pF

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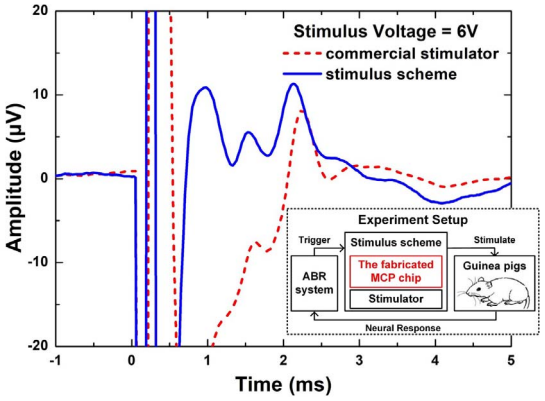

Fig. 7. *In-vivo* measurement setup and comparisons on the measured EABR waveforms evoked by a commercial stimulator (a bulky equipment) or the proposed implantable stimulus scheme in siliocn chip (this work).

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