ESD Protection Design of High-Linearity SPDT CMOS T/R Switch for Cellular Applications

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***Abstract*—Electrostatic discharge (ESD) protection design for high-linearity single-pole double-throw (SPDT) transmit/receive switch (T/R switch) at 0.9/1.8 GHz GSM band was proposed and verified in a standard 0.18-μm CMOS process. The SPDT CMOS T/R switch was implemented with body-floating technique, multi-stacked structure, and series-shunt topology to obtain low insertion loss, high power handling capability, and good isolation. With the proposed ESD protection design, the T/R switch can sustain human-body-model (HBM) ESD voltages of 3.5 kV under the positive-to-V_{SS} stress and 5 kV under the negative-to-V_{SS} stress. Experimental results including ESD characteristics, RF performance, and failure analysis are presented.**

***Keywords*— ESD protection design, transient detection circuit, high-linearity switch, power-rail ESD clamp circuit, SPDT, T/R switch.**

I. INTRODUCTION

The RF transmit/receive front-end circuit plays an important role between antenna and mixer, including low noise amplifier (LNA), power amplifier (PA), and transmit/receive switch (T/R switch), as shown in Fig. 1 [1]-[3]. However, ESD protection circuit such as conventional dual diodes and power-rail clamp circuit must be placed to the I/O pad and co-designed with the RF transmit/receive front-end circuit together [4], [5]. The low-capacitance and area-efficient ESD protection devices are strongly requested by RF ICs. Due to the position between antenna and the transceiver circuits, the antenna node (ANT) of T/R switch is very sensitive to ESD stress during module assembly. Therefore, on-chip ESD protection design shall be provided to the ANT node of T/R switch.

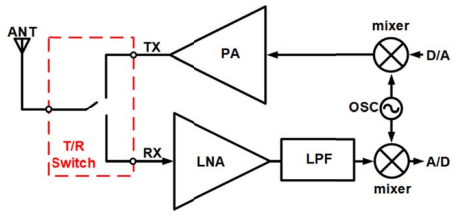

Fig. 1. RF transceiver front-end circuit with T/R switch.

The conventional ESD protection scheme (dual diodes + power-rail ESD clamp circuit) can meet a typical specification of 2-kV HBM ESD stress. However, such a conventional ESD protection scheme was not suitable for the ESD protection design targeted to the T/R switch for 0.9/1.8GHz GSM cellular applications. Since the maximum GSM transmitter power can reach 30 dBm, the large amplitude and high-frequency transmitting signals from the transmitting (TX) path may mis-trigger on the conventional ESD protection circuit. Besides, the existence of the body-floating resistor, which is used to suppress the insertion loss in the high-power T/R switch, prevents the parasitic path at the ANT node for ESD current discharging to V_{SS}. Therefore, a suitable ESD protection design customized for high-power T/R switch must be developed to effectively protect the T/R switch and the inner core circuits.

II. DESIGN OF T/R SWITCH

The T/R switch using series-shunt topology with multi-stacked-transistor architecture [6] had been implemented in a 0.18-μm standard CMOS process. The schematic of the high-power T/R switch is illustrated in Fig. 2. There are 6 terminals in the schematic, including ANT, TX, RX, V_{TX}, V_{RX}, and GND. By controlling the voltage signals V_{TX} and V_{RX}, the operation modes of the circuit can be determined. In the circuit schematic, $M_1 \sim M_4$ and $M_6 \sim M_8$ are the series transistors of receiving (RX) branch and transmitting (TX) branch, respectively. On the contrary, M_5 and $M_9 \sim M_{12}$ are the shunt transistors of RX branch and TX branch, respectively. In this architecture, the number of the stacked transistors is determined by the specification of power handling capability. During the transmit-mode circuit operations, $M_1 \sim M_4$ and $M_9 \sim M_{12}$ are in off-state and stacked in series to sustain the signals of high voltage swing. However, the stacked $M_1 \sim M_4$ will also increase the insertion loss in RX branch, since the turn-on resistance is multiplied by the number of the stacked transistors.

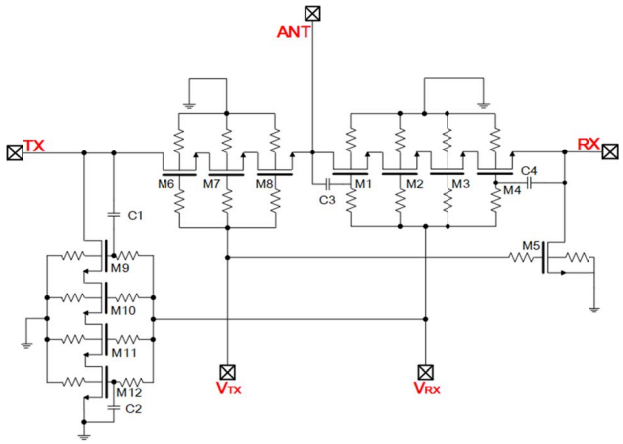

Fig. 2. Schematic of a T/R switch without ESD protection.

III. DESIGN OF ESD PROTECTION

The proposed ESD protection scheme, as drawn in Fig. 3, attempts to deal with the positive-to-V_{SS} (PS-mode) ESD threat on the ANT port. A transient detection circuit is located at the ANT port to distinguish the ESD transition in ESD events from the RF signals in normal circuit operations. With a proper ESD transient detection circuit, the ESD current on the ANT port is discharged to ground by the RX transistors of the T/R switch. The ESD discharging path is chosen with the transistors of RX branch instead of the TX's, because the number of the stacked transistors in RX branch is fewer than that in TX branch. In the

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NS-mode (negative-to-V_{SS}) ESD stress, the stacked parasitic bipolar junction transistors (BJT's) of the inherent transistors will be the discharging path. Although the T/R switch has no circuit directly connecting to the V_{DD} node, the PD-mode (positive-to-V_{DD}) and ND-mode (negative-to-V_{DD}) ESD tests are still applied to check the ESD robustness of a RF transceiver chip. The PD-mode and ND-mode ESD discharging paths in the high-power T/R switch are illustrated in Fig. 4, where the discharging paths from the ANT to V_{DD} for the PD-mode and ND-mode ESD events are shown with the red line and the blue line, respectively. The traditional power-rail ESD clamp circuit can achieve the ESD level of ± 8kV easily. As a consequence, the weakest part along the PD-mode and ND-mode discharging paths is located at the ANT-to-V_{SS} segment in the T/R switch. In other words, the ESD robustness of PD-mode and ND-mode stresses is determined by the ESD levels of T/R switch under PS-mode and NS-mode stresses. So, this work emphasizes the ESD discharging paths between the ANT node and V_{SS}.

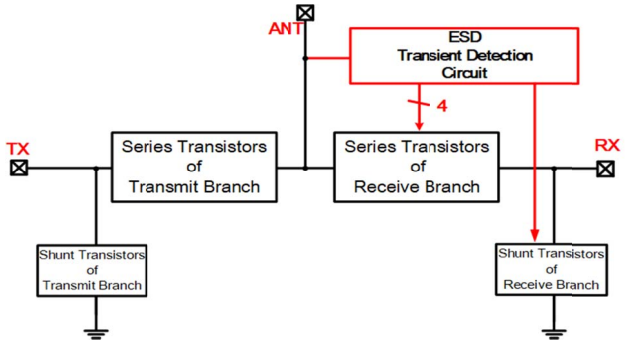


Fig. 3. The schematic of the proposed ESD protection scheme.

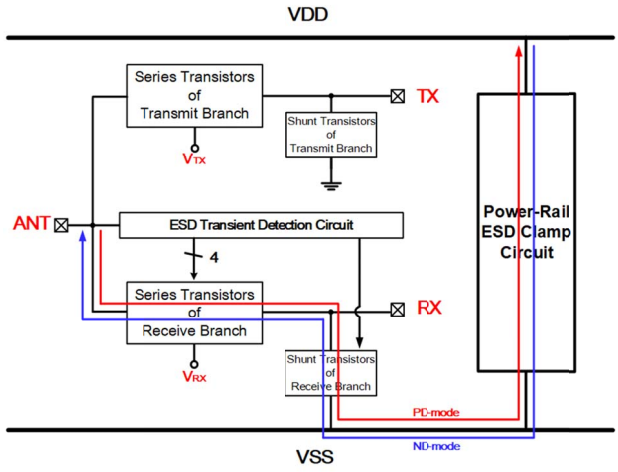


Fig. 4. The discharging paths under PD-mode and ND-mode ESD stress.

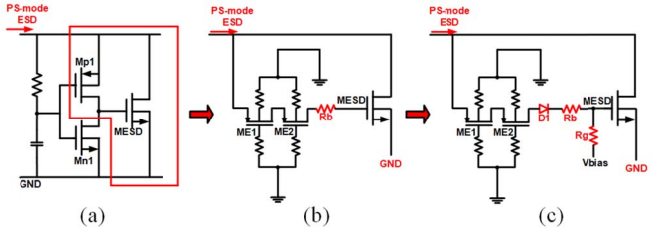


Fig. 5. The evolution of the ESD transient detection circuit from (a) power-rail clamp circuit, via (b) stacked PMOS and resistor R_b to distinguish the RF signals from ESD transient, to (c) diode D1 and resistor R_g to ensure the normal DC voltage bias of the RX transistors.

A. Type 1 ESD Protection Design

The idea of the ESD transient detection circuit was inspired from the traditional power-rail ESD clamp circuit. The evolution of the design is depicted in Fig. 5(a) ~ Fig. 5(c). In the power-rail ESD clamp circuit with RC-inverter scheme [7], the large transistor M_{ESD} is triggered on by the transistor Mp1 during ESD events. However, the T/R switch circuit in Fig. 2 has no connection to the VDD node. Thus, only the PMOS Mp1 and large M_{ESD} in the power-rail ESD clamp circuit are preserved in the proposed ESD protection design.

The traditional power-rail ESD clamp circuit can be simplified to the red frame in Fig. 5(a). Next, in order to endure the large voltage swing from the transmitter, more PMOS's are stacked and equipped with the gate and the body-floating resistors, which are similar to the transistors in the T/R switch circuit. Moreover, in Fig. 5(b), a blocking resistor R_b of 10 kΩ is employed to block the normal RF signals from the ANT port. Since the frequency (GHz) of RF signals is much faster than that (MHz) of the ESD transient, the blocking resistor R_b can block the RF signals to reach the gate of M_{ESD}, whereas the slower ESD transient can pass through it to reach the gate of M_{ESD}. In Fig. 5(c), a diode D1 is inserted between the gate of M_{ESD} and the detection circuit to isolate the DC voltage bias of the transistors in normal circuit operations. Based on this design concept, the ESD transient detection circuit (as shown in Fig. 3) can be realized to turn on the transistors of receive branch for ESD current discharging.

The whole circuit schematic of the proposed ESD protection design realized with the T/R switch circuit together is shown in Fig. 6(a), which is named as "type 1" ESD protection design in this work. The ESD transient detection circuit of type 1 is constructed by the stacked PMOS transistors (M_{E1}, M_{E2}, and M_{E3}), blocking resistors (R_{b1}, R_{b2}, R_{b3}, R_{b4}, and R_{b5}), diode D_1, and a diode string (of 8 diodes). Under the PS-mode ESD stress condition, the positive ESD voltage zapping at ANT port will pass through the ESD transient detection circuit to charge the gates of M_1 ~ M_5 in the RX branch. The turn-on resistance R_{on} among the M_{E1} ~ M_{E3} will affect the trigger time of the RX transistors to discharge ESD current. The gates of M_1 ~ M_5 will be charged up faster, if the dimensions of M_{E1} ~ M_{E3} are larger. Therefore, the device dimensions (W/L) of M_{E1}, M_{E2}, and M_{E3} are all selected as 300μm/0.35μm. Besides, the number of the stacked "M_E" transistors will influence the power compression point, too. With consideration of gate oxide reliability during the TX mode operation, three stacked PMOS transistors (M_{E1}, M_{E2}, and M_{E3}) are used. Finally, a diode string (of 8 diodes) is utilized to make sure that the proposed ESD protection design does not affect the normal T/R switch circuit operations with the control signal V_{TX}.

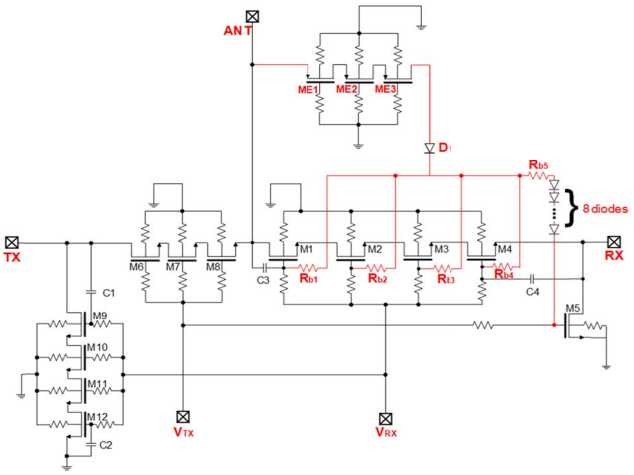
B. Type 2 ESD Protection Design

In T/R switch with body-floating technique, the body of each transistor is separated from its source and connected with a large resistor to ground. In the proposed type 1 ESD protection design, since the ESD stress is delivered from drain to source rapidly after the M_1 ~ M_5 are triggered on under PS-mode ESD events, the voltage at the body of each transistor cannot be kept the same as that at its source. The voltage difference between source and body will increase the threshold voltage (V_{th}) of the

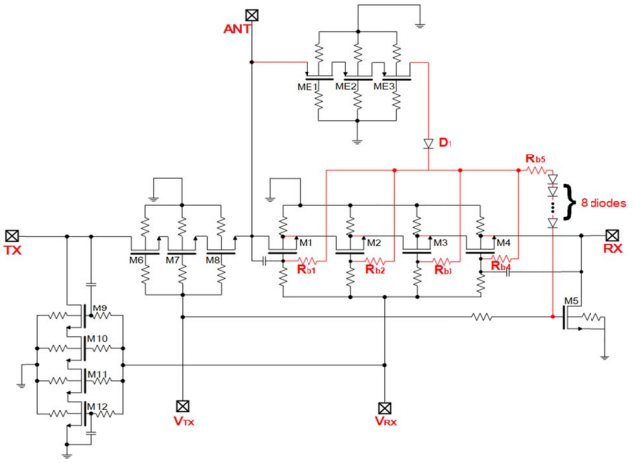
NMOS transistors due to the body effect. The increasing V_{th} is not a good thing for type 1 ESD protection design, because it reduces the current conducting capability among the transistors ($M_1 \sim M_5$) to discharge the ESD current from ANT to ground. Therefore, a modified design is depicted in Fig. 6(b), which is named as the "type 2" ESD protection design in this work. With body and source connected together in the transistors $M_1 \sim M_4$, the rising of the threshold voltage can be eliminated. The PS-mode ESD robustness of the type 2 ESD protection design is expected to be better than that of the type 1 ESD protection design, because the transistors ($M_1 \sim M_4$) in type 2 ESD protection design do not suffer the body effect. However, when the body and source are connected together in the transistors ($M_1 \sim M_4$), the RF signals at ANT port would leak to RX port more easily. The drawback is that the performance of insertion loss and linearity in transmit mode will be degraded.

Under NS-mode ESD stress on ANT port, the discharging paths are formed by the parasitic BJT's of the stacked NMOS transistors in both RX and TX branches. As illustrated in Fig. 7(a), the base of each BJT is connected to ground through a body-floating resistor of 10 kΩ. The voltage potential of the base will be raised during NS-mode ESD events. Once the V_{BE} exceeds the turn-on voltage of BJT, the parasitic BJT's will be triggered on to discharge the NS-mode ESD current.

The cross-sectional view to show the NS-mode discharging path in the type 2 ESD protection design is sketched in Fig. 7(b). A parasitic diode string in series connection is formed naturally among the NMOS transistors. The location of the parasitic diode in each NMOS transistor is also indicated in Fig. 7(b). The parasitic diodes among the transistors in RX branch will be the preferred path to discharge NS-mode ESD stress, as comparing to the BJT path in TX branch. Therefore, the NS-mode ESD robustness of the type 2 design will be higher than that of the type 1 design.

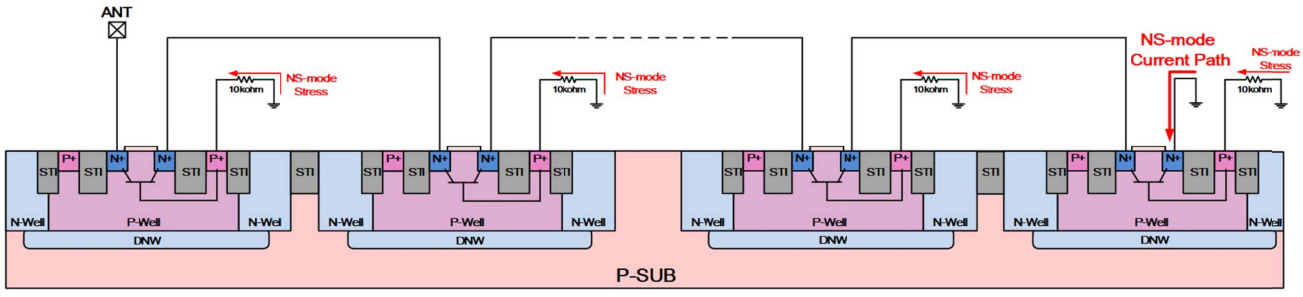


(a)

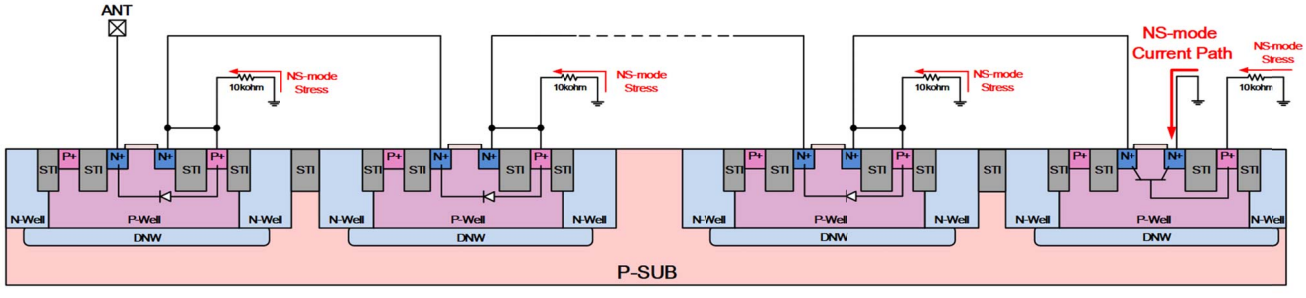


(b)

Fig. 6. The proposed ESD protection designs of (a) type 1, and (b) type 2, for the high-linearity T/R switch.



(a)



(b)

Fig. 7. (a) Cross-sectional view of the stacked-transistors showing (a) the series parasitic BJTs of NS-mode discharging path in the type 1 ESD protection design, and (b) the series parasitic diodes of NS-mode discharging path in the type 2 ESD protection design.

IV. Experimental Results

The proposed ESD protection designs (type 1 and type 2) with the T/R switch together had been fabricated in a 0.18-µm CMOS process. A photo of the fabricated chip is shown in Fig. 8. The area of a single T/R switch is 0.5mm×1mm. The RX mode insertion loss of the high-power T/R switch without ESD protection design is 1.98/2.83dB at 0.9/1.8GHz, whereas the TX mode insertion loss is 1.81/2.58dB at 0.9/1.8GHz. For the T/R switch with the type 1 or type 2 ESD protection designs, there is a degradation of 0.2dB ~ 0.5dB in GSM bands on its insertion loss. Fig. 9 shows the comparison of measured P_{1dB} among the T/R switches. The P_{1dB} of T/R switch without ESD protection design can reach 28.6dBm at 1.8GHz. However, the P_{1dB} of the T/R switch with type 1 and type 2 ESD protection designs are only 23.4dBm and 22.7dBm, respectively.

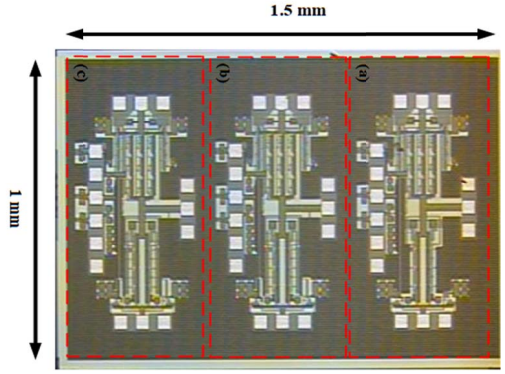


Fig. 8. Chip photo of (a) high-power T/R switch, (b) high-power T/R switch with type 1 ESD protection design, and (c) high-power T/R switch with type 2 ESD protection design.

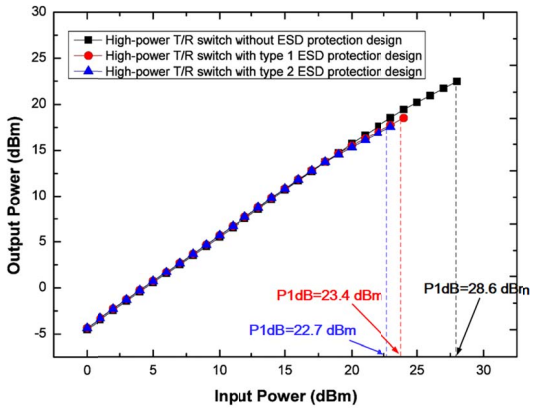
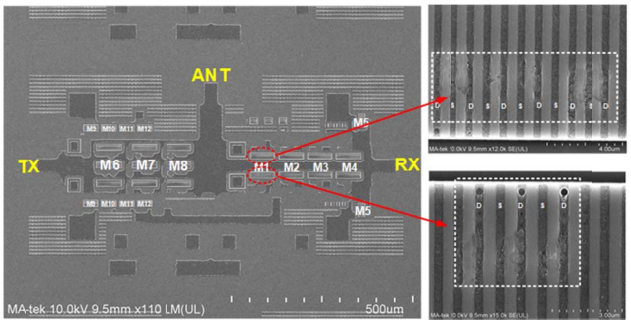


Fig. 9. Measured P_{1dB} of the T/R switches at 1.8GHz, with or without ESD protection.

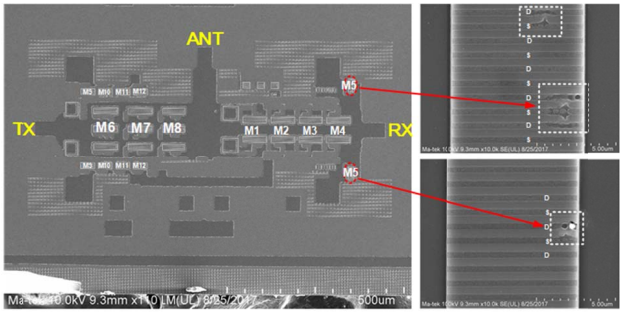
TABLE I
Measured HBM levels among the T/R switches

HBM ESD tests on ANT node	Judged by DC IV curves		Judged by RF performance	
	PS-mode	NS-mode	PS-mode	NS-mode
T/R switch w/o ESD protection design	0.1 kV	5 kV	below 0.5 kV	> 4 kV
T/R switch with type 1 ESD protection design	3.75 kV	5 kV	3.5 kV	> 4 kV
T/R switch with type 2 ESD protection design	4.5 kV	6 kV	4.5 kV	> 4 kV

The HBM ESD levels of the fabricated T/R switches with or without ESD protection design, judged by DC-IV curves or by RF performance degradation, are summarized in Table I. Failure analysis is used to investigate the damaged locations on the T/R switches after ESD test. Fig. 10(a) shows the damaged transistors in the T/R switch with type 1 ESD protection design after PS-mode ESD stress of 4 kV, where the burned-out marks are located at the RX transistor M_1. In Fig. 10(b), the damaged parts on the T/R switch with type 2 ESD protection design after PS-mode ESD stress of 5 kV are located at the shunt transistor M_5 of RX branch. Since the body and source are connected together in the type 2 ESD protection design, the ESD current can be more efficiency delivered to the last and the smallest transistor (M_5) of the discharging path.



(a)



(b)

Fig. 10. SEM photos of (a) T/R switch with type 1 ESD protection design after PS-mode HBM ESD stress of 4 kV, and (b) T/R switch with type 2 ESD protection design after PS-mode HBM ESD stress of 5 kV.

V. Conclusion

The high-power T/R switch with the proposed type 1 and type 2 ESD protection designs have been verified in a 0.18-µm CMOS process. The RF performance and ESD robustness of the T/R switch with and without ESD protection have been practically measured and analyzed in silicon. The PS-mode ESD stress is the most critical event of the original T/R switch. In this work, the ESD protection designs of type 1 and type 2 can discharge ESD current through the inherent parasitic paths among the RX transistors to enhance the PS-mode HBM ESD robustness from the original level of 0.1kV to 3.5kV and 4.5kV, respectively.

Acknowledgment

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