ESD TEST METHODS ON INTEGRATED CIRCUITS : AN OVERVIEW

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ABSTRACT: ESD phenomenon has become a serious problem for IC products fabricated by deep-submicron CMOS technologies. To qualify the ESD immunity of IC products, there are some test methods and standards developed by some organizations, which are ESDA, AEC, EIA/JEDEC, and MIL-STD organizations. ESD events have been classified into 4 models, which are HBM, MM, CDM, and SDM. Besides, there are 4 modes of pin combinations for ESD zapping on the IC pins, which are specified as (1) Pin-to-VSS, (2) Pin-to-VDD, (3) Pin-to-Pin, and (4) VDD-to-VSS. All the test methods are designed to evaluate the ESD immunity of IC products. The zap number, zap interval, and sample size are all well defined in the related industrial standards. This paper provides an overview among ESD test methods on IC products. In general, the commercial IC products are requested to sustain at least 2-kV HBM, 200-V MM, and 1-kV CDM ESD stresses.

1. INTRODUCTION

ESD (electrostatic discharge) phenomenon can happen according to the different electrostatic potentials between two or more objects, and EOS (electrical overstress) is taken place by the electrical event that is outside the specified range of the DUT (device under test). Devices are usually damaged by EOS/ESD via the rapidly generated heat or the rapidly created strong electrical field. The latent or fatal failures on a silicon chip are possibly caused by even an electrostatic discharge or electrical overstress event. To predict the ESD immunity level, or to find the ESD sensitive (weak) point of the DUT, there are several organizations who make the ESD related primary standards. They are ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA/JEDEC (Electronic Industries Alliance / Joint Electron Device Engineering Council), and MIL-STD (US Military Standard). The ESD test methods are known as HBM (Human Body Model), MM (Machine Model), CDM (non-socketed Charged-Device Model, Field Induced Model, or Direct Charge Model), and SDM (Socket Device Model, or Socketed Discharge Model).

There are four pin combinations for ESD test on an IC product which are shown in Fig. 1, which are known as Pin-to-VSS, Pin-to-VDD, Pin-to-Pin, and VDD-to-VSS. The Pin-to-VSS stress, shown in Fig. 1(a), is to apply the ESD stress on the PUT (pin under test) when the VSS pins are connected to ground. The Pin-to-VDD stress, which is shown in Fig. 1(b), is to apply the ESD stress on the PUT when the VDD pins are connected to ground. The Pin-to-Pin stress, which is shown in Fig. 1(c), is to apply the ESD stress on the PUT when the other pins, except VDD/VSS pins, are connected to ground. The VDD-to-VSS stress, which is shown in Fig. 1(d), is to apply the ESD stress on the VDD pins when VSS pins are connected to ground. The ESD stresses can have positive or negative voltage with respect to the ground. The IC after ESD stresses, it may cause damages not only locating at the I/O circuits or devices, but also locating in the internal circuits. Therefore, each IC product must be designed with effective on-chip ESD protection circuits to sustain the requested ESD level.

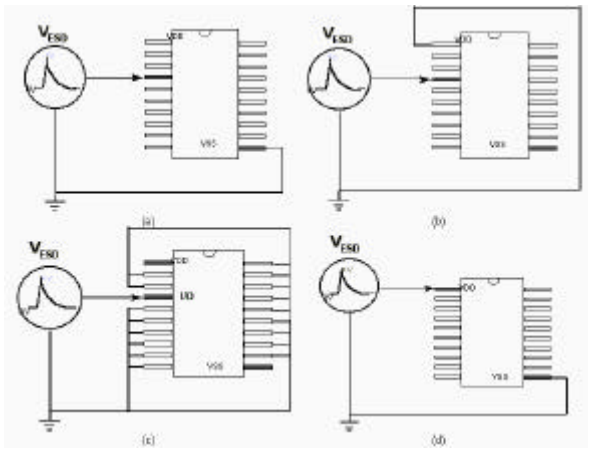

Fig. 1 The Pin combination for ESD test on an IC product: (a) Pin-to-VSS; (b) Pin-to-VDD; (c) Pin-to-Pin; and (d) VDD-to-VSS.

2. HUMAN BODY MODEL (HBM)

The typical ESD event for the real-case HBM ESD event is shown in Fig. 2. The ESD static charges are initially stored in the body of a human, and then transfer into the IC, when the finger of a human touches the IC. The equivalent circuit diagram of HBM ESD event is shown in Fig. 3 [1], which is used to replicate the HBM ESD events on semiconductor devices. The HBM circuit is designed to eliminate the weak protection designs and susceptible devices of the DUT. The most important is that it can provide a repeatable means to simulate field ESD failures of the DUT.

Fig. 4 shows the waveform specifications of a HBM ESD pulse, generated by the ESD HBM tester to a short wire [1]. Generally, commercial IC's are requested to sustain at least 2-kV HBM ESD stress according to the classification in the standards. A 2-kV HBM ESD event can generate an ESD current peak of ~1.3Amp with a rise time of ~10ns. There are 3 dependencies on HBM

ESD tester. The first one is the path length from the pulse source to the device(s), and from the device(s) to the ground plate. The second is the parasitic effect of different IC packages and fixture designs of the tester, and the last is the parasitic inductance and capacitance of the tester. The sample size of an IC product for HBM ESD verification under each pin combination should be equal to, or greater than 3 devices of the specified lot [3].

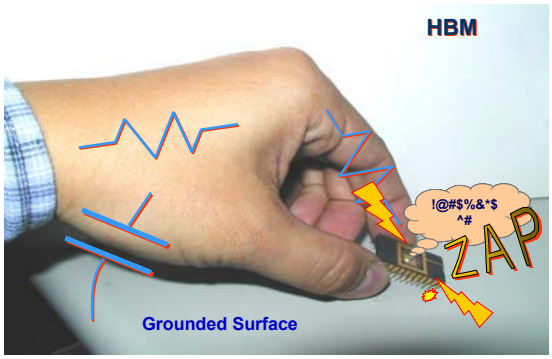

Fig. 2 A real case of human-body-model (HBM) ESD stress on a packaged IC.

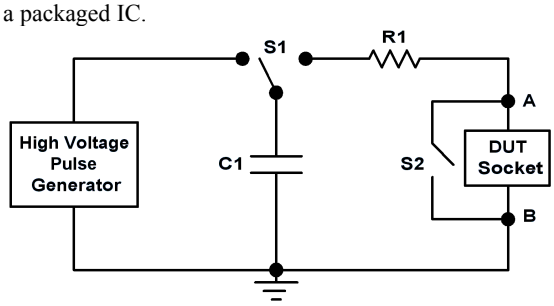

Fig. 3 The equivalent circuit of the HBM ESD event with R1= 1500ohm and C1= 100pF.

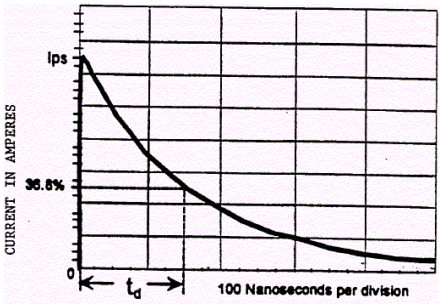

Fig. 4 Definition of the HBM pulse decay time (td).

The primary HBM standards are MIL-STD-883D method 3015.7 notice 8 [2], JESD22-A114-B [1], ESDA STM5.1-1998 [3], and AEC-Q100-002-REV-C. A 500 ohm measurement is added in JESD22-A114-B and ESDA STM5.1-1998 to ensure the stray capacitance of the system is minimized.

2.1 MIL-STD-883D method 3015.7 notice 8

The MIL-STD-883 method 3015.7 notice 8 is the first device level ESD test method. Its waveform definition is changed from voltage to current (Tektronix CT-1) waveform. It perhaps is the last HBM standard released by US military, because MIL-STD is going to take the EDSA HBM standard in the future.

2.2 ESDA STM5.1-1998

The ESDA STM5.1-1998 was developed in early 90's to eliminate the flaws in MIL-STD-883, and its most recent re-release was updated in 1998. HBM Device Testing Working Group is working on efforts with JEDEC to develop a joint ESDA/JEDEC HBM standard. In addition, the group's work on test procedures for validating HPC (High Pin Count) device testing on a small pin count tester is awaiting the results of additional testing before analyses can be performed. Additional work on the effects of the test socket capacitance is under the WIP (Work In Process) phase.

2.3 JEDEC EIA/JESD22-A114-B

The JEDEC EIA/JESD22-A114-B was developed to eliminate the flaws in MIL-STD-883, but different from ESDA STM5.1-1998 (zap interval). The most recent re-release was updated in June 2000, and its WIP is to work together with ESDA on the HPC test methods (effects of testing the HPC device on smaller pin count testers) [1].

3. MACHINE MODEL (MM)

The equivalent circuit diagram of MM ESD event is shown in Fig. 5 [4], which is used to replicate the machine ESD events on semiconductor devices. Fig. 6 shows the waveform specifications of the 400-V MM ESD pulse [4], generated by the MM ESD tester. The commercial IC is requested to sustain at least 200-V MM ESD stress. A 200-V MM ESD event can generate an ESD current peak of ~3.5Amp with a rise time of ~10ns. The ESD damage on IC caused by the MM ESD stress is similar to that caused by the HBM ESD stress, but it occurs at a significantly lower voltage. Typically, the ratio between HBM ESD robustness and MM ESD robustness of the same IC product is about 8 ~ 12.

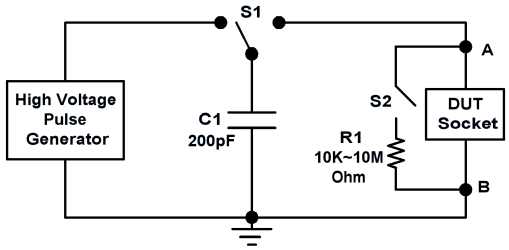

Fig. 5 The equivalent circuit of MM ESD event.

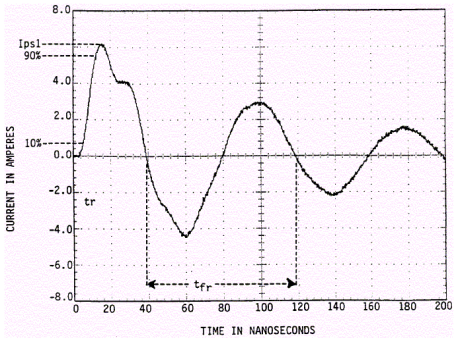

Fig. 6 Current waveform of 400-V MM ESD voltage discharging through a short wire.

The primary MM standards are known as JEDEC EIA/JESD22-A115-A [4], ESDA STM5.2-1999 [5], and AEC-Q100-003-REV-C. The sample size of the MM ESD test at each pin combination should be equal to, or greater than 3 devices of the specified lot [4], [5].

3.1 JEDEC EIA/JESD22-A115-A

The JEDEC EIA/JESD22-A115-A was developed and released in 1994 for eliminating flaws in the EIAJ test method. The most recent re-release was updated in October 1997 [4].

3.2 ESDA ESD STM5.2-1999

The ESDA ESD STM5.2-1999 was developed in early 90's, and the most recent re-release was updated in 1999. ESDA MM Device Testing Working Group reviewed the results of additional round-robin testing using a reduced number of pulses per stress level (1 pulse instead of 3). The results obtained thus far reveal inconsistent failure thresholds. Further investigation into waveform parameters revealed large variations while meeting standard requirements. The group is summarizing the test information into a technical report that it hopes to finalize in this year.

4. CHARGED-DEVICE MODEL (CDM)

The CDM ESD event is schematically drawn with the device cross-sectional view in Fig. 7. In this CDM ESD event, the ESD static charges are initially stored in the body of a floating IC, as that shown in Fig. 7. Most of the CDM charges are initially stored in the body (the whole p-substrate) of a CMOS IC. When some pin of this charged IC is touched by an external ground, the stored charged will be discharged from the inside of IC to the outside ground. The CDM ESD test method are shown in Fig. 8. In Fig. 8(a), the IC is initially charged by the filed-induced method without the socket, and then discharging through a grounded metal probe. In Fig. 8(b), the IC is initially charged by the direct connection to the high voltage source through the IC socket, and then discharging through the switch and the socket of tester to ground. Fig. 9 shows the waveform specifications of the CDM ESD pulse. The commercial IC is requested to sustain at least 1-kV CDM ESD stress. The typical 1-kV CDM ESD event from a charged IC (with an equivalent 4pF capacitance to ground) can generate a current peak as high as ~15A within a rise time of only ~200ps. With such so large ESD current and so fast transition time, the I/O devices in CMOS IC's are totally destroyed by such ESD currents.

The primary CDM standards are ESDA STM5.3.1-1999 and JEDEC JESD22-C101-A [6]. The original CDM waveform and subsequent test system was developed by AT&T Bell Labs in the mid 80's. This architecture and waveform was the basis for the development of the JEDEC JESD22-C101-A. Besides, the ESDA began development on its own method (ESD STM5.3.1 & ESD STM5.3.2).

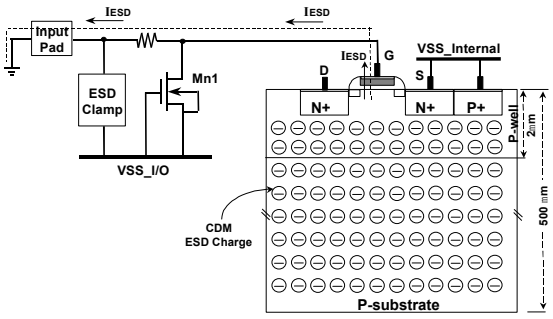

Fig. 7 The charged-device-model (CDM) ESD static charges initially stored in a floating IC and then discharging through a suddenly grounded pin.

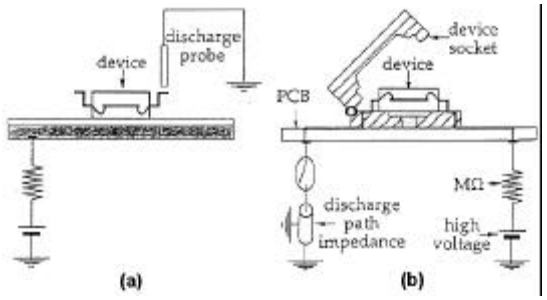

Fig. 8 CDM ESD testing models: (a) Field-induced (non-socketed) Model, and (b) Socketed Discharge Model.

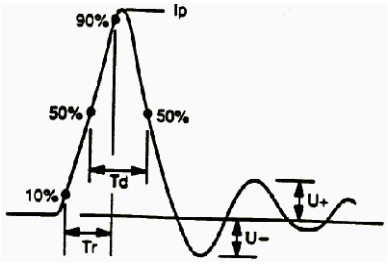

Fig. 9 CDM ESD current waveform.

4.1 JEDEC JESD22-C101-A

The JEDEC JESD22-C101-A, which AT&T still has a strong voice on its development, was updated in June 2000 for the most recent re-release. Both JEDEC and ESDA are working together for recent questions/ concerns on the size of the charge plate vs. the size of the ground plane and the number of zaps evaluated for a possible change.

4.2 ESDA STM5.3.1-1999

The ESDA STM5.3.1-1999 was developed in early 90's as a method to eliminate flaws in the JEDEC JESD22-C101-A, and the most recent re-release was updated in 1999. The WIP are: new modules will allow the use of a 1GHz oscilloscope; recent questions/ concerns on charge plate vs. ground plane sizes; and both JEDEC and ESDA work together for above concerns. Moreover, the CDM device testing working group decided to further conduct additional round-robin tests using 3 modules with capacitances of 6.8 pF, 35 pF, and 55 pF. Previous testing was performed with 10 pF and 35 pF modules only. The current draft standard specifies with the capacitances of 4 pF and 30 pF [7].

4.3 SDM (Socketed Discharge Model)

The SDM ESD tester is shown in Fig. 8(b). The primary SDM standard is the ESDA DS5.3.2, which is frozen, because it's based on only one developed system's architecture. ESDA SDM Device Test Working Group completed its technical report on SDM testers and began brainstorming its next steps. The group is planning an industry survey focusing on the need for a second-generation SDM tester.

5. ESD ZAPPING WAVEFORMS

To clearly observe the transient waveforms of the device under HBM/MM ESD tests, a ggNMOS (gate-grounded NMOS) fabricated in 0.25-μm CMOS process with device W/L of 300/0.7(μm/μm) was tested by HBM/MM ESD tester. The corresponding device breakdown I-V curve and ESD transient voltage/current waveforms are measured by Tektronix 370A Curve Tracer and TDS3000 oscilloscope, respectively.

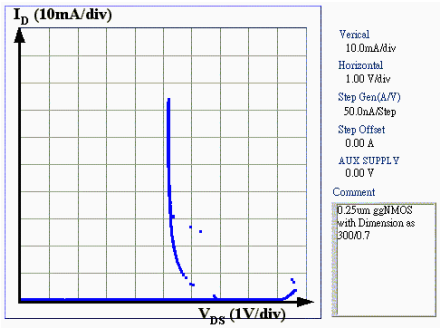

Fig. 10 The measured I-V curve of the ggNMOS device with W/L = 300/0.7(μm/μm), fabricated in a 0.25-μm CMOS process.

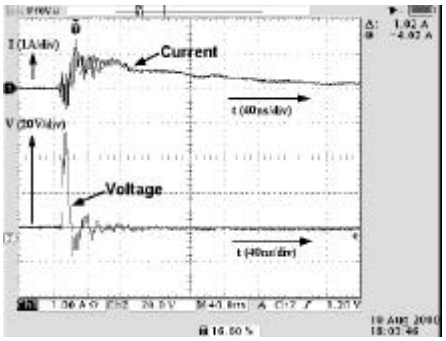

Fig. 11 The HBM current and voltage waveforms on the ggNMOS under the 2-kV HBM ESD test.

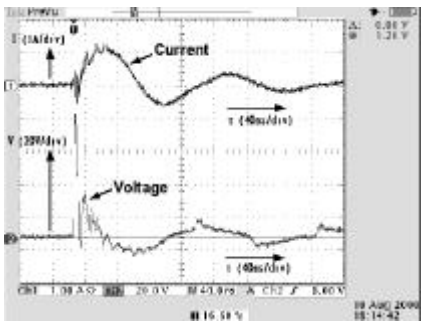

Fig. 12 The MM current and voltage waveforms on the ggNMOS under the 200-V MM ESD test.

The drain of the ggNMOS was as the pin under zapping, and the gate/source were both connected to the ground line. The breakdown I-V curve of the ggNMOS measured by Tektronix 370A Curve Tracer is shown in Fig. 10, where the first breakdown voltage is about 9.5V, and the snapback holding voltage is about 5.8V. The related HBM and MM current/voltage waveforms, measured by Tektronix TDS3000 oscilloscope, are shown in Fig. 11 and Fig. 12, respectively.

In Fig. 11, the upper curve is the current waveform of the ggNMOS under 2-kV HBM ESD zapping with a current peak of 1.5A and a decay time of 150ns, which are both within the specifications of the EIA/JESD22-A114-B standard. The related voltage waveform is shown at the bottom curve of Fig. 11 with a voltage peak of 55V. The current/voltage waveforms of the ggNMOS under 200-V MM ESD zapping are shown in Fig. 12. The upper curve is the current waveform with a peak current of 1.2A and a resonance frequency of 6.8MHz. The lower curve is the voltage waveform with a peak voltage of 76V.

6. CONCLUSION

The ESD standards released by ESDA & JEDEC are commonly used to verify the component-level ESD robustness of IC products by the semiconductor industry. After ESD zapping, dynamic/static function test and leakage current on the DUT are both necessary to ensure whether the DUT is damaged by the ESD stress, or not. To meet ESD robustness specifications of IC products, on-chip ESD protection circuits must be added into every IC chip to achieve a whole-chip ESD protection design [8].

7. REFERENCES

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