LAYOUT DESIGN ON MULTI-FINGER MOSFET FOR ON-CHIP ESD PROTECTION CIRCUITS IN A 0.18-μM SALICIDED CMOS PROCESS

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ABSTRACT: The layout design to improve uniform ESD current distribution in multi-finger MOSFET devices for better ESD robustness is investigated in a 0.18-μm salicided CMOS process. The multi-finger MOSFET, without adding the pick-up guard ring inserted into its source region, or with the vertical direction of power line connection, can sustain a higher ESD level. The layout of I/O cell can be drawn more compactly, but still to provide deep-submicron CMOS IC's with higher ESD robustness.

1. INTRODUCTION

With the shallower junction and much thinner gate oxide of MOSFET devices, electrostatic discharge (ESD) issue has become a main reliability concern of integrated circuits (IC's) in sub-quarter-micron CMOS technology. To sustain a reasonable ESD stress (typically, ±2kV in the human-body-model [1] ESD event) for safe mass production, on-chip ESD protection circuits have to be added into the IC products. The typical on-chip ESD protection circuits used for input, output, and power pads are shown in Fig.1 [2]. In order to sustain the desired 2-kV ESD level, each ESD-protection MOSFET in the ESD protection circuits often has a total channel width of several hundreds micrometer (μm). With such a large device dimension for ESD protection, the MOSFET devices in ESD protection circuits are often drawn in the multi-finger structure to save layout area of the I/O cells. However, the layout area for I/O cells in the high-pin-account IC is critically limited. To further reduce the occupied layout area of the I/O cells with the ESD protection devices, the staggered layout style for I/O cells has been widely used in the high-pin-account CMOS IC products. The I/O cells in staggered layout style are shown in Fig.2, where each cell pitch is only 50 μm. With such a limited layout area in the staggered I/O cells, the layout efficiency of ESD protection devices to sustain high ESD robustness becomes more important in the high-pin-account IC products.

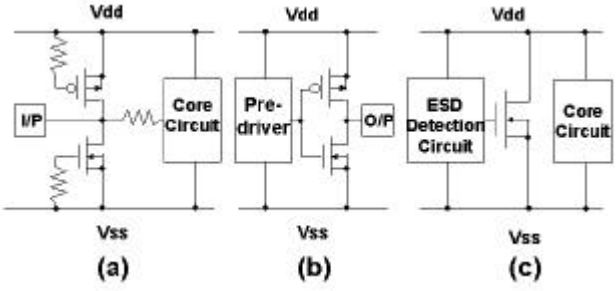


Fig.1 The typical on-chip ESD protection circuits for, (a) input pad, (b) output pad, and (c) power rails, of a CMOS IC.

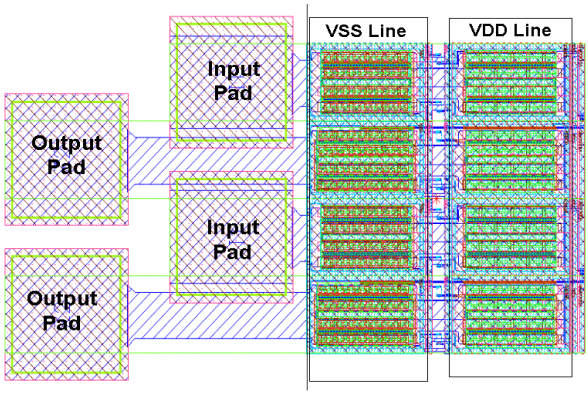


Fig.2 Layout example of four I/O cells drawn in the staggered style in a CMOS IC.

In this paper, layout efficiency of ESD protection devices in multi-finger structure for providing high ESD robustness within limited layout area is investigated in a 0.18-μm salicided CMOS process. Especially, the impact of inserted pick-up guard rings and the direction of power line connection on ESD robustness of the multi-finger MOSFET is first reported in the literature.

2. LAYOUT STRUCTURE OF MOSFET

The layout parameters such as channel length, total channel width, each finger width, spacing from drain contact to poly-gate edge, and so on, have obvious influence on ESD robustness of multi-finger MOSFET devices [3]-[5]. When the gate-grounded NMOS is under ESD zapping, the parasitic lateral bipolar in NMOS device structure will be triggered into its snapback region. If one of the parallel multiple fingers is first triggered on during ESD zapping, the ESD current is mainly discharged through the first turned-on finger. Such non-niform turn-on issue on multi-finger MOSFET often decreases its ESD robustness [6], even if the MOSFET has a large enough device dimension.

However, even if the layout of multi-finger NMOS is drawn uniformly, the equivalent substrate resistance of the central finger is still largest because the distance from its channel region to the guard ring is longest in layout. Thus, the central finger of the multi-finger NMOS is often turned on early than the other fingers to cause the non-uniform turn-on issue. In order to solve this non-uniform turn-on problem, the additional pick-up guard ring (inserting into each source region of the multi-finger NMOS layout) was reported to improve ESD robustness in a 0.35-μm CMOS technology [7]. The P+ pick-up guard ring inserted into the source region of a multi-finger NMOS device is shown in Fig.3.

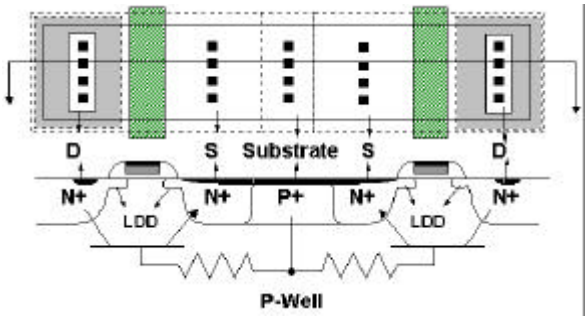


Fig.3 The layout top view and device cross-sectional view of the NMOS device with additional pick-up guard ring inserted into its source region.

Table 1
The four different devices drawn in the test chip with different numbers of the additional pick-up guard ring inserted into the source region in a 0.18-μm CMOS process.

	Gate-oxide thickness, tox (Å)	W/L (μm/μm)	ESD implantation
3.3V_NMOS	68	480/0.5	Born + As.
1.8V_NMOS	32	480/0.33	Born
3.3V_PMOS	68	480/0.45	None
1.8V_PMOS	32	480/0.28	None

To further verify the impact of the additional pick-up guard rings on the ESD robustness of multi-finger MOSFET devices, four device layout structures with different numbers of the P+ (N+) pick-up guard rings inserted into source regions of multi-finger NMOS (PMOS) devices are drawn in Fig.4. In Fig. 4(a), it is the typical layout structure of multi-finger MOSFET without any additional pick-up guard ring inserted into the source region. In Fig. 4(b), there is one additional pick-up guard ring inserted into the central source region (called as one NPN structure for NMOS, or one PNP structure for PMOS). In Fig. 4(c), there is one NPN (PNP) structure between every four fingers, and totally it has two NPN (PNP) structures in the multi-finger MOSFET layout. In Fig. 4(d), there is one NPN (PNP) structure in every source region, and totally it has five NPN (PNP) structures in the multi-finger MOSFET layout.

Each multi-finger NMOS (or PMOS) device has 12 parallel fingers in Fig.4, and every finger is drawn with a finger length of 20μm. So, the total channel width for each multi-finger NMOS (or PMOS) device is 480μm. For mixed-voltage applications, this 0.18-μm salicided CMOS process also provides two different gate-oxide thickness of 68 Å and 32 Å on both the NMOS and PMOS devices for operating with 3.3V and 1.8V power supplies, respectively. Therefore, four multi-finger devices with different gate-oxide thickness or different channel length are drawn and tested with different numbers of the P+ (N+) pick-up guard rings into their source regions. The four multi-finger devices with different gate-oxide thickness or different channel length are listed in Table 1. The ESD implantation on NMOS has been generally used to enhance ESD robustness of NMOS in sub-micron CMOS processes [8].

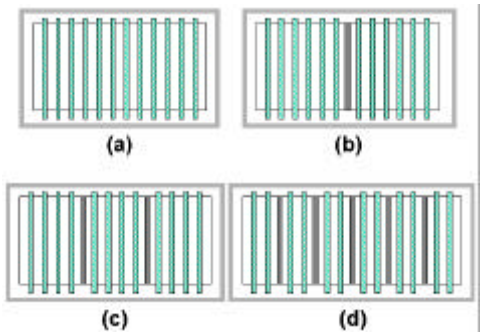


Fig.4 The layout top view of the multi-finger MOSFET with different numbers of additional pick-up guard rings inserted into source region, called as NPN (PNP) structures in NMOS (PMOS) devices. (a) NPN (PNP) = 0, (b) NPN (PNP) = 1, (c) NPN (PNP) = 2, and (d) NPN (PNP) = 5.

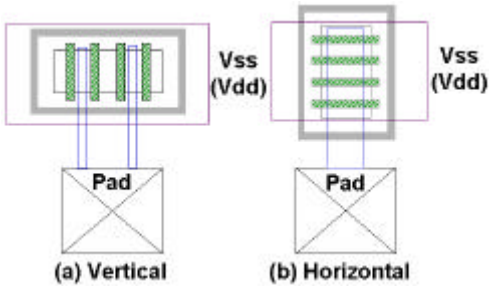


Fig.5 The layout of the multi-finger MOSFET with (a) vertical, and (b) horizontal, direction of the power line connection.

In the staggered I/O cells, the layout area for ESD protection devices is further limited, as seen in Fig.2. The power metal lines (VDD and VSS) connected to the ESD protection devices may be drawn in the vertical or horizontal directions to reduce the total layout area of an ESD-protection MOSFET with the specified device dimension. The different directions of power line connection to the multi-finger MOSFET devices may have an impact on its ESD robustness. To further verify this layout effect on ESD robustness of the multi-finger MOSFET devices, two different layout styles of power line connection are shown in Fig.5. In Fig. 5(a), the VSS (VDD) power line connected to the source of NMOS (PMOS) is vertical to the poly-gates of the multi-finger MOSFET, where the ESD current can uniformly flow from the pad to the drain region of every finger. On the other hand, in Fig. 5(b), the VSS (VDD) power line connected to the source of NMOS (PMOS) is horizontal to the poly-gates of the multi-finger MOSFET, where the ESD current could first turn on the finger near to the pad to cause the non-uniform turn-on issue among the multiple fingers of the MOSFET. In Fig. 5(a) and 5(b), the MOSFET's (for 3.3-V NMOS and 3.3-V PMOS) are drawn with 12, 20, 24, or 36 parallel fingers in the test chip, and each finger has the same finger length of 20μm. All of the test chips to investigate the impact of the inserted pick-up guard rings and the direction of power line connection on ESD robustness of the multi-finger MOSFET devices had been fabricated in a 0.18-μm salicided CMOS process with additional silicide-blocking mask on the drain region of every finger.

3. EXPERIMENTAL RESULTS

The curve tracer Tek370 is used to measure the dc I-V curves of the fabricated MOSFET devices for investigating their first breakdown voltage (Vt1), the parasitic lateral bipolar trigger current (It1), and the holding voltage (Vh) of snapback breakdown. The second breakdown current (It2) and HBM ESD level are measured to investigate ESD robustness of the fabricated MOSFET devices. The second breakdown current (It2) and voltage (Vt2) are measured by the transmission line pulse generator (TLPG) with a pulse width of 100 ns. The HBM ESD level is measured by a *Zapmaster* ESD tester. ESD failure criterion is defined as the ESD zapping voltage to cause the leakage current on devices greater than 1μA under the corresponding VDD bias.

3.1 Effect of the additional pick-up guard rings

Fig.6 shows the measured dc I-V curves of the 3.3V gate-grounded NMOS (ggNMOS) with four different numbers of additional pick-up guard rings, as those shown in Fig.4. From Fig.6, the parasitic lateral bipolar trigger current (It1) and the snapback breakdown holding voltage (Vh) of the gate-grounded multi-finger NMOS can be found and compared in Fig.7. When the numbers of NPN structures are increased, the It1 and Vh are also increased. The base resistance of the parasitic lateral bipolar is reduced by the increase of the additional pick-up guard rings (NPN structures), where the distance between the channel region to the substrate contact becomes shorter. With an increased trigger current (It1), the parasitic lateral bipolar in the multi-finger MOSFET becomes more difficult to be triggered on. With an increased snapback breakdown holding voltage (Vh), the power dissipation generated by ESD current on the multi-finger MOSFET becomes higher. From the measured device I-V curves, the multi-finger MOSFET with increased NPN (PNP) structures is predicted to have a lower ESD level.

The dependences of It2 and HBM ESD level on different numbers of NPN (PNP) structures in the layout of multi-finger MOSFET are measured and compared in Fig. 8(a) and 8(b), respectively. For 3.3V ggNMOS and 3.3V gate-Vdd PMOS devices, the numbers of the NPN (PNP) structures do not have a noticeable influence on the ESD robustness. But, in the 1.8V ggNMOS and the 1.8V gate-Vdd PMOS devices, the ESD robustness is obviously degraded when the numbers of NPN (PNP) structures in the multi-finger MOSFET are increased. These experimental results are quite different to the previous study in [7]. With both verifications by the TLPG-measured It2 and the HBM ESD level, the increase of NPN (PNP) structures has been confirmed to cause a low ESD robustness on multi-finger MOSFET. From such experimental results, the pick-up guard ring inserted into the source region is not recommended to draw the layout of MOSFET devices with multiple fingers. Without adding the pick-up guard ring inserted into the source region, the layout area for the multi-finger MOSFET can be further reduced. Therefore, the staggered I/O cell can be realized with more compact silicon area and higher ESD robustness in IC products.

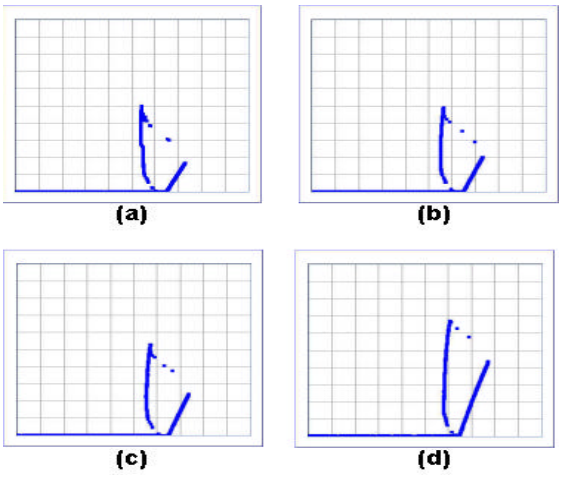


Fig.6 The measured dc I-V curves of the fabricated 3.3V ggNMOS for (a) NPN = 0, (b) NPN = 1, (c) NPN = 2, and (d) NPN = 5, with the same total device dimension of W/L = 480/0.5 (μm/μm). (X-axis: 1V/div.; Y-axis: 20mA/div.)

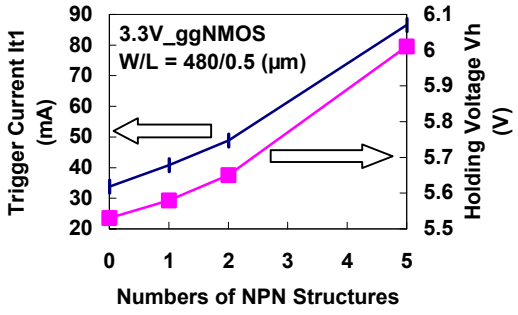
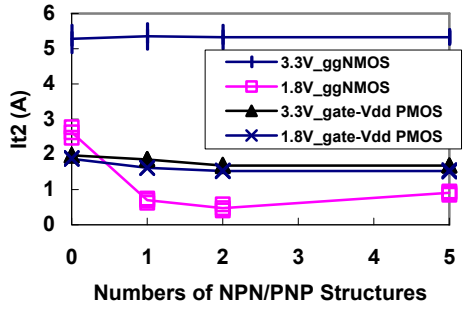
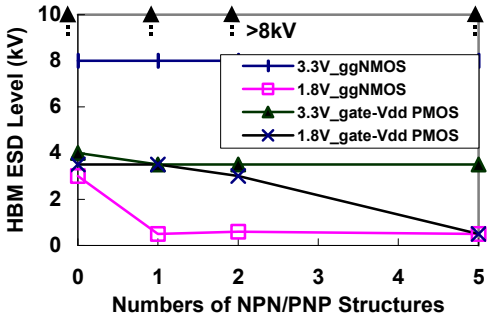


Fig.7 The parasitic lateral bipolar trigger current (It1) and the snapback breakdown holding voltage (Vh) of the 3.3V multi-finger ggNMOS under different numbers of NPN structures.



(a)

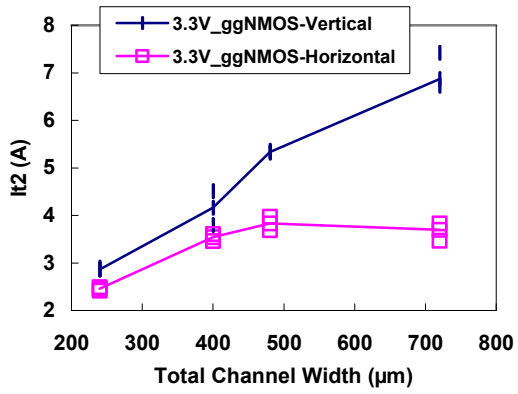


(b)

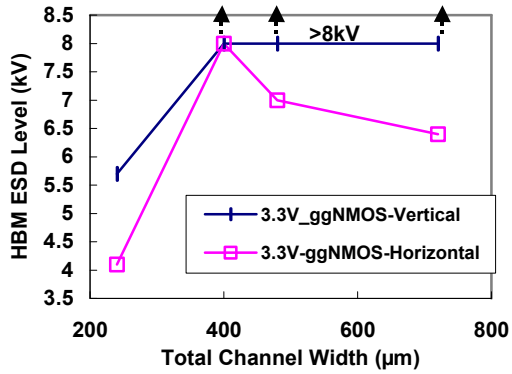
Fig.8 Dependence of (a) It2, and (b) HBM ESD level, on different numbers of NPN (PNP) structures in the layout of multi-finger NMOS (PMOS).

3.2 Effect of vertical / horizontal power line connection

The snapback breakdown holding voltage (Vh) of NMOS is lower than its trigger voltage (Vt1), as that shown in Fig.6. If one of multiple fingers in the NMOS layout is triggered on first, the other fingers will not be turned on until its drain voltage is larger than Vt1 again. This often causes non-uniform current distribution among the multiple fingers of MOSFET. Therefore, the ESD robustness of multi-finger MOSFET can not be linearly and continually increased by the increase of total channel width. The vertical or horizontal directions of power line connection in device layout could cause such non-uniform turn-on effect on the multi-finger MOSFET.



(a)



(b)

Fig.9 Dependence of (a) It2, and (b) HBM ESD level, on the total channel width of 3.3V ggNMOS with vertical or horizontal power line connection.

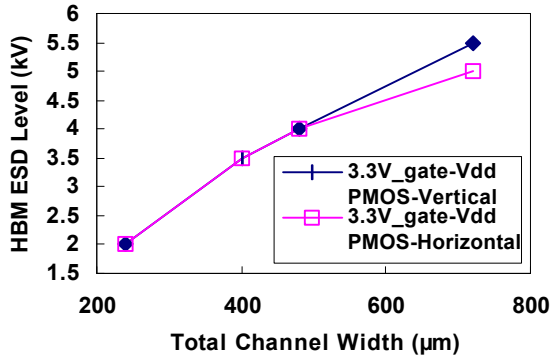


Fig.10 Dependence of HBM ESD level on the total channel width of 3.3V gate-Vdd PMOS with vertical or horizontal power line connection.

The It2 and HBM ESD level of the 3.3V ggNMOS with vertical or horizontal power line connection and different total channel width are compared in Fig. 9(a) and 9(b). From Fig.9, there is an obvious decrease on ESD robustness of the multi-finger MOSFET with horizontal power line connection in the layout, when total channel width becomes large. From these experimental results, it has confirmed that the multi-finger MOSFET realized in the layout with horizontal power line connection easily causes the non-uniform turn-on phenomenon among the multiple fingers of MOSFET.

Fig.10 shows the dependence of HBM ESD level on the total channel width of 3.3V gate-Vdd PMOS with vertical or horizontal power line connection. The non-uniform turn-on issue in Fig.10 is not serious as that in Fig.9 of NMOS device, because the PMOS has no obvious snapback after drain breakdown. However, the ESD level of multi-finger PMOS is still slightly degraded, when the total channel width of PMOS is increased larger than 600 μm. Therefore, in the compact I/O cell layout, the multi-finger MOSFET is recommended to be drawn with a vertical power line connection for sustaining a higher ESD level.

4. CONCLUSION

The impact of layout styles on ESD robustness of multi-finger MOSFET in a 0.18-μm salicided CMOS process has been experimentally investigated in details. From the experimental results, the pick-up guard ring inserted into the source region is not recommended in the layout of multi-finger MOSFET devices. Moreover, the multi-finger MOSFET drawn with a vertical power line connection has a higher ESD level than that drawn with the horizontal style.

5. REFERENCES

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