Whole-Chip ESD Protection Strategy for CMOS Integrated Circuits in Nanotechnology

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Abstract

On-chip electrostatic discharge (ESD) protection circuits had been built in IC chips to protect the devices and circuits against ESD damage. But, ESD protection circuits constructed with the scaled-down CMOS devices are very weak to ESD stress. Therefore, novel ESD protection solutions must be developed to overcome this reliability challenge for integrated circuits fabricated in the nano-scale CMOS technology. In this paper, the whole-chip ESD protection strategy for CMOS integrated circuits in nanotechnology has been proposed with two main methods. One is the substrate- triggered circuit technique used to effectively improve ESD robustness of devices in the nano-scale CMOS technology. The other is the novel design concept of "ESD Buses" used to solve the internal ESD damage issue of CMOS IC with multiple and separated power lines. The internal circuits or interface circuits, realized by nano-scale CMOS devices, are more sensitive to such internal ESD damage issue. By using ESD buses, ESD current can be quickly discharged far away from the internal circuits or interface circuits of CMOS IC to achieve the goal of whole-chip ESD protection.

1. Introduction

CMOS devices, especially realized with the nano-scale gate oxide thickness in the sub-quarter-micron CMOS technology, are very sensitive to electrostatic discharge (ESD) events. ESD level of commercial IC products had been generally requested to be higher than 2kV in the HBM (human body model [1]), and 1kV in the CDM (charged device model [2]) ESD stresses.

The typical ESD event for the real-case HBM ESD stress is shown in Fig.1. The ESD static charges are initially stored in the body of a human, and then transfer into the IC, when the finger of a human touches the IC in the way shown in Fig.1. The ESD event for the CDM ESD stress is schematically drawn with the device cross-sectional view in Fig.2. In this CDM ESD event, the ESD static charges are initially stored in the body of a floating IC, as that shown in Fig.2. Most of the CDM charges are initially stored in the body (the whole p-substrate) of a CMOS IC. When some pin of this charged IC is touched by an external ground, the stored charges will be discharged from the inside of IC to the outside ground. For the HBM ESD event with a charged 2000-V human body, its ESD current discharging waveform is shown in Fig.3(a), where it has a current peak of ~1.3A and a rise time of 5~10ns [1]. The typical 1000-V CDM ESD event from a charged IC (with an equivalent 4pF capacitance to ground) can generate a current peak as high as ~15A within a rise time of ~200ps [2], which is shown in Fig.3(b). With such so large ESD current and so fast transition time, the I/O devices in CMOS ICs are totally destroyed by such ESD currents.

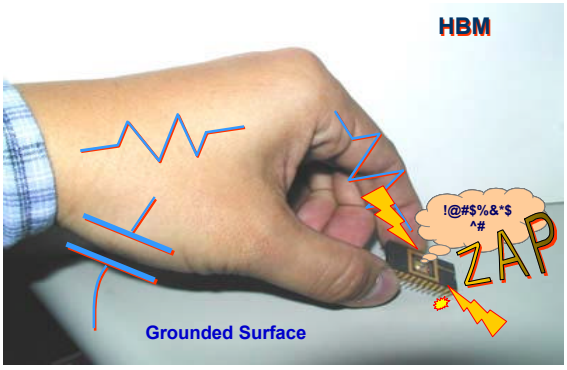


Fig.1 A real case of human-body-model (HBM) ESD stress on a packaged IC.

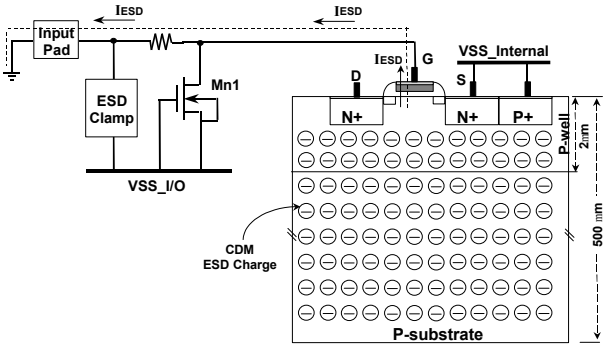
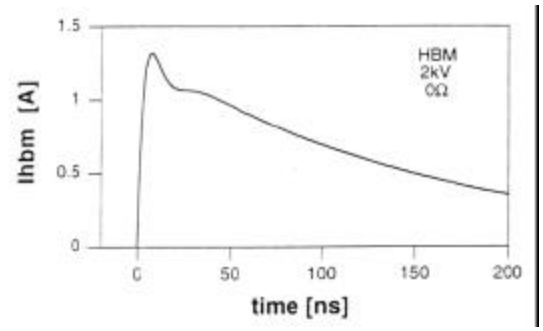
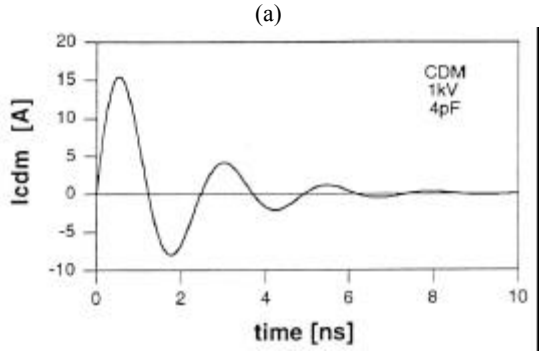


Fig.2 The charged-device-model (CDM) ESD static charges initially stored in a floating IC and then discharging through a suddenly grounded pin.

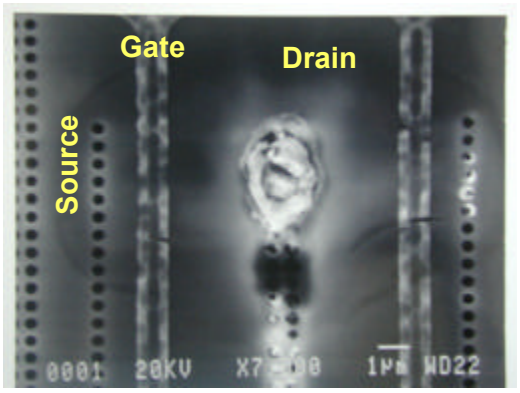


(a)

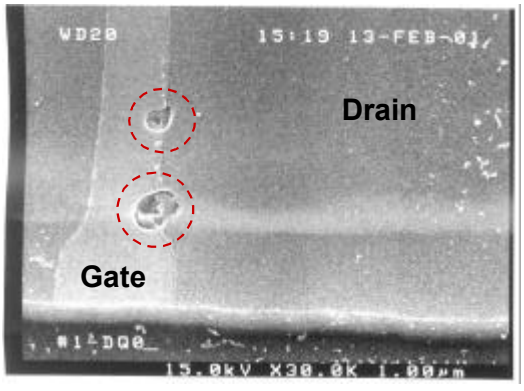


(b)

Fig.3 The ESD current waveforms generated from (a) a 2000-V HBM ESD event, and (b) a 1000-V CDM ESD event with a 4pF capacitance.



(a)



(b)

Fig.4 The failure pictures of CMOS ICs after (a) HBM, and (b) CDM, ESD stresses.

The typical failure pictures on output buffers of CMOS ICs fabricated by a 0.18-μm CMOS process are shown in Fig.4(a) after HBM, and Fig.4(b) after CDM, ESD stresses. Therefore, on-chip ESD protection circuits must be built into the IC chip to protect the devices and circuits against ESD damage. However, on-chip ESD protection circuits constructed with such nano-scale CMOS devices are very difficult to meet the general ESD specification of HBM 2kV (CDM 1kV) for commercial IC products. This ESD reliability issue has become the top-one serious problem to product CMOS ICs in any sub-quarter-micron CMOS technology. Therefore, some novel ESD protection solutions must be developed to overcome this reliability challenge on ESD protection.

In this paper, the whole-chip ESD protection strategy for CMOS integrated circuits in sub-quarter-micron CMOS technology is proposed.

2. Substrate-Triggered Technique

To sustain the requested ESD level without causing damage in IC, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices in ESD protection circuits are often realized by finger-type layout to save total layout area [3]. But, during ESD stress, the multiple fingers of ESD protection NMOS cannot be uniformly turned on. Only several fingers of the NMOS were turned on and therefore damaged by ESD [4]. The EMMI photography on the turn-on behavior of a gate-grounded NMOS (W/L= 300μm/0.35μm) under a 40mA drain pulse current stress is shown in Fig.5. Only some regions of the center fingers in this gate-grounded NMOS are turned on. Because the short-channel NMOS has an obvious snapback effect on its I-V curve, as that shown in Fig.6. The turned-on center fingers of Fig.5 will cause ESD current crowding on those fingers. If the turned-on region cannot be extended to full regions of all fingers before second breakdown occurs in the NMOS device, ESD current will be mainly discharged through this turned-on region. This often causes a low ESD level, even if the NMOS has a large device dimension.

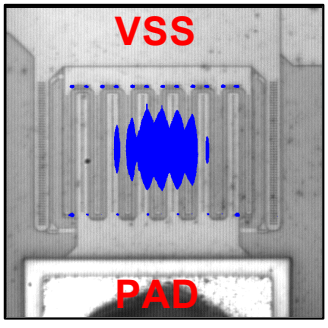


Fig.5 The EMMI photography on the turn-on behavior of a gate-grounded NMOS under 40mA current pulse stress.

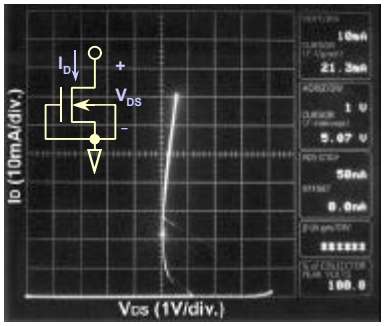
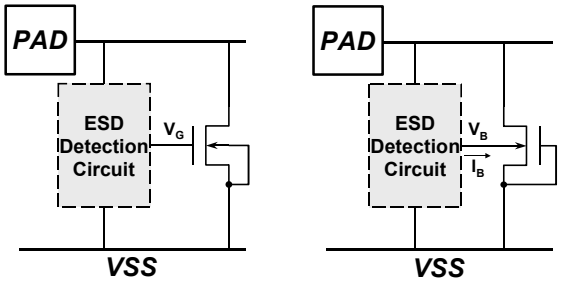


Fig.6 The snapback I-V curve of a gate-grounded NMOS device with a channel length of 0.35μm.



(a) (b)

Fig.7 The circuit designs with (a) the gate-driven technique, and (b) the substrate-triggered technique, to improve ESD robustness of ESD protection circuits.

To improve the turn-on uniformity among the multiple fingers, the gate-driven design [4]-[6] and substrate-triggered design [7]-[11] had been reported to increase ESD level of the large-device-dimension NMOS. The circuit schematic diagrams are shown in Fig. 7(a) and 7(b), respectively. In Fig.7(a), an ESD detection circuit is connected between the pad and the gate of NMOS. In Fig.7(b), the ESD detection circuit is connected between the pad and the bulk of NMOS. In the normal circuit operation condition, the V_G in Fig.7(a) is kept at zero to turn off the channel of NMOS, and the V_B in Fig.7(b) is kept at ground to turn off the parasitic lateral BJT in the NMOS device. There are two main current paths in the MOSFET device structure to discharge ESD current. One is the channel current of MOSFET, the other is the turn-on current of parasitic lateral BJT. In the gate-driven design, ESD current is mainly discharged through the surface channel of MOSFET. In the substrate-triggered design, ESD current is mainly discharged through the parasitic lateral BJT in the MOSFET device, which is far away from the surface channel of MOSFET. With a current path far from the surface channel, the ESD-generated heat can be more efficiently dissipated by the large volume of the substrate. Therefore, the substrate-triggered design can be more effective to improve ESD robustness of the ESD protection devices, as comparing to the gate-driven design.

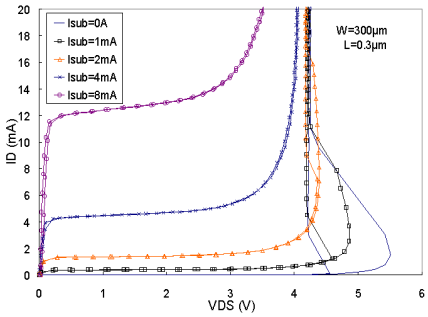


Fig.8 The I-V curves of the substrate-triggered NMOS under different substrate current biases.

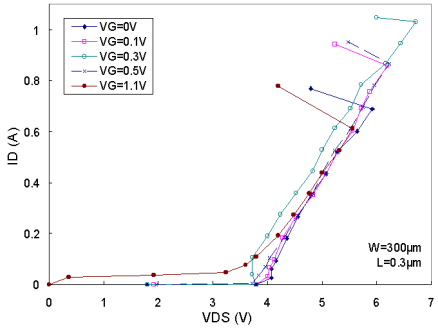


Fig.9 The TLPG-measured I-V curves of the traditional finger-type NMOS under different gate biases.

The I-V curves of a substrate-triggered NMOS fabricated in a 0.18-μm CMOS process under different substrate biases are measured and shown in Fig.8. The TLPG (transmission line pulse generator) with a pulse width of 100nS is used to find the It2 (second breakdown current) of the NMOS devices under different gate or substrate biases. The TLPG-measured I-V curves of NMOS under different gate and substrate biases are shown in Fig.9 and Fig.10, respectively. The dependence of It2 on the gate and substrate biases is shown in Fig.11 and Fig.12, respectively.

As seen in Fig.11, It2 of the gate-driven NMOS is first increased when the gate bias is increased from 0V. But, the It2 is dropped suddenly, when the gate bias is greater than some critical value. In Fig.11, the NMOS with a W/L of 300/0.3 under 0.8-V gate bias has an It2 even smaller than that under 0-V gate bias. This implies that the gate-driven design is no longer suitable for using to improve ESD robustness of NMOS devices in the nano-scale CMOS technologies. In Fig.12, the It2 of substrate-triggered NMOS can be continually increased when the substrate current is increased without sudden degradation. As comparing the It2 values of the NMOS with the same channel width of 300μm in Fig.11 and Fig.12, the It2 of substrate-triggered NMOS is two times greater than that of gate-driven NMOS. This verifies the effectiveness of the substrate-triggered technique to improve ESD robustness of ESD protection devices.

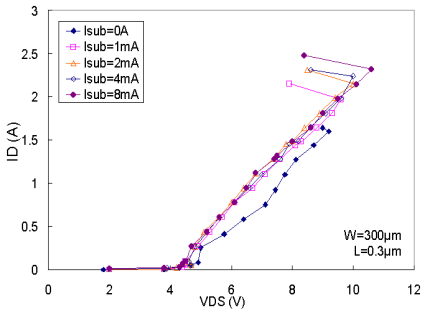


Fig.10 The TLPG-measured I-V curves of the substrate-triggered NMOS under different substrate current biases.

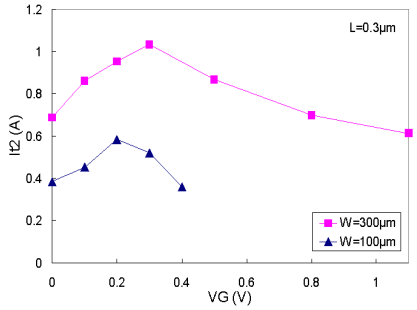


Fig.11 The dependence of It2 on the gate bias of the traditional finger-type NMOS.

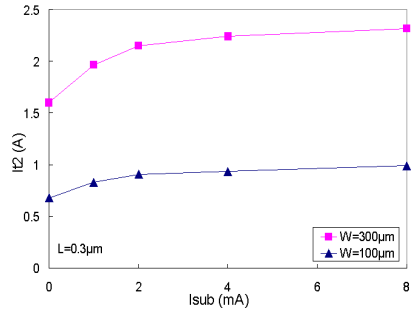


Fig.12 The dependence of It2 on the substrate current bias of the substrate-triggered NMOS.

To explain the effect of substrate-triggered design, the energy band diagrams in the NMOS with different substrate- triggered biases under ESD stress at drain side are illustrated in Fig.13. The cross-sectional view of NMOS device is shown in Fig.13(a). Energy bands across some positions in the NMOS device structure, along the A-A', B-B', and C-C' lines in Fig.13(a), are analyzed and drawn in Fig.13(b), 13(c), and 13(d) under different substrate biases (V_{BS}=0, V_{BS}>0, and V_{BS}>>0). The energy band diagrams of substrate-triggered devices can be lowered as those shown in Fig.13(c) and 13(d), where the gate bias of MOSFET is held on ground. The substrate bias can lower energy bands in the substrate and extend the effective current flow region S. This current flow region S through the lateral BJT is far away from the surface channel. A device, with more current flow region in its device structure, has more space to dissipate the ESD-generated heat. So, substrate-triggered devices can sustain higher ESD robustness. Therefore, the device triggered by substrate bias can have a much higher ESD level [12].

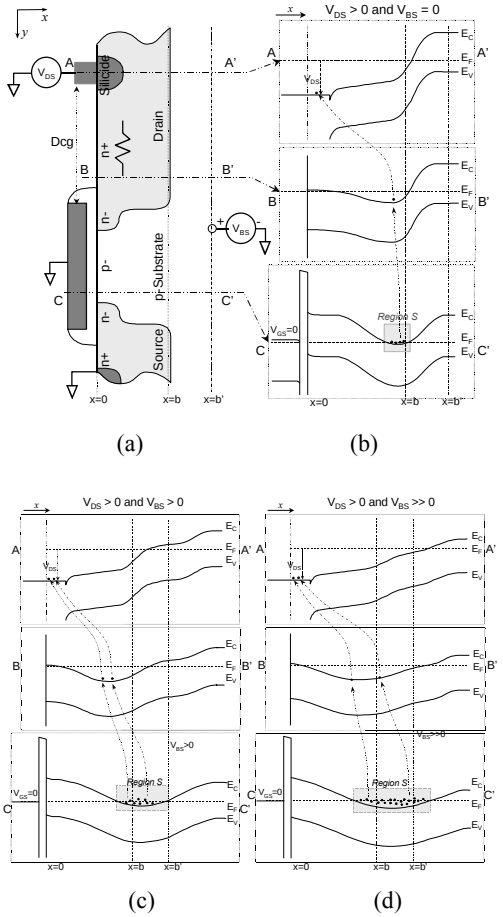
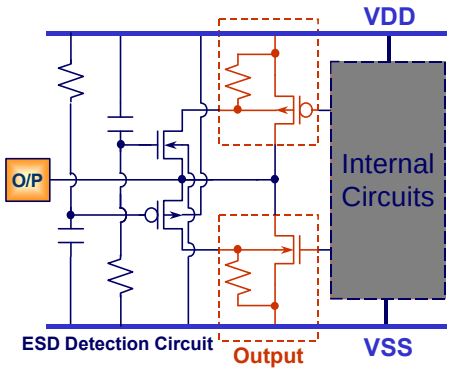


Fig.13 Illustration on the energy band variations of NMOS device under different substrate-triggered operations.

To effectively improve ESD robustness of I/O devices in the nano-scale CMOS technology, the substrate-triggered circuit design on a CMOS output buffer is shown in Fig.14(a). The experimental results verified in a 0.18-μm salicided CMOS process are shown in Fig.14(b), which have proven that the proposed substrate-triggered technique can effectively increase HBM ESD level of output NMOS from the original 0.8kV to become >3kV. In Fig.15, the EMMI micro-photography's on the turn-on behaviors of an NMOS under ESD stress with substrate-triggered design are demonstrated. With the substrate-triggered design, NMOS during high-current ESD stress can be very uniformly turned on, therefore its ESD robustness

can be effectively improved. The substrate bias can pull down the ESD current path far away from the surface of NMOS, therefore this substrate-triggered technique can significantly improve ESD robustness of CMOS ICs in the nano-scale CMOS technology.



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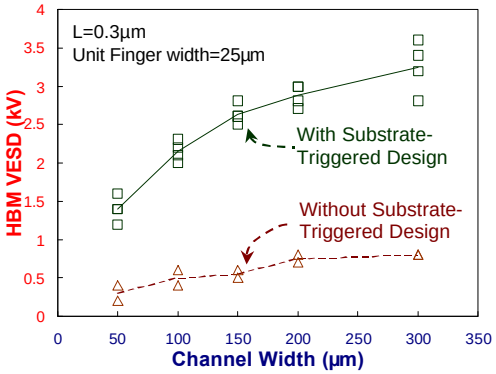
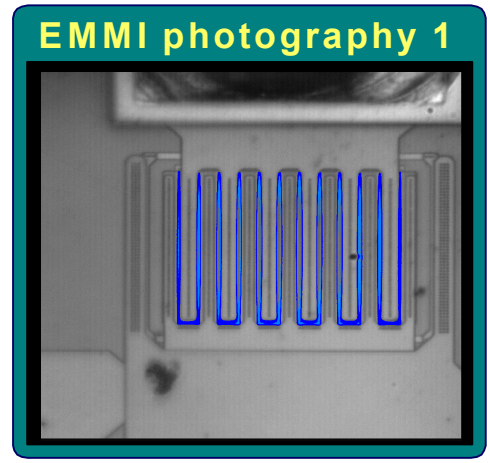


(b)

Fig.14 (a) The novel substrate-triggered circuit design to effectively improve ESD robustness of output devices in CMOS ICs. (b) Comparison on ESD robustness of output devices in a 0.18-µm CMOS process with or without the substrate-triggered design.

3. ESD Buses

Moreover, due to the considerations on the noise coupling issue and power dissipation issue, a high-integration giga-scale SoC chip often has multiple and separated power lines surrounding in chip layout. But, some unexpected ESD damages had been found to locate on the internal circuits or interface circuits between the circuit blocks of a CMOS IC with multiple and separated power lines, even if there are ESD protection circuits placed at the input, output, and power pins. The ESD current path flowing in a CMOS IC with separated power line is illustrated in Fig.16, where the interface circuits between two circuit blocks with different power lines are often damaged during pin-to-pin ESD stress. The internal circuits, realized in nano-scale CMOS technology, are more sensitive to such internal ESD damage issue. This causes a more difficult challenge to achieve effective on-chip ESD protection design.



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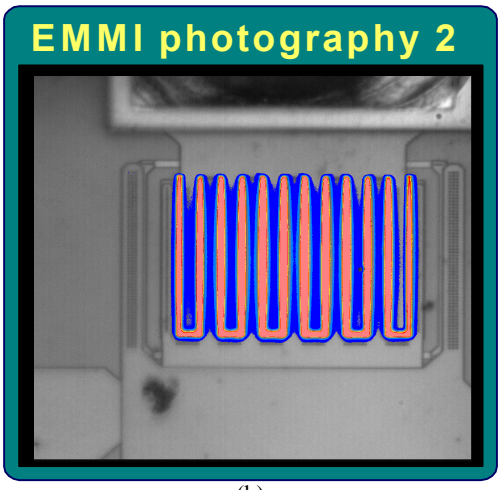

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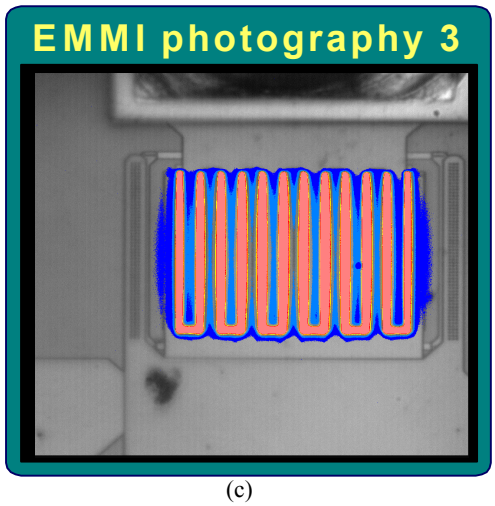

(c)

Fig.15 The EMMI micro-photography's on the turn-on behaviors of NMOS under ESD stress with substrate-triggered design. (a) low current stress, (b) middle current stress, and (c) high current stress.

In this work, another design concept of "ESD Buses" is shown in Fig.17 to generally solve such internal ESD damage issue in CMOS ICs. By using ESD buses, the ESD-stress current can be quickly discharged far away from the internal circuits or interface circuits of CMOS ICs. A simplified version of whole-chip ESD protection design with two ESD buses is shown in Fig.18, which has been practically used in some complex CMOS ICs to successfully achieve the HBM ESD level of >3kV [13].

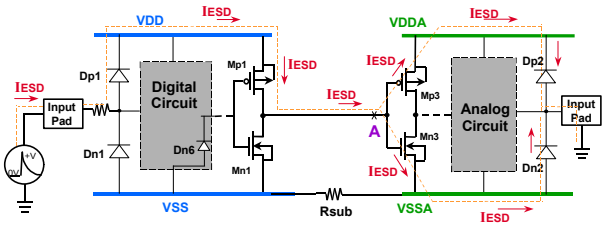

Fig.16 The ESD current path flowing in a CMOS IC with separated power line. The interface circuits between two circuit blocks with different power lines are often damaged during such pin-to-pin ESD stress.

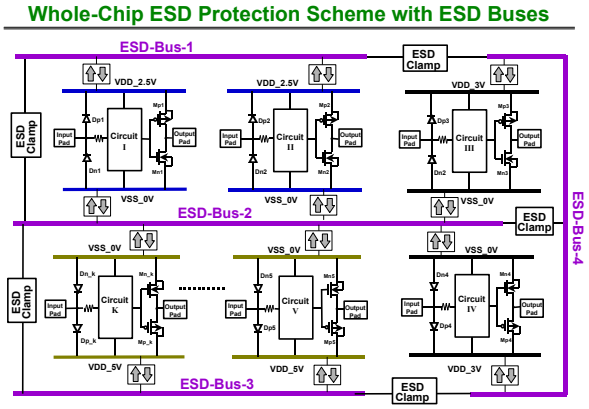

Fig.17 The novel ESD protection methodology by using ESD buses to protect the CMOS IC with multiple separated power lines in sub-quarter-micron CMOS technology.

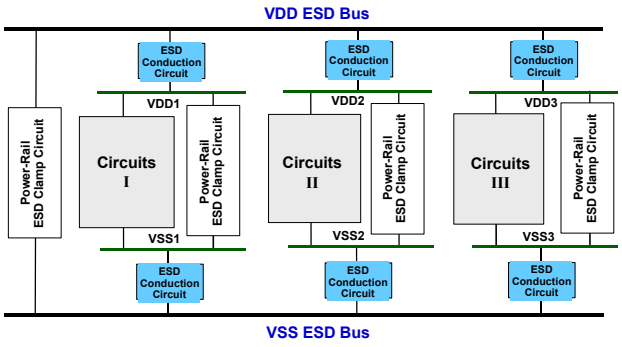

Fig.18 A simplified version of whole-chip ESD protection design in a CMOS IC with two ESD buses.

4. Conclusion

By using the proposed both substrate-triggered technique and ESD buses, ESD level of CMOS ICs realized in nano-scale CMOS technology can be successfully designed to meet the 2-kV HBM ESD specification. The power lines and ESD buses lines in the whole-chip IC layout should be drawn with wide enough metal width to quickly discharge ESD current away from the internal circuits.

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