ESD Implantations in 0.18-μm Salicided CMOS Technology for On-Chip ESD Protection with Layout Consideration

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1. Introduction

ESD robustness of CMOS devices used in the I/O pad becomes a main challenge on reliability issue, because the diffusion junction depth is reduced and LDD (lightly-doped drain) / salicide are generally used in sub-quarter-micron CMOS technology. In order to enhance ESD robustness, some ESD implantations had been reported for including into the process flow to modify the device structures for ESD protection [1]-[4].

The N-type ESD implantation is used to cover the LDD peak structure and to make a deeper junction in NMOS device for ESD protection [1]. The P-type ESD implantation located under the drain junction of NMOS is used to reduce the junction breakdown voltage and to earlier turn on the parasitic lateral BJT of the NMOS [2]. Because of the higher concentration than the P-well, the P-type ESD implantation can be also used to reduce the junction breakdown voltage of diode or field-oxide device, and to sustain higher ESD robustness under reverse-biased condition [3]. Moreover, both of the N-type and P-type ESD implantations are used in NMOS device to wish a higher ESD robustness [4]. Although there were some issued US patents to claim those process methods for realizing such different ESD implantations, the experimental comparison among those different ESD implantations for ESD protection in a same CMOS process was never reported in the literature before.

In this paper, the effectiveness of different ESD implantation solutions on NMOS and diode devices for ESD protection is investigated in a 0.18-μm salicided bulk CMOS process. The second breakdown current (It2) of the fabricated devices is measured by the transmission line pulse generator (TLPG). The human-body-model (HBM) and the machine-model (MM) ESD levels of these devices are also measured and compared. The layout dependence of NMOS devices and diodes with different ESD implantations are also investigated.

2. Devices with different ESD Implantations

Four types of the multi-finger gate-grounded NMOS (ggNMOS) structures in a 0.18-μm salicided CMOS process with different ESD implantations are shown in Fig.1, where the additional silicide-blocking mask is used to remove $CoSi_2$ silicide at both source and drain regions. In the device A, there is no ESD implantation in the source and drain side. In the device B, the boron (B) is used for the P-type ESD implantation under the drain side. In the device C, the arsenic (As) is used for the N-type ESD implantation under the drain side. The previous study had shown that the NMOS with As-implanted LDD has a higher ESD robustness than that with Phosphorus (P)- implanted LDD [5]. Therefore, the As is chosen for N-type ESD implantation in this study to get a better ESD level. In the device D, N-type As ESD implantation and P-type B ESD implantation are both used at the drain side. The process features of this 0.18-μm salicided bulk CMOS technology with different ESD implantations are summarized in Table I.

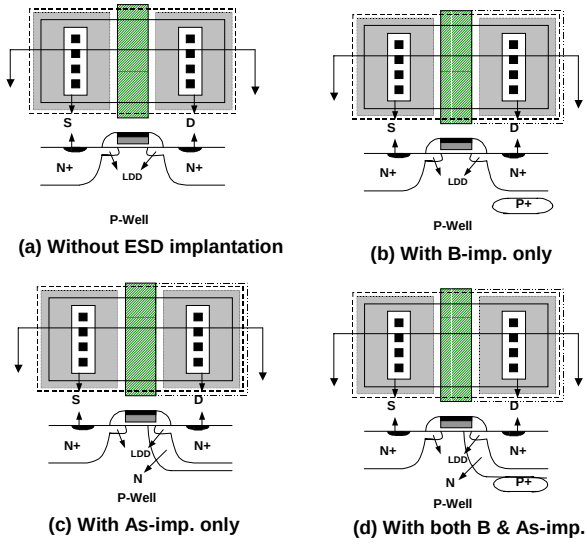


Fig. 1: The layout top view and device cross-sectional view of NMOS in (a) device A, (b) device B, (c) device C, and (d) device D, with different ESD implantations.

The diodes can be used as forward diode string or reverse breakdown device for on-chip ESD protection. The layout top view and the device cross-sectional view of the

diodes with different junction are shown in Fig.2, where the additional silicide-blocking mask is used to remove the silicide on the p/n diffusion of the diode for overcoming the STI (shallow trench isolation) boundary issue on the diode structure [6]. The device structure shown in Fig.2(a) is called as the P-type diode (Dp), that in Fig.2(b) is called as the N-type diode (Dn), and that in Fig.2(c) is called as the N-type diode (Dn) with boron (B) ESD implantation, respectively.

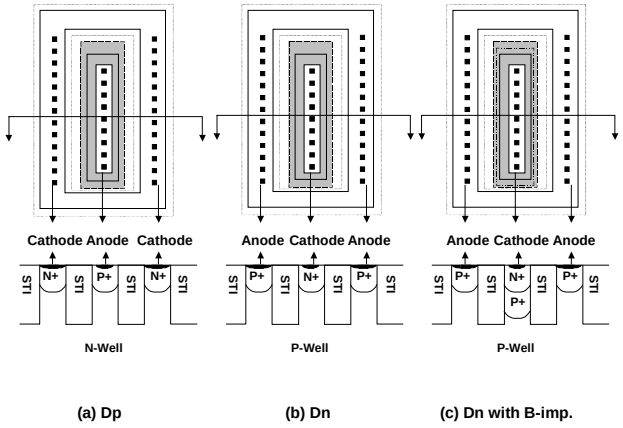


Fig. 2: The layout top view and device cross-sectional view for (a) P-type diode, (b) N-type diode, and (c) N-type diode with B ESD implantation.

Table I :
Process features of the 0.18-μm salicided CMOS process with different ESD implantations.

Gate Oxide Thickness (tox) for 3.3V N (P) MOS	68Å
Gate Oxide Thickness (tox) for 1.8V N (P) MOS	32Å
Dose Concentration of P-Type (B) ESD Implantation	5E13 cm^{-2}
Energy of P-Type (B) ESD Implantation	80keV
Dose Concentration of N-type (As) ESD Implantation	1E15 cm^{-2}
Energy of N-type (As) ESD Implantation	60keV
N-Well (P) Implantation	First: 700keV 3E13 cm^{-2} Second: 60keV 1.5E12 cm^{-2}
P-Well (B) Implantation	First: 300keV 3E13 cm^{-2} Second: 60keV 8E12 cm^{-2}
Silicide	$CoSi_2$

The curve tracer Tek370 is used to measure the dc I-V curves of devices for investigating the breakdown (trigger) voltage (Vt1) and the snapback holding voltage (Vh). The second breakdown current (It2) and voltage (Vt2) are measured by TLPG with a pulse width of 100ns. The ESD failure criterion of devices is defined, as the leakage current is greater than 1μA under the VDD bias of 3.3V. The PS-mode (positive-to-VSS) HBM ESD level (HBM V_{ESD}) and MM ESD level (MM V_{ESD}) are measured by *Zapmaster* ESD simulator to verify the correlation between It2 and HBM V_{ESD}, and to compare the ESD robustness under the HBM and MM ESD stresses.

3. Experimental Results

3.1 Multi-Finger GGNMOS with ESD-Imp.

The measured dc I-V curves of the 3.3-V ggNMOS devices with different ESD implantations are shown in Fig.3, where the doping concentration of B ESD implantation is 5E13 cm^{-2} and the implantation energy is 80keV. The device breakdown voltage (Vt1) is measured at the voltage when the current is 1mA for reference. The comparison on Vt1 among the four devices with different ESD implantations is shown in Fig.4. The Vt1 can be reduced from the original 10.4V to about 6.9V by using the B ESD implantation, and about 9.8V by using the As ESD implantation. The Vt1 and the snapback holding voltage (Vh) of the device D with both ESD implantations are about 6.5V and 5.96V, respectively.

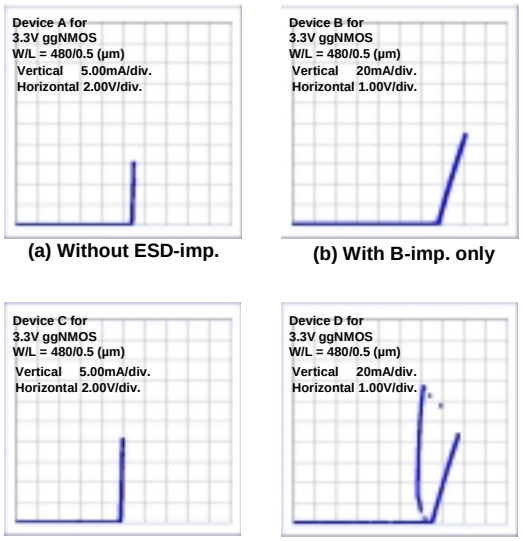


Fig. 3: The measured dc I-V curves of NMOS in the (a) device A, (b) device B, (c) device C, and (d) device D, under gate-grounded condition.

The TLPG-measured I-V curves of four NMOS devices are shown in Fig.5, and the It2 are compared in Fig.6. For the NMOS without any ESD implantation, the It2 is about 0.48A and Vt2 is about 6.68V. When the B ESD implantation is used, the It2 increases to 1.65A and Vt2 is about 7.18V. If the As ESD implantation is used, the It2 becomes 2.7A and Vt2 becomes 9.33V. If both ESD implantations are used, the It2 increases up to 5.33A and Vt2 is about 12.76V. This result has verified the

effectiveness of different ESD implantations for ESD protection.

Figs.7(a) and 7(b) show the HBM and MM ESD levels of the four devices in the PS-mode ESD stress condition. From the experimental results, the ESD implantations have a significant improvement on ESD level of ggNMOS, especially for the device with both B and As ESD implantations.

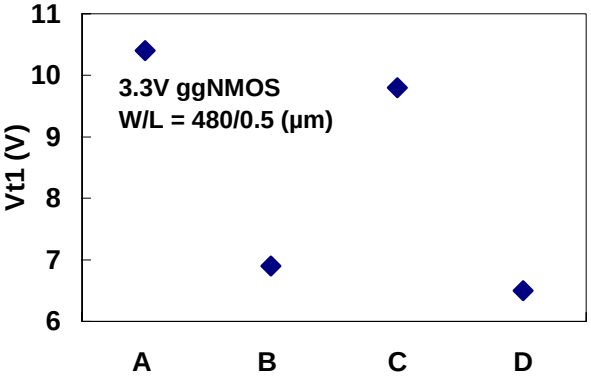


Fig. 4: The Vt1 defined at I=1mA of the 3.3V ggNMOS with different ESD implantations, whereas the four devices (A, B, C, and D) have the same W/L of 480μm/0.5μm.

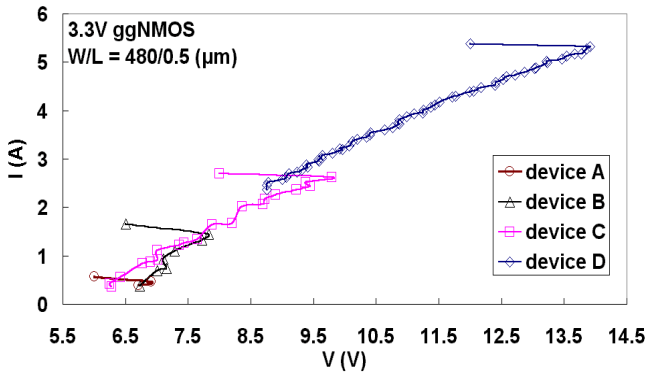


Fig. 5: The TLPG-measured I-V curves of the 3.3V gate-grounded NMOS with different ESD implantations.

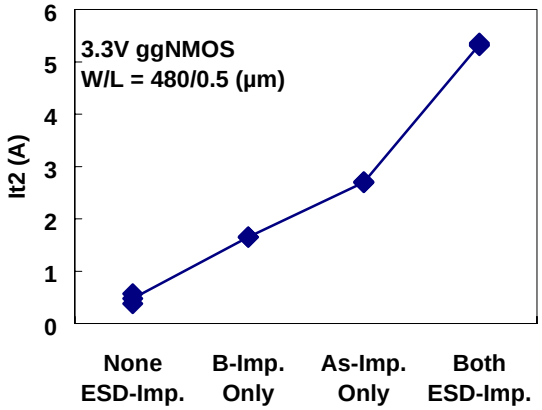
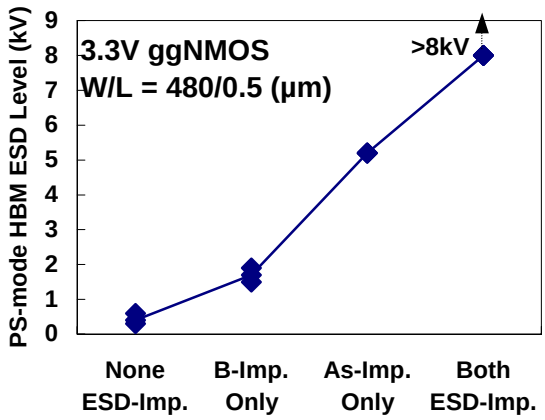
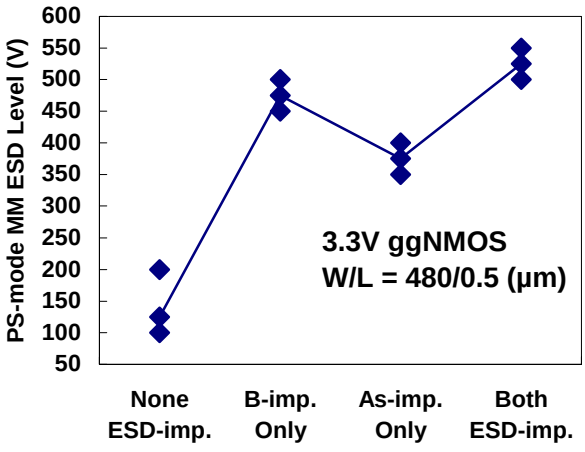


Fig. 6: The It2 of the 3.3V ggNMOS with different ESD implantations.



(a)



(b)

Fig. 7: The PS-mode ESD levels of the 3.3V ggNMOS with different ESD implantations under the (a) HBM, and (b) MM, ESD stresses.

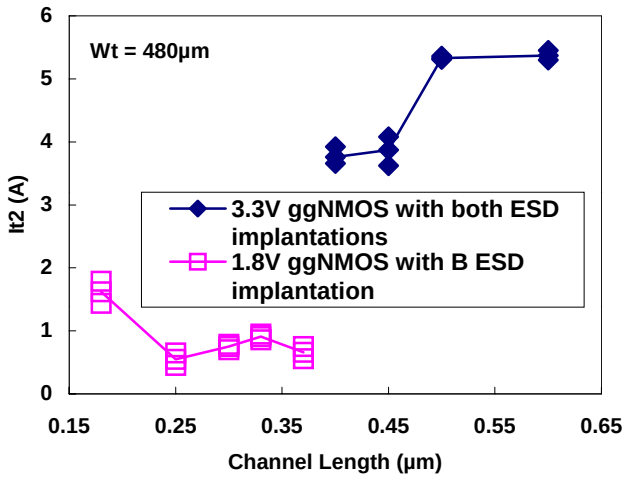


Fig. 8: The relation between It2 and channel length of ggNMOS with a total width of 480μm.

Fig.8 ~ Fig.10 compare the It2, HBM, and MM ESD levels of 3.3V and 1.8V ggNMOS's with different channel lengths (L), where the 3.3V devices have both B and As ESD implantations but the 1.8V devices have only the B ESD implantation. When the channel is short enough in the 1.8V devices, the turn-on efficiency of the lateral BJT in NMOS device is significantly improved. Therefore, the NMOS with shorter channel length can sustain a higher ESD level [7].

Fig.11 ~ Fig.13 compare the It2, HBM, and MM ESD levels of the 3.3V and 1.8V ggNMOS's with different total channel width (Wt). These devices are drawn with a fixed unit finger width of 20μm and different finger numbers to have different total channel widths. The 1.8V ggNMOS with Wt=720μm in Fig.12 still having a low ESD level is due to the non-uniform turn-on behavior among its multiple fingers [8].

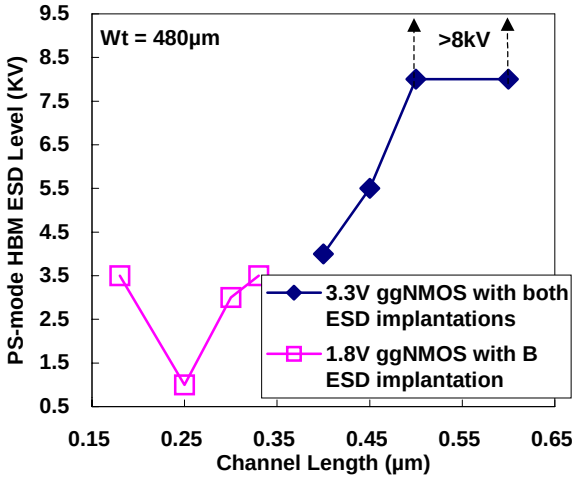


Fig. 9: The relation between PS-mode HBM ESD level and channel length of ggNMOS with a total width of 480μm.

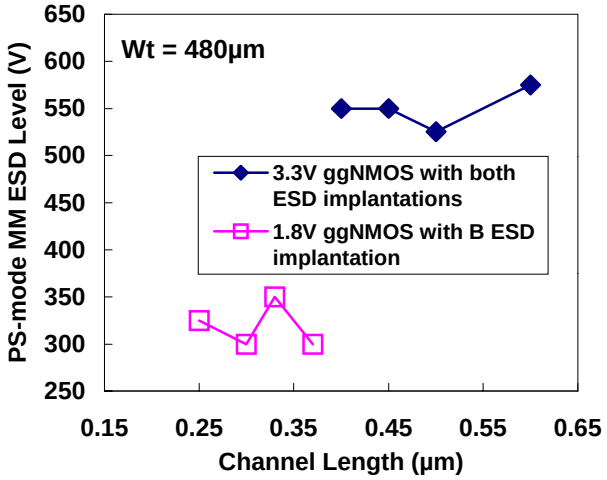


Fig. 10: The relation between PS-mode MM ESD level and channel length of ggNMOS with a total width of 480μm.

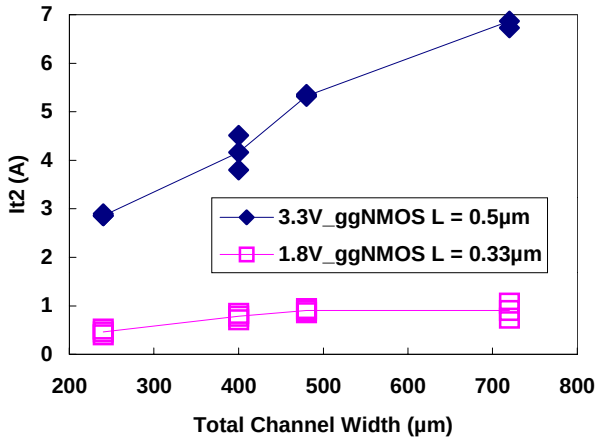


Fig. 11: Dependence of It2 on the total channel width of ggNMOS.

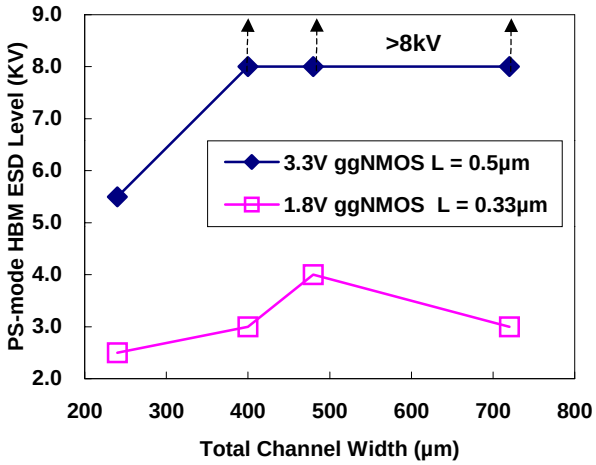


Fig. 12: Dependence of PS-mode HBM ESD level on the total channel width of ggNMOS.

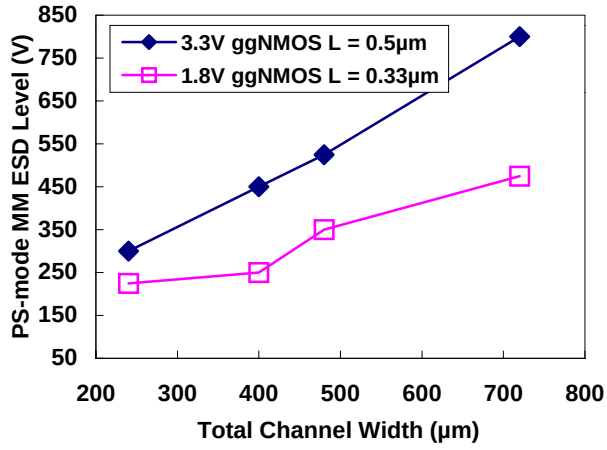


Fig. 13: Dependence of PS-mode MM ESD level on the total channel width of ggNMOS.

3.2 Diodes with B ESD-Imp.

The dc I-V characteristics of the diodes drawn in Fig.2 under reverse-biased condition are shown in Fig.14 with the B ESD implantation of dose concentration of 5E13 cm^{-2} and energy of 80keV. The breakdown voltages are also indicated in Fig.14. From the measured results, the additional B ESD implantation can effectively reduce the reverse junction breakdown voltage to only 6.1V. With a lower breakdown voltage, the power and heat under PS-mode ESD stress can be reduced. Therefore, the diode with the B ESD implantation is expected to have a higher ESD robustness.

The TLPG-measured I-V curves of these diodes under reverse-biased condition are shown in Fig.15. All the diodes in Fig.15 have the same total junction perimeter (Pt) of 120μm. The P-type diode under the ND-mode (negative-to-VDD) ESD stress is operated in the reverse-biased condition to discharge ESD current. The P-type diode under the PD-mode (positive-to-VDD) ESD stress is operated in the forward-biased condition to discharge ESD current. For the P-type diode Dp without any ESD implantation, the It2 is about 0.29A and Vt2 is about 20.95V. For the N-type diode Dn without any ESD implantation, the It2 is about 0.19A and Vt2 is about 29.59V. When the B ESD implantation is used on Dn, its It2 increases to 0.24A and Vt2 is lowered to 23.04V. The diode device with lower Vt2 and higher It2 can sustain a higher ESD stress. The It2 of the Dn with or without B ESD implantation in PS-mode ESD stress is compared in Fig.16. This experimental result has verified the effectiveness of boron ESD implantation on N-type diode for ESD protection under reverse-biased condition.

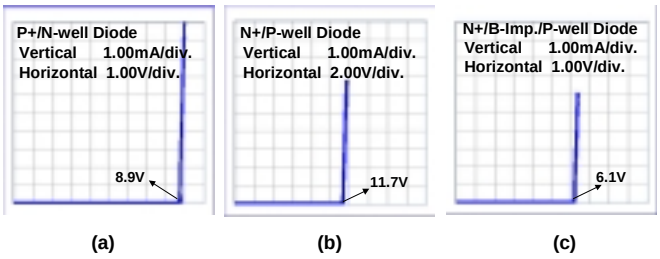


Fig. 14: The measured dc I-V curves of the (a) P-type diode, (b) N-type diode, and (c) N-type diode with B ESD implantation.

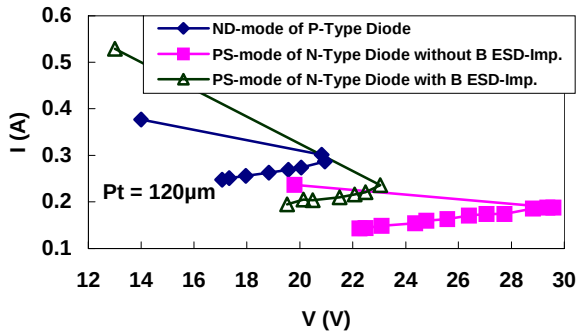


Fig. 15: The TLPG-measured I-V curves of the different diodes under reverse-biased condition.

Fig.17 shows the HBM ESD level of the N-type diodes under the PS-mode and NS-mode (negative-to-VSS) ESD stress condition. Under the PS-mode (NS-mode) ESD stress, the N-type diode is operated in the reverse-biased (forward-biased) condition to discharge ESD current. The N-type diode in NS-mode ESD stress can sustain HBM ESD level greater than 8kV, no matter the B ESD implantation is used or not. But, the N-type diode with a total junction perimeter of 120μm under the PS-mode ESD stress has a much lower HBM ESD level of only ~ 1kV.

Fig.18 and Fig.19 compare the It2 and HBM ESD level of the P-type diode and N-type diode (without ESD implantation) under different total junction perimeters. These diodes are drawn with a fixed unit finger perimeter of 40μm and different finger numbers from 1 to 3 to have different total junction perimeters. The non-uniform turn-on issue among the multiple fingers of ggNMOS is not observed in diodes. When the total junction perimeter of diode is increased, the It2 and ESD level of diode are almost linearly increased.

Fig.20 and Fig.21 compare the It2 and HBM ESD level of the diodes with different spacings from anode to cathode. The experimental results show that the It2 and HBM ESD level of the P-type diode and N-type diode (without B ESD implantation) under forward- and reverse-biased conditions are increased, when the anode-to-cathode spacing is increased.

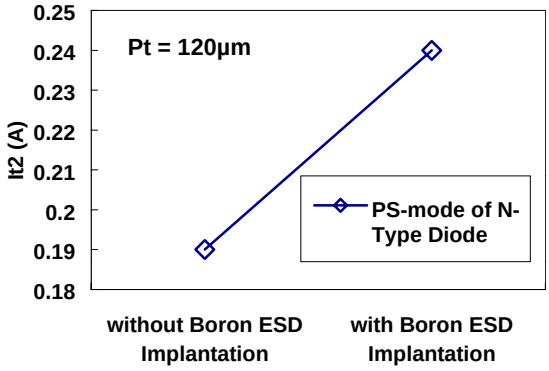


Fig. 16: The It2 of the N-type diode in reverse-biased condition with or without B ESD implantation.

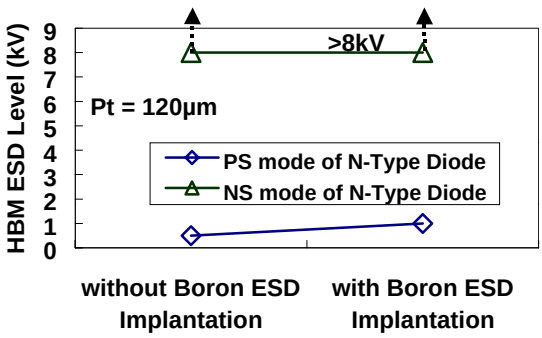


Fig. 17: The PS-mode and ND-mode HBM ESD levels of the N-type diodes with or without B ESD implantation.

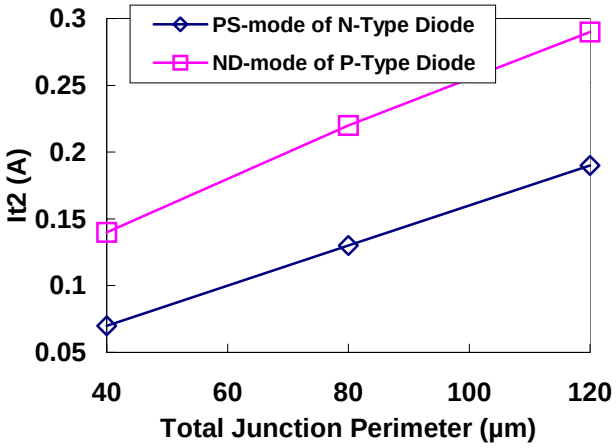


Fig. 18: Dependence of It2 on the total junction perimeter of diode under reverse-biased condition.

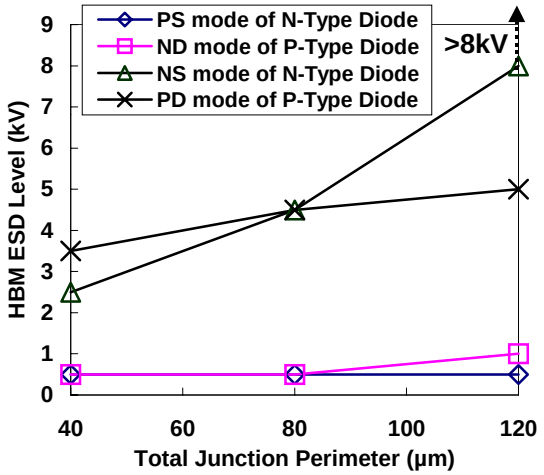


Fig. 19: Dependence of HBM VESD on the total junction perimeter of P-type and N-type diodes.

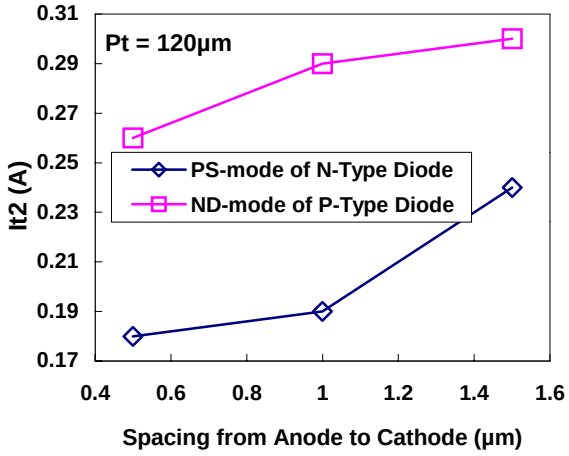


Fig. 20: The relation between It2 and the spacing from anode to cathode of diode with a total perimeter of 120μm under reverse-biased condition.

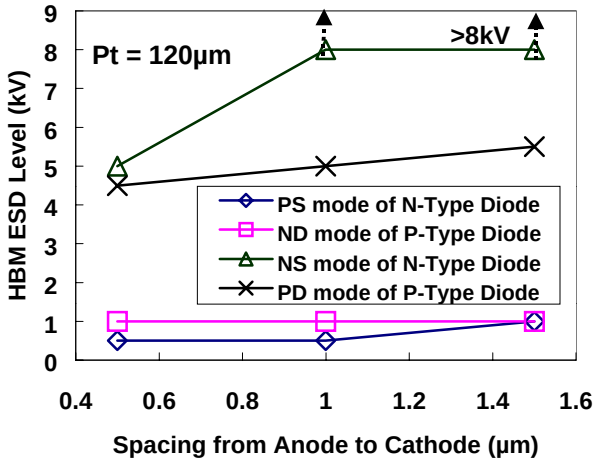


Fig. 21: The relation between HBM ESD level and the spacing from anode to cathode of diode.

4 Conclusion

The second breakdown current (It2) and ESD level of NMOS devices and diodes with different ESD implantations for on-chip ESD protection have been verified in a 0.18-μm salicided bulk CMOS technology. The significant improvement is observed when the NMOS is fabricated with boron or arsenic ESD implantations. Besides the process solution, the layout design on the NMOS and diode for ESD protection must be optimized to sustain a higher ESD level.

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