Novel Diode Structures and ESD Protection Circuits in a 1.8-V 0.15-μm Partially-Depleted SOI Salicided CMOS Process

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1. Introduction

Due to the low thermal conductivity of the buried oxide underneath the thin-film silicon layer and the shallow-trench-isolation (STI) structure on the insulating layer, electrostatic discharge (ESD) robustness of CMOS devices in Silicon-on-Insulator (SOI) CMOS technology had become a main reliability challenge [1]-[3]. As the SOI technology continues to be scaled down, the thickness of top layer silicon film will be decreased. The junction area for ESD protection devices to discharge ESD current becomes smaller. Therefore, the ability to dissipate the heat generated by ESD events in SOI CMOS IC's is seriously degraded.

Diode is one of the powerful devices for on-chip ESD protection due to its low trigger (cut-in) voltage, low turn-on resistance, and high ESD robustness. The typical ESD protection circuit with double diodes for I/O pad is shown in Fig. 1. To perform a diode structure of high ESD robustness in SOI CMOS process, the *Lubistor* diode was therefore invented for ESD protection in silicon-on-insulator (SOI) CMOS technology [4]. In order to sustain a high ESD stress and to provide an efficient protection for core circuits, the diode string of stacked configuration under forward-biased condition had been designed in the ESD clamp circuits [5]-[7]. Diode string used as ESD clamp device must be checked its leakage issue under forward-biased condition in bulk CMOS process [7], when IC is under normal circuit operation condition. Due to no parasitic vertical BJT structure in the p+/n-well diode realized in the SOI CMOS process, the stacked diodes in SOI technology can be designed with a lower enough leakage current for effective on-chip ESD protection.

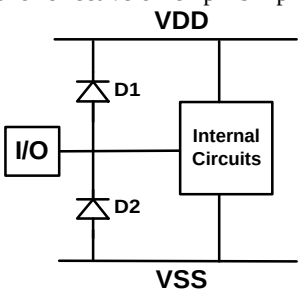


Fig. 1 The typical I/O ESD protection circuit constructed by double diodes in CMOS IC.

In this paper, two novel diode structures with effective larger p/n junction area for better heat dissipation in partially-depleted SOI CMOS technology are proposed. The I-V characteristics and ESD robustness of these new diodes are investigated and compared to that of *Lubistor* diode.

2. Diode Structures in SOI

Three kinds of diode structures are shown in Figs. 2(a) ~ 2(c), which are fully process-compatible to the general SOI CMOS technology. In Fig. 2(a), the device structure is called as *Lubistor* diode [4], which has a gate structure with both the n+ and the p+ implantations between the anode and cathode of the diode structure. In Fig. 2(b), the new proposed device structure is called as gated diode, which has an n-well/p-well junction instead of the n+/p-well junction in *Lubistor* diode. The n-well/p-well junction is located at the middle region under the polysilicon gate, which can be realized by layout design without extra mask layer or process step. In this new proposed structure, it has larger p/n junction area for better heat dissipation than *Lubistor* diode. In Fig. 2(c), another new device structure is called as non-gated diode, which is realized by independent n+ and p+ mask layers definition by layout drawing. The STI region between the anode and cathode in the non-gated diode structure is blocked by the active-region-definition mask layer. In this structure, the silicide-blocking mask layer is used to remove the silicide across the p/n junction of non-gated diode. Only by drawing different layout patterns on the related mask layers, these three diode structures can be realized and fabricated by the general SOI CMOS process without adding any extra mask layer or process step.

Such three diodes are fabricated in a 1.8-V 0.15-μm partially-depleted SOI salicided CMOS process to verify their ESD performance. The process features of this partially-depleted SOI salicide CMOS process used to verify these different diode structures are listed in Table I. The top thin-film silicon layer has a thickness of 1500Å. The thickness of the insulating layer, named as the buried oxide (BOX), is 1000Å. The gate oxide of 1.8V CMOS devices has a thickness of only 26Å. The n-well/p-well doping concentration is around 5E17cm^{-2}, and the p+/n+ source/drain doping concentration is about 10^{21} ~ 10^{22}cm^{-2}.

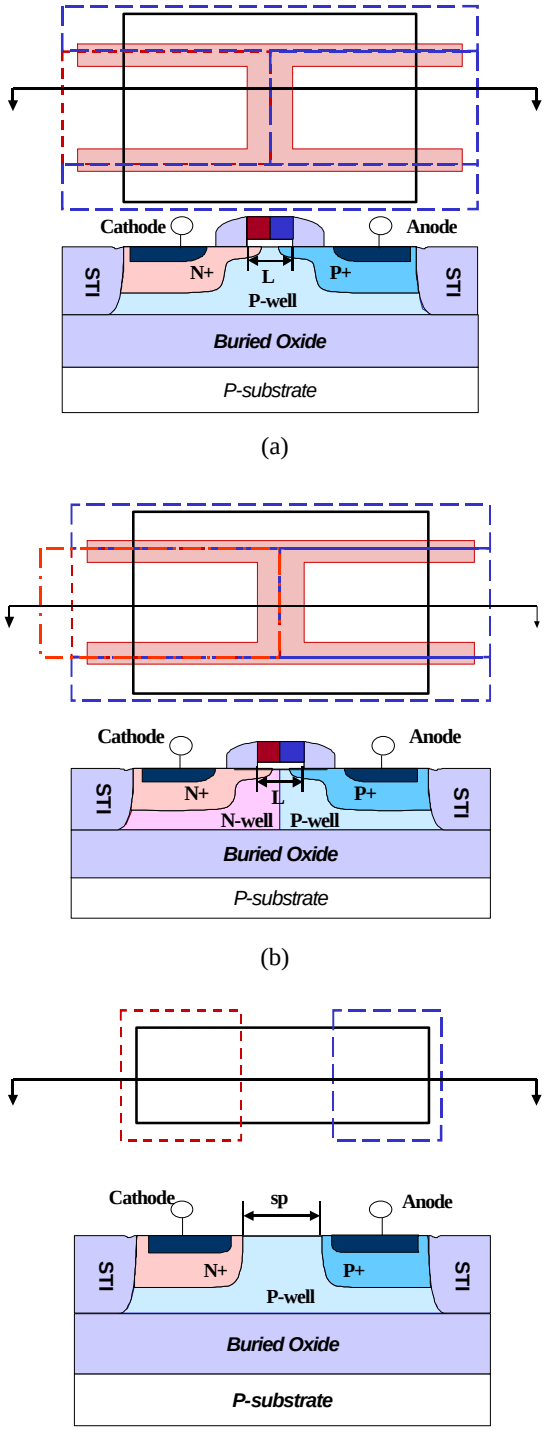


Fig. 2 The layout top view and device cross-sectional view for (a) *Lubistor* diode, (b) gated diode, and (c) non-gated diode, realized in a SOI CMOS process.

Table I
Process features of the 0.15-µm partially-depleted SOI salicide CMOS process.

Gate OxideThickness (thin, for 1.8V)	26 Å
NMOS / PMOS Threshold Voltage (Vtn/Vtp)	0.45V/0.5V
Buried Oxide (BOX) Thickness	1000 Å
Silicon Thickness on BOX	1500 Å
n+, p+ Doping Concentration	10^{21}~10^{22} cm^{-2}
N-well, P-well Doping Concentration	5E17 cm^{-2}

3. Experimental Results

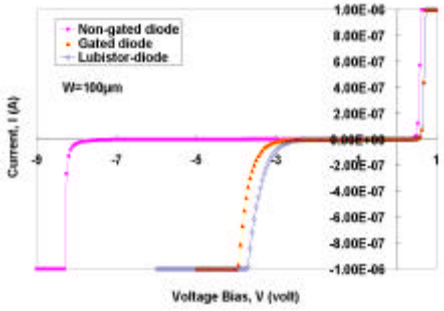
3.1. DC Characteristics

The dc characteristics of these three kinds of diodes are shown in Figs. 3(a) ~ 3(d). In Fig. 3(a), the gated and non-gated diodes have higher breakdown voltage than *Lubistor* diode under reverse-biased condition. The *Lubistor* diode is drawn with a gate channel length of L=0.5µm. The gated diode is drawn with a gate channel length of L=2µm. The non-gated diode is drawn with a anode-to-cathode spacing of sp=1µm. In Fig. 3(b), the reverse-biased breakdown voltages (@ I=1µA) among these three diodes with the specified channel length (L) or spacing (sp) are compared. In Fig. 3(c), the dependence of the forward-biased current (@ forward Vbias=2V) among these diodes on the number of stacked diodes are compared. The forward-biased current can be reduced when the number of stacked diodes is increased. In Fig. 3(d), the dependence of forward-biased cut-in voltage (@ Ibias=0.1µA) among these diodes on the number of stacked diodes are investigated. The cut-in voltage of the stacked diodes can be linearly increased, when the number of the diodes in the stacked configuration is increased. This will be useful for using the diodes in stacked configuration in the power-rail ESD clamp circuits.

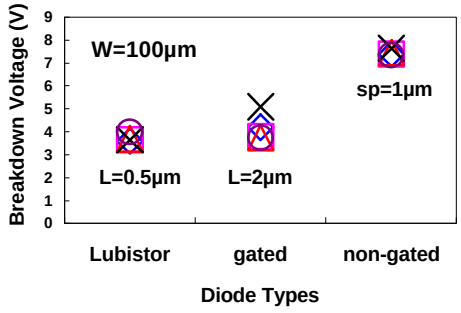
3.2. ESD Robustness

The HBM (human-body-model) ESD robustness of these three diodes with different device total junction perimeters under forward-biased condition is compared in Fig. 4. The ESD failure criterion is defined when the leakage current greater than 1µA under 2-V reverse bias across the diodes. The ESD robustness shown in Fig. 4 has the sequence of non-gated diode > gated diode > *Lubistor* diode. In Fig. 5(a), the dependence of ESD robustness of non-gated diode on its anode-to- cathode spacing under forward- and reverse-biased conditions is investigated, where the non-gated diode has a fixed junction perimeter of 300µm. The second breakdown current (It2) of non-gated diodes with different anode-to- cathode spacings under forward-biased condition, measured by the transmission line pulse generator (TLPG) with pulse width of 100ns [8]-[9], is shown in Fig. 5(b). The HBM ESD level of the non-gated diode is degraded, when its anode-to-cathode spacing is increased. Moreover, the non-gated diode in

forward-biased condition can sustain a much higher ESD level that it operated in the reverse- biased condition.



(a)



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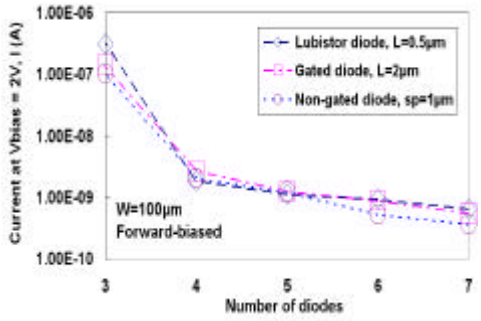
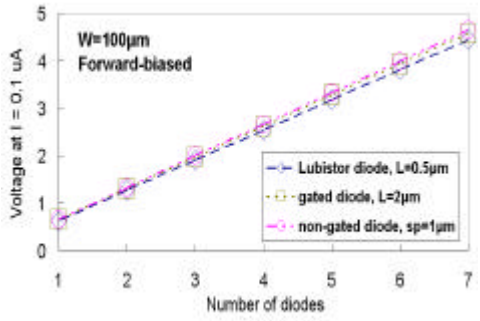


(c)



(d)

Fig. 3 The DC characteristics of (a) I-V characteristics, (b) reverse-biased breakdown voltage, (c) the forward-biased current under voltage bias of 2V, and (d) the cut-in voltage defined at I=0.1μA, of these three diodes fabricated in a 0.15-μm partially-depleted SOI salicide CMOS technology.

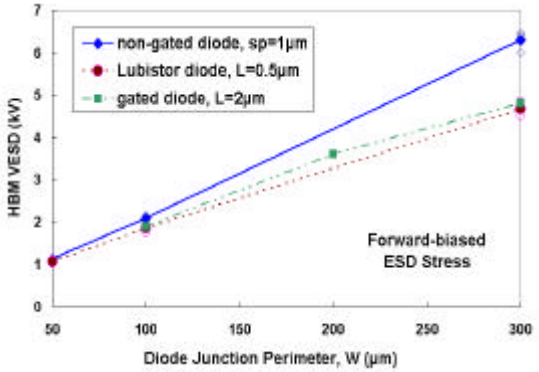
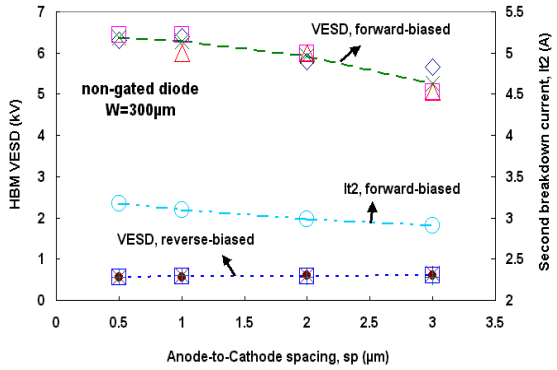
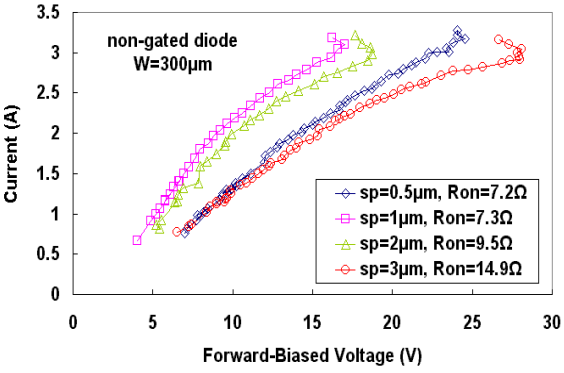


Fig. 4 Dependence of HBM ESD level on the total junction perimeter of these three kinds of diodes under forward-biased ESD stress condition.



(a)

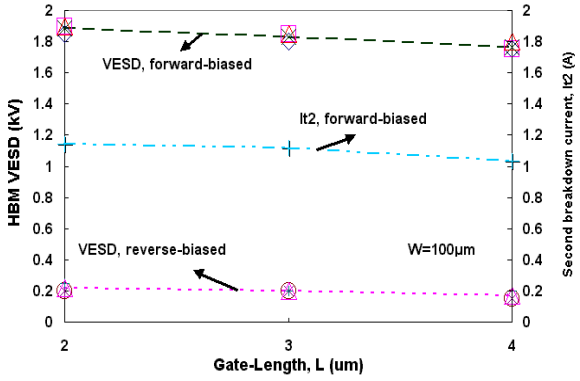


(b)

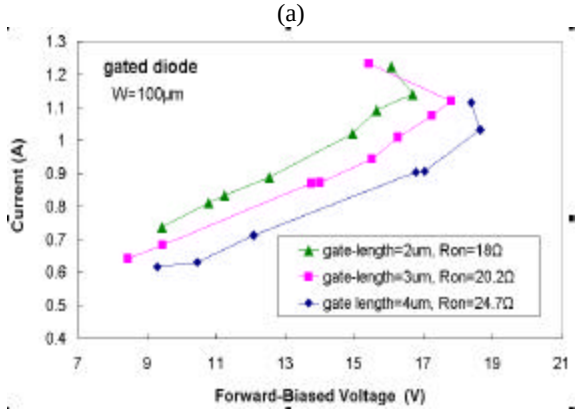
Fig. 5 (a) Dependence of HBM ESD level and It2 on the anode-to-cathode spacing (sp) of the non-gated diode with a total junction perimeter of 300μm. (b) The I-V characteristics of the non-gated diode measured by TLPG to find the It2 values.

The dependences of HBM ESD level and It2 on the gate length of the gated diode with a total junction perimeter of 100μm under forward- and reverse-biased conditions are shown in Fig. 6(a). The I-V characteristics of the gated diode measured by TLPG to find the It2 are shown in Fig. 6(b). The HBM ESD level of the gated diode is also

slightly degraded, when its gate length is increased. Of course, the gated diode in forward-biased condition can sustain a much higher ESD level that it operated in the reverse-biased condition.



(a)



(b)

Fig. 6 (a) The dependence of HBM ESD level and second breakdown current (It2) on the gate length of the gated diode with a total perimeter of 100μm. (b) The TLPG-measured I-V characteristics of the gated diode under forward-biased condition to find the It2.

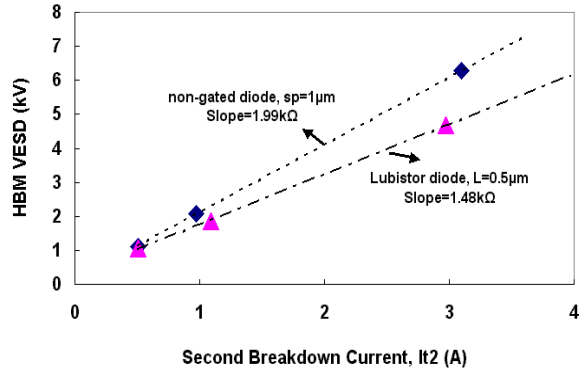
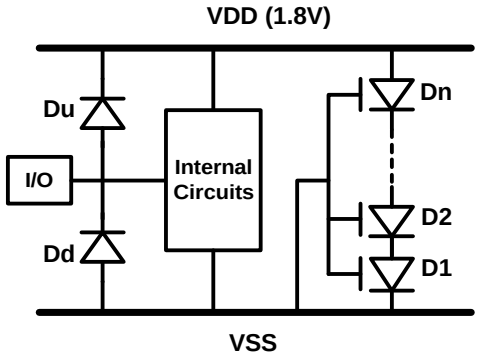


Fig. 7 The correlations between the HBM ESD level and It2 value of the non-gated diode and *Lubistor* diode under different device junction parameters.

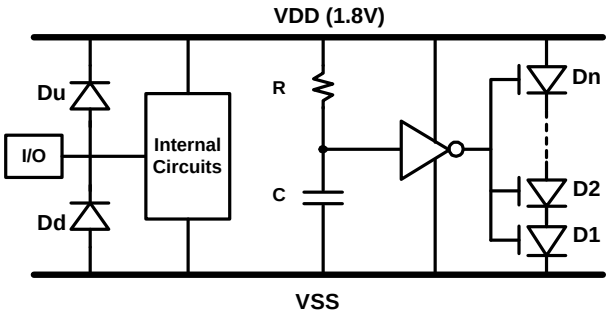
The correlations between the HBM ESD level and It2 value (measured by TLPG with pulse width of 100ns) of the non-gated diode and *Lubistor* diode are compared in Fig. 7. The non-gated diode has a V_{ESD}-to-It2 slope of 1.99 kohm, but the *Lubistor* diode has a V_{ESD}-to-It2 slope of 1.48 kohm. The experimental results have confirmed that the new proposed gated and non-gated diode structures have better ESD robustness than that of the *Lubistor* diode in this 0.15-μm partially-depleted SOI salicided CMOS process.

3.3. Power-Rail ESD Clamp Circuits with Diode String

The power-rail ESD clamp circuits constructed with the proposed gated diodes in stacked configuration for 1.8-V SOI CMOS IC are shown in Figs. 8(a) and 8(b). In Fig. 8(a), all the gates of gated diodes are connected to VSS. But in Fig. 8(b), all the gates of gated diodes are triggered by the ESD detection circuit [10] formed with *RC* and inverter. During positive VDD-to-VSS ESD transition, the ESD detection circuit will generate a positive voltage to bias the gates of the gated diodes in Fig. 8(b). With a positive gate bias, the gated diodes are expected to have higher ESD robustness and faster turn-on speed to discharge ESD current. Therefore, it can be more effective to protect the devices of internal circuits.



(a)



(b)

Fig. 8 Application of the gated diodes in VDD-to-VSS ESD clamp circuits with (a) gate-grounded design; and (b) gate-triggered design, in 1.8-V SOI CMOS IC.

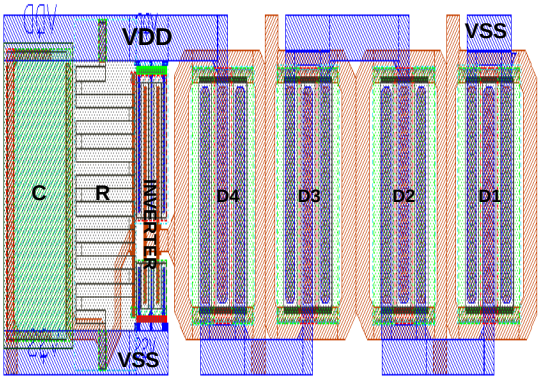


Fig. 9 Layout picture of the power-rail ESD clamp circuits constructed with four gated diodes in stacked configuration.

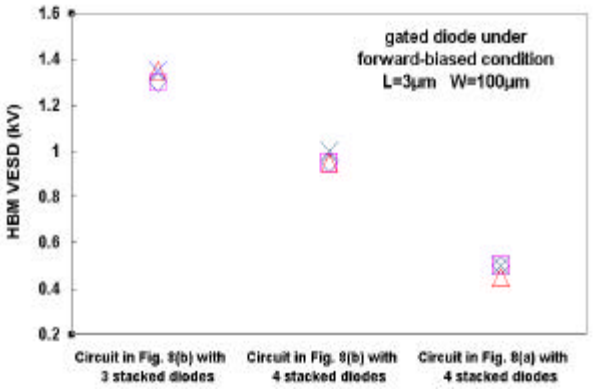


Fig. 10 The comparisons of (a) HBM, and (b) MM, ESD levels on the numbers of stacked diodes between the different power-rail ESD clamp circuits with gate-grounded or gate-triggered designs.

The layout picture of the power-rail ESD clamp circuits constructed with four gated diodes in stacked configuration realized in a 0.15-μm partially-depleted silicon-on-insulator CMOS process is shown in Fig. 9. The number of gated diodes in the stacked configuration is changed to verify its ESD level. The HBM and MM (machine-model) ESD test results of the power-rail ESD clamp circuits with different diode numbers are compared in Figs. 10(a) and 10(b), respectively. The ESD failure criterion is defined as that the leakage current greater than 1μA under 2-V VDD bias.

The ESD robustness of gate-grounded diode string is smaller than that of the gate-triggered design. In the gate-triggered design, the HBM and MM ESD levels of the power-rail ESD clamp circuits are decreased when the number of gated diodes in stacked configuration is increased. The more diodes in the stacked configuration have higher turn-on resistance, therefore to cause a lower ESD level. The HBM (MM) ESD level of the circuit in Fig. 8(b) with gate-triggered design, having 3 gated diodes in stacked configuration, is about 1.3kV (110V). When the number of gated diodes in stacked configuration changes to 4, the HBM (MM) ESD level degrades to 0.9kV (80V). The HBM (MM) ESD level of the circuit in Fig. 8 (a) with gate-grounded design, having 4 diodes in stacked configuration, is only 0.5kV (40V). The ratio of HBM-to-MM ESD level of the gated diode structure is about 11 ~ 12 in this 1.8-V 0.15-μm partially-depleted SOI salicided CMOS process.

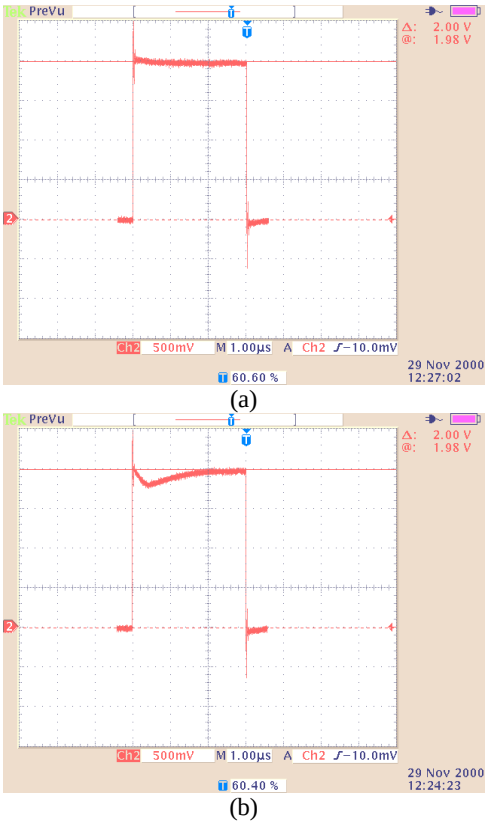


Fig. 11 The turn-on verifications on the power-rail ESD clamp circuits with (a) the gate-grounded diode string, and (b) the gate-triggered diode string, where both the diode strings have 4 stacked diodes. (X-axis:1μs/Div., and Y-axis: 0.5V/Div.)

To verify the turn-on efficiency of the power-rail ESD clamp circuits with the gated diodes during the ESD stress condition, a 0-to-2V voltage pulse is applied to VDD with VSS relatively grounded. The measured waveform on VDD node is shown in Fig. 11(a) for the power-rail ESD clamp circuit with gate-grounded design, and shown in Fig. 11(b) for the power-rail ESD clamp circuit with gate-triggered design, where both the diode strings have 4 gated diodes in stacked configuration. In Fig. 11(a), the 0-to-2V voltage waveform is not degraded, but that in Fig. 11(b) is degraded. This is due to the turn-on of stacked diode string by the ESD detection circuit (RC + inverter) to earlier clamp the applied pulse voltage. The degraded voltage waveform shown in Fig. 11(b), as well as the higher ESD level shown in Figs. 10(a) and 10(b), have further verified the effectiveness of these new proposed diode structures for ESD-protection applications in SOI CMOS IC's.

However, the number of diodes in stacked configuration must be design more enough to avoid the leakage current from VDD to VSS, especially when the IC is under normal operation condition at a high-temperature environment [7].

4. Conclusion

I-V characteristics, ESD robustness, and It2 of the gated and non-gated diode structures for ESD protection in a 0.15-μm partially-depleted silicon-on-insulator CMOS technology have been investigated and compared to that of *Lubistor* diode. Only by drawing different layout patterns on the related mask layers, the proposed diode structures can be realized and fabricated by the general SOI CMOS process without adding any extra mask layer or process step. The experimental results have confirmed that the proposed new diode structures have higher ESD robustness than the *Lubistor* diode. A novel gate-triggered design on the power-rail ESD clamp circuit with the gated diodes in stacked configuration has shown a higher ESD robustness and faster turn-on speed to effectively protect the devices of internal circuits. With a turn-on efficient power-rail ESD clamp circuit, SOI diodes in the I/O ESD protection circuits can be designed to operate in forward-biased condition during ESD stresses. Therefore, CMOS IC's can be designed to still have high enough ESD robustness in the sub-quarter-micron SOI CMOS technology.

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