ESD Protection Design for CMOS RF Integrated Circuits

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Abstract -- ESD protection design for CMOS RF integrated circuits is proposed in this paper by using the stacked polysilicon diodes as the input ESD protection devices to reduce the total input capacitance and to avoid the noise coupling from the common substrate. The ESD level of the stacked polysilicon diodes on the I/O pad is restored by using the turn-on efficient power-rail ESD clamp circuit, which is constructed by substrate-triggered technique. This polysilicon diode is fully process-compatible to general sub-quarter-micron CMOS processes.

I. Introduction

ESD phenomenon continues to be a reliability issue in CMOS ICs because of technology scaling and high frequency requirements. For RF ICs [1], on-chip ESD protection has some limitations: low parasitic capacitance [2], constant input capacitance, insensitive to substrate coupling noise [3]-[6], and high enough ESD robustness. A typical request for an RF input pad with maximum loading capacitance is only 200 fF for circuit operation at 2 GHz [2]. This 200-fF target not only includes the ESD protection devices but also the bond pad itself. In order to fulfill these requirements, diodes are commonly used for ESD protection in I/O circuits [2]. To deal with these challenges, low capacitance bond pad and low capacitance ESD protection circuitry had been reported with some specific techniques [7]-[10].

If the physical size of a bond pad is directly reduced, the parasitic capacitance generated from the bond pad can be reduced. If the bond pad on a chip is realized by only using the top-layer metal in a CMOS process of multiple metal layers, the bond pad capacitance can be further reduced. But, the bond pad constructed by using only top metal layer often results in the peel-off phenomenon. Therefore, such modified bond pads must be verified by the bonding reliability test, including the ball shear test and wire pull test [11]. Recently, by using the broken shape metal layers and additional diffusion layers, the bond pad capacitance has been successfully reduced 70% from the traditional bond pad without extra process modification [7]. This low-capacitance bond pad has passed the bonding reliability test for general applications in IC products.

Moreover, by adding a turn-on efficient ESD clamp circuit across the power rails of the input ESD protection circuit formed by the diodes, the overall ESD level of the input pin can be significantly improved [12]. The schematic diagram for input ESD protection circuit comprised of the diodes with the power-rail (VDD-to-VSS) ESD clamp circuit is illustrated in Fig. 1. When the ESD zap is applied to the pad 1 with the pad 2 grounded, the ESD current is conducted to the VDD power rail through the forward-biased ESD diode Dp1. The ESD current on VDD is discharged to the VSS power rail by the efficient VDD-to-VSS ESD clamp circuit [12]. Finally, the ESD current is conducted to grounded pad 2 through the forward-biased ESD diode Dn2. The ESD current discharging path has been indicated by the bold line in Fig. 1. By using such ESD protection design, the ESD clamp diodes are all operating in their forward-biased condition to discharge ESD current. The diode operating in the forward-biased condition can sustain a much higher

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ESD level within a small device dimension. Thus, the ESD clamp devices in the input ESD protection circuit can be realized with smaller device dimensions to significantly reduce the input capacitance of the input ESD protection circuit for high-frequency applications [8]-[10].

However, the ESD clamp devices in the input ESD protection circuit (realized by diode, MOSFET, BJT, or even SCR) have the p-n junctions located within the common substrate of CMOS ICs. The substrate noise, generated from other circuits in the same chip, may couple into the RF input node through the p-n junctions of input ESD protection devices to seriously degrade RF circuit performance [3]-[4]. Still now, there is no effective design solution to avoid the substrate noise coupling into the RF circuits through the input ESD protection devices.

In this paper, a novel diode structure constructed by the polysilicon layer for ESD protection in RF applications is proposed. The polysilicon diode can be connected in series to further reduce the total parasitic capacitance seen from the input pad. Moreover, the polysilicon diode isolated far away from the common substrate by the thick field-oxide layer is free from the substrate noise coupling problem.

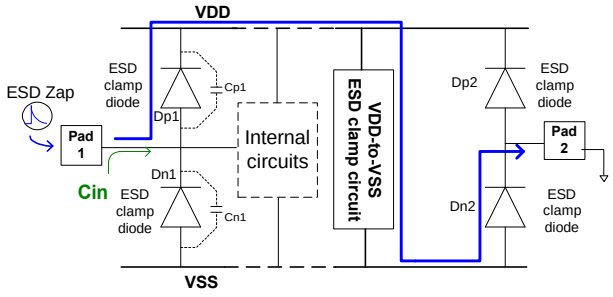

Fig. 1 The schematic diagram of a typical ESD protection design for the I/O pad with diodes and power-rail ESD clamp circuit.

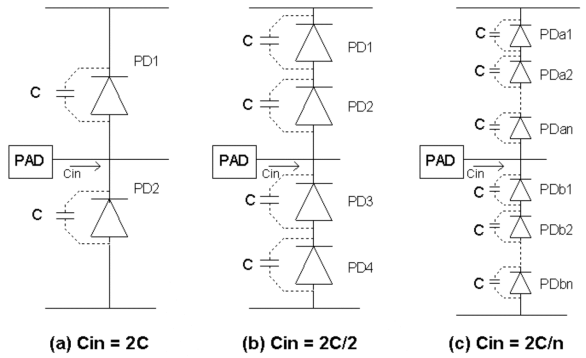

Fig. 2 The diodes in the ESD protection circuit can be further stacked to reduce the total input capacitance seen from the pad.

II. RF ESD Protection Design

A. ESD Protection Design for RF Circuits

For RF applications in GHz frequency, the total input capacitance of an input pad including ESD clamp devices is limited to only 200 fF [2]. To further reduce the capacitance generated from the ESD clamp devices becomes an important task for RF ESD protection design. From basic circuit theory, multiple capacitors stacked in series can result in a total capacitance smaller than that of a single capacitor. So, the diodes in the ESD protection circuit can be further stacked to reduce the total input capacitance, seen from the pad. The input ESD protection circuits realized with different numbers of stacked diodes to reduce the total input capacitance are shown in Fig. 2.

However, the stacked configuration connected from the pad to VSS cannot be realized by the N+ diodes within a p-type substrate, because the p-type substrate is common to every N+ diode. The stacked configuration connected from the pad to VDD may be realized by the P+ diodes within separated N-wells. Each N-well is also located in the same p-substrate to generate a vertical p-n-p BJT in every P+ diode. The additional N-well to p-substrate junction capacitance in every P+ diode causes some increase in the total input capacitance [2]. The physical device structures within a common substrate limit the realization of stacked configuration on ESD diodes to reduce the total input capacitance.

If the ESD diodes can be realized without a parasitic connection to the common substrate, ESD diodes can be fully stacked to further reduce the total input capacitance. Based on this concept, the whole-chip ESD protection design for RF circuits is proposed in Fig. 3, where the stacked polysilicon diodes are used as the input ESD clamp devices.

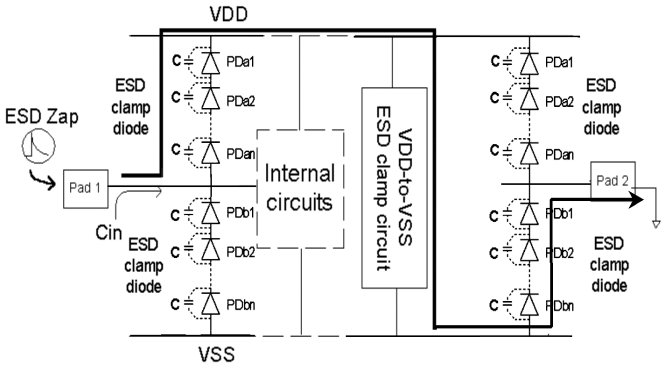

Fig. 3 The proposed ESD protection scheme for RF ICs with the stacked polysilicon diodes as input ESD clamp devices.

When a pin-to-pin ESD zapping occurs on the RF IC, the polysilicon diodes in cooperation with the turn-on efficient VDD-to-VSS ESD clamp circuit can provide a low-impedance path to quickly discharge ESD current. For a given ESD specification on the input pin, the polysilicon diodes should be drawn large enough to sustain the corresponding ESD current. The required device dimension of a polysilicon diode to sustain a specified ESD current can be calculated from its secondary breakdown current (It2). If the polysilicon diode is drawn with a smaller dimension, it has a smaller capacitance but also a lower ESD level. It is difficult to meet both the high ESD level and a low enough input capacitance. However, the new solution proposed in Fig. 3 can both sustain a high enough ESD level and further reduce the total input capacitance for GHz RF input pins. The polysilicon diodes with isolated junctions from the common IC substrate can be directly stacked to reduce the total input capacitance. In Fig. 3, if there are n stacked diodes placed from the pad to VSS and VDD, the total input capacitance becomes only 2C/n, where C is the capacitance of a single polysilicon diode. By using this design, both the ESD level and input capacitance from the requirements of GHz RF circuits can be achieved.

When the ESD zap is applied to the Pad 1 with the Pad 2 grounded, the ESD current is conducted to the VDD power rail through the forward-biased stacked polysilicon diodes (PDa1 ~ Pdan). The ESD current on VDD is discharged to the VSS power rail by the efficient VDD-to-VSS ESD clamp circuit. Finally, the ESD current is conducted to the grounded Pad 2 through another forward-biased stacked polysilicon diodes of the Pad 2. The ESD current discharging path has been indicated by the bold line in Fig. 3. With such a design, all the polysilicon diodes operate in the forward-biased condition to discharge ESD current, therefore they can sustain a higher ESD level. When the IC operates in normal condition with power supplies, all the ESD clamp diodes are operated in the reverse-biased condition. With suitable layout spacing between the N+/P+ regions on the diode structure, the polysilicon diodes can be kept off.

Because the polysilicon diodes are located on the thick shallow-trench-isolation (STI) field-oxide layer, it is far from the common IC substrate. The noise coupled from the substrate to the RF input pad can be significantly reduced if the input ESD clamp devices are realized by the proposed stacked polysilicon diodes. The traditional p-n junction diodes are very susceptible to substrate noise, because they are directly fabricated within the common substrate.

B. Process-Compatible Polysilicon Diode

The device structure of the polysilicon diode realized in a general sub-quarter-micron CMOS process is shown in Fig. 4. The polysilicon layer, used as the gate of NMOS and PMOS in CMOS technology, is drawn with separated P+ / N+ doping regions to realize the diode structure. Between the N-type high doping region, N+, and the P-type high doping region, P+, there is a region indicated "I" without impurity doping. The region I is an un-doped region of the polysilicon layer. To avoid a short between the anode and cathode of the polysilicon diode fabricated in a salicided CMOS process, a salicide-blocking mask is used to limit the polycide formation across the region I. The doping concentrations of P+/N+ regions in the polysilicon diodes are the same as the polysilicon gates of the NMOS/PMOS devices in the CMOS process. Therefore, the proposed polysilicon diode is fully process-compatible to general CMOS process without extra process modification.

A similar polysilicon diode used for power conversion and ESD protection in a smart card IC had been successfully realized in a CMOS process with extra N- (or P-) implantation process step and mask [13]. But, the polysilicon diode proposed in this work can be fully realized in general sub-quarter-micron CMOS processes without adding any extra implantation process step or mask. The spacing between the N+ and P+ regions may affect the device characteristics and will be investigated in the experimental test chips. The polysilicon diode realized on the shallow-trench-isolation (STI) layer has no junction touching the common substrate, therefore the substrate noise coupling issue can be eliminated.

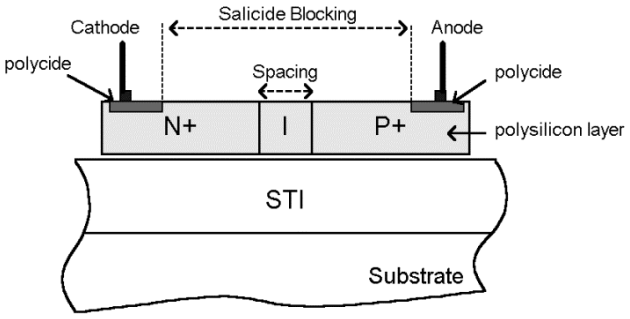

Fig. 4 The device structure of the polysilicon diode realized in a sub-quarter-micron CMOS process.

III. Power-Rail ESD Clamp Circuit with Substrate-Triggered Design

A. Substrate-Triggered Effect

In Fig. 3, the effective ESD protection design to protect the RF pin needs the strong cooperation with a turn-on efficient power-rail ESD clamp circuit. To sustain a high enough ESD level, the ESD protection device in the power-rail ESD clamp circuit often has a large device dimension. The ESD protection device with a large device dimension is generally realized by the finger-type layout. But, there is non-uniform turn-on issue among the multiple fingers in the large-dimension device during ESD stress [14]. To improve the turn-on uniformity and also to increase ESD robustness of the multi-finger NMOS device, the substrate-triggered technique has been developed [15]-[20].

The device structure and corresponding finger-type layout pattern of the substrate-triggered NMOS are shown in Fig. 5. A p+ diffusion is located in the center of NMOS device, which is used as the substrate-triggered point of ESD protection NMOS. The N-well placed under the source region, as shown in Fig. 5, is used to form a higher equivalent substrate resistance for more efficient substrate-triggered design. The dc I-V curves of a fabricated substrate-triggered NMOS (W/L= 100μm/0.3μm) under different substrate current biases are measured in Fig. 6. With a higher substrate-triggered current (I_B), the trigger voltage can be lowered to quickly turn on the parasitic lateral n-p-n BJT in the NMOS structure.

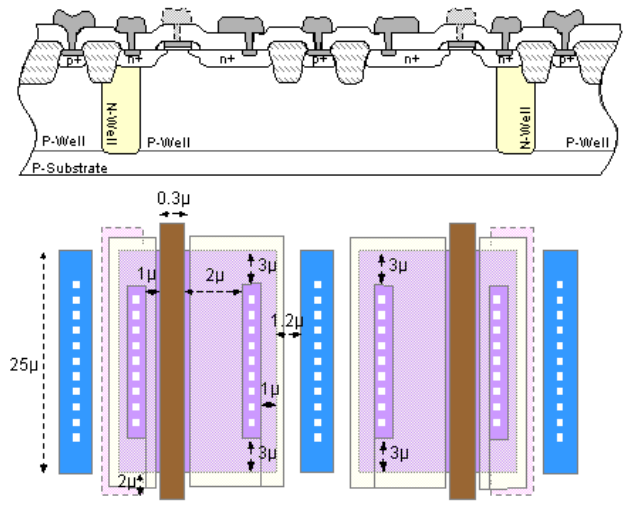

Fig. 5 Device structure and layout pattern of the substrate-triggered NMOS.

The transmission line pulse generator (TLPG) [21] with a pulse width of 100 ns is used to find the It2 (secondary breakdown current) of the fabricated NMOS under different substrate biases. The dependence of It2 on the substrate biases is shown in Fig. 7. The It2 of substrate-triggered NMOS can be continually increased when the substrate current is increased without sudden degradation. Compared to the gate-driven design [22], the substrate-triggered design can continuously increase the ESD level of the multi-finger NMOS device, when the substrate-triggered current is increased [20]. Therefore, the power-rail ESD clamp circuit in this work in conjunction with the RF input ESD protection circuit is designed by using the substrate-triggered technique.

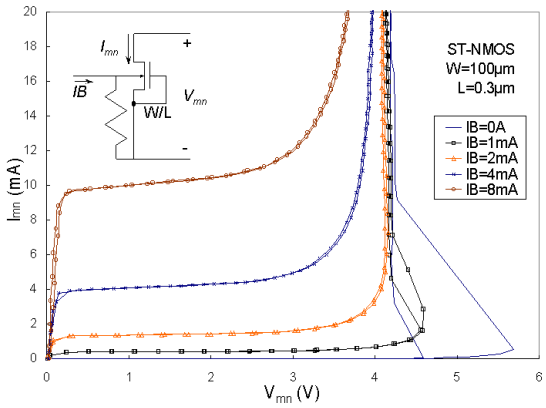

Fig. 6 The I-V curves of the substrate-triggered NMOS under different substrate current biases.

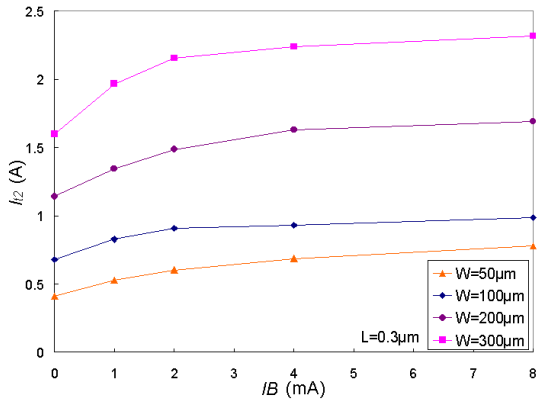

Fig. 7 The dependence of It2 on the substrate current bias of the substrate-triggered NMOS.

B. Substrate-Triggered ESD Clamp Circuit

In Fig. 8, a novel power-rail ESD clamp circuit designed with stacked polysilicon diodes and substrate-triggered technique is proposed to quickly discharge ESD current across the power rails. The

stacked polysilicon diodes in the forward-biased connection are designed to perform the desired substrate current to trigger on the ESD clamp NMOS. If the stacked diodes in Fig. 8 were realized by the P+ diffusion in N-well in a CMOS process, there was a significant leakage current (at high temperature) in the order of mA from VDD to VSS due to the parasitic vertical BJT effect [23]-[24]. But, when the stacked diode string is realized by the polysilicon layer, the leakage current can be reduced below 1μA under 2.5-V VDD bias. Therefore, the leakage current from VDD to VSS through the diode string, the substrate resistance Rsub, and NMOS in Fig. 8 can be controlled smaller than 1μA (or the desired leakage current level), if the diode number in the stacked diode string is large enough. The detailed calculation to find the suitable number (n) of the stacked polysilicon diodes in the proposed substrate-triggered ESD clamp circuit will be derived in the next sub-section.

C. Calculation on Diode Number

In Fig. 8, the stacked polysilicon diodes are used to trigger the substrate of NMOS for ESD protection. But in IC normal circuit operating condition, these polysilicon diodes may be slightly forward biased. The leakage current along the substrate-triggered NMOS and the stacked polysilicon diodes must be controlled as small as possible under the normal circuit operating condition.

The static model of a forward-biased polysilicon diode is shown in Fig. 9(a). The Gummel-Poon static model of the parasitic BJT of the substrate-triggered NMOS is drawn in Fig. 9(b). A series resistor r_d is connected with an ideal diode in Fig. 9(a). In the forward-biased condition, the current of each ideal diode is

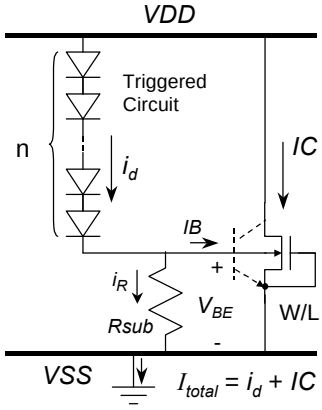

Fig. 8 The proposed turn-on efficient power-rail ESD clamp circuit by using stacked polysilicon diodes to form the substrate-triggered current.

$$i_d = I_S\left(e^{v_d/hv_T} - 1\right). \quad (1)$$

The voltage drop on each ideal diode (v_d) can be expressed as

$$v_d = hv_T \ln\left(1 + \frac{i_d}{I_S}\right), \quad (2)$$

where I_S is the saturation current, v_T is the thermal voltage, and the factor h generally has a value between 1 and 2. The voltage drop (V_{PAD}) on the VDD pad across the proposed substrate-triggered ESD clamp circuit can be expressed as

$$V_{PAD} = i_d \cdot (Rsub + n \cdot r_d) + nhv_T \ln\left(1 + \frac{i_d}{I_S}\right) - IB \cdot Rsub, \quad (3)$$

where n is the diode number of the stacked polysilicon diodes, and $Rsub$ is the parasitic substrate resistance of substrate-triggered NMOS in Fig. 8. The diode number (n) can be further derived from (3) and expressed as

$$n = \frac{V_{PAD} - v_{BE}}{hv_T \ln\left(1 + \frac{v_{BE}}{Rsub \cdot I_S} + \frac{IB}{I_S}\right) + \left(\frac{v_{BE}}{Rsub} + IB\right) \cdot r_d}. \quad (4)$$

The total leakage current between power rails under the normal circuit operating condition must be limited less than 1μA. The total leakage current of this ESD clamp circuit can be expressed as

$$i_{leakage} = i_d + IC = i_d + \frac{I_{SS}}{q_b}\left(e^{q \cdot v_{B'E'}/n_F \cdot kT} + \frac{1}{b_R} + q_b C_4\right) < 1\mu A. \quad (5)$$

From above calculation or using SPICE simulation, the relation between the diode number (n) and the total leakage current along this ESD clamp circuit under the normal circuit operating condition can be found. In general, the more stacked polysilicon diodes added into this ESD clamp circuit lead to less leakage current along this ESD clamp circuit.

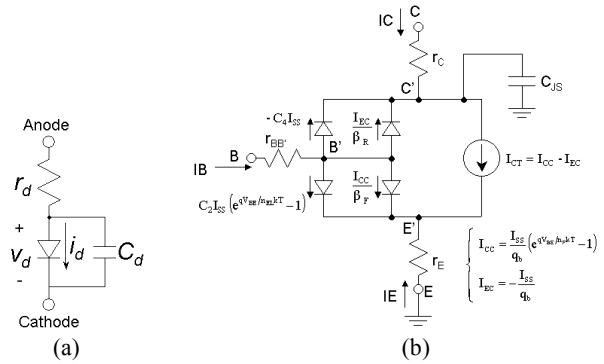

Fig. 9 The static models of (a) the polysilicon diode, and (b) the parasitic lateral BJT of the substrate-triggered NMOS, in the proposed substrate-triggered ESD clamp circuit.

IV. Experimental Results

A. Polysilicon Diode

To examine the polysilicon diode device, test chips had been fabricated in a standard salicided 0.25-μm CMOS process. The photography of a fabricated polysilicon diode is shown in Fig. 10. To use polysilicon diode as an effective ESD protection device in the integrated circuits, the dc I-V characteristics must be investigated in detail to prevent leakage issue. The measured I-V features of the fabricated polysilicon diodes with different spacing of the center region I (between N+ and P+ regions) are shown in Fig. 11. The polysilicon diode with a spacing of 0 μm has the direct connection of N+ and P+ regions without the non-doped central region. The polysilicon diode with a negative spacing has the overlap between the N+ and P+ regions in the test chip. In Fig. 11, the polysilicon diode with a spacing of 0.5 μm has a forward-biased cut-in voltage of 0.64 volts and a reverse-biased breakdown voltage of -5.02 volt, which are both defined at the 1-μA current. When the spacing decreases from 0.5 μm to -0.5 μm, the forward-biased cut-in voltage and the reverse-biased breakdown voltage are both decreased. Therefore, for the ICs with different power voltage levels, the layout spacing between N+/P+ regions of the polysilicon diodes can be adjusted to meet different applications.

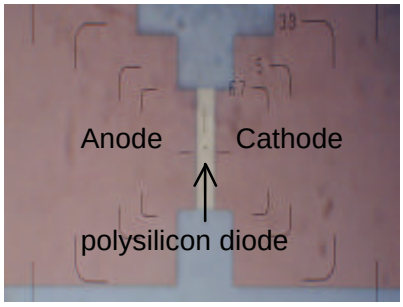

Fig. 10 The photography of a fabricated polysilicon diode in a 0.25-μm CMOS process with an junction perimeter of 30μm.

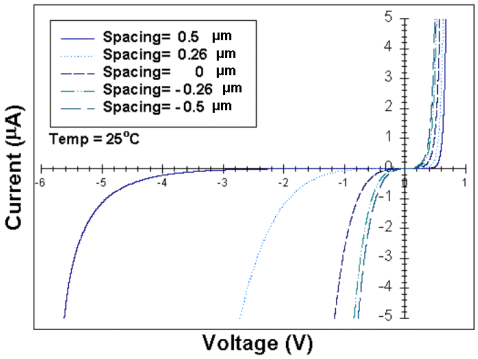

Fig. 11 The dc characteristics of the fabricated polysilicon diodes with different N+/P+ layout spacing.

Because the IC applications may cover a range of temperature, the temperature dependence on the polysilicon diodes is also investigated in this work. The temperature dependence of the forward-biased cut-in voltage on the fabricated polysilicon diodes is measured and shown in Fig. 12. When the temperature increases from 25 °C to 125 °C, the cut-in voltages of polysilicon diodes with different spacing are reduced about 0.1 V.

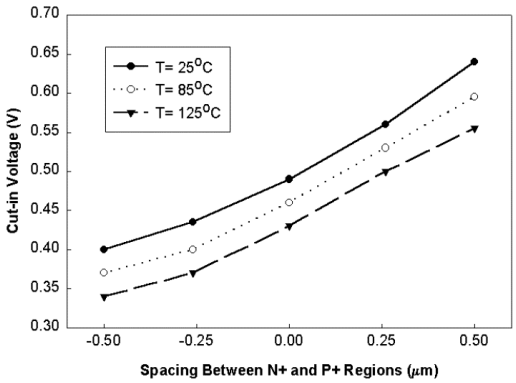

Fig. 12 The cut-in voltage variation versus the spacing between N+ and P+ regions of the polysilicon diode under different temperatures.

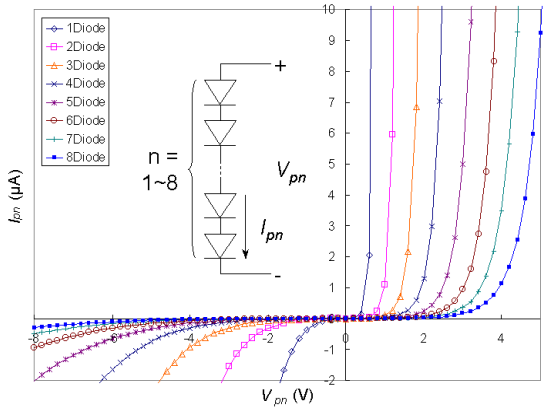

Fig. 13 I-V curves of stacked polysilicon diodes with different diode numbers.

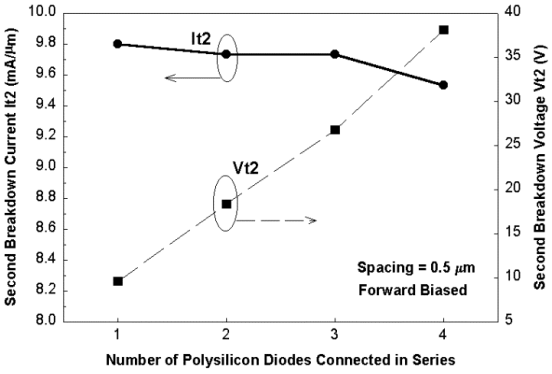

Fig. 14 The TLPG-measured second breakdown current and voltage of the stacked polysilicon diodes with different diode numbers.

To understand the I-V characteristics of stacked polysilicon diodes, the I-V curves of stacked polysilicon diodes with different diode numbers are measured in Fig. 13. With more polysilicon diodes placed into a stacked configuration, the cut-in voltage is increased. To further verify the ESD robustness of the stacked polysilicon diodes under forward-biased condition, the TLPG-measured It2 and Vt2 of the polysilicon diodes with N+/P+ spacing of 0.5 μm are shown in Fig. 14. Increasing the number of polysilicon diodes in the stacked configuration only causes a little degradation on the It2. But the second breakdown voltage increases apparently when the number of stacked polysilicon diodes is increased. The reason is that the more polysilicon diodes in stacked configuration will increase the total resistance, thereby increasing the voltage drop across the diodes. However, the stacked diodes still have high enough It2 to sustain the desired ESD level.

In Fig. 14, with four stacked polysilicon diodes, the forward-biased It2 is still as high as ~9.5mA/μm in a 0.25-μm STI CMOS process. The gate-grounded NMOS in the same CMOS technology with salicide-blocking process has an It2 of only ~6.7mA/μm under breakdown condition. Therefore, the stacked polysilicon diodes, designed for operating in the forward-biased condition to discharge ESD current as that shown in Fig. 3, can sustain a higher ESD level than a gate-grounded NMOS in the breakdown condition. To sustain a 2-kV HBM ESD stress (a corresponding It2 of 1.33A), each polysilicon diode in the stacked configuration has to be drawn with a p-n junction perimeter of 140 μm in the physical layout. The total input capacitance seen from the pad is further reduced by the stacked configuration. With a significantly reduced input capacitance and a high enough It2, the input ESD protection circuit realized by the stacked polysilicon diodes is very suitable for GHz RF circuits.

B. Substrate-Triggered ESD Clamp Circuit

To optimize the leakage current through the proposed power-rail ESD clamp circuit, the dc I-V characteristics of the substrate-triggered ESD clamp circuit with different number of stacked polysilicon diodes are measured by curve tracer, and the results are summarized in Fig. 15. To limit the leakage current less than 1μA under 2.5-V normal VDD voltage bias, the diode number is selected greater than 7 for 2.5V applications. To investigate the temperature effect on the leakage current along the substrate-triggered ESD clamp circuit with different number of stacked polysilicon diodes, the cut-in voltage defined at I=1μA is measured from 25 °C to 125 °C. The dependence of the cut-in voltage on the number of stacked diodes is shown in Fig. 16. Although the cut-in voltage of the power-rail ESD clamp circuit is somewhat reduced when the temperature increases, the leakage current can be still kept below 1μA if the number of stacked diodes is large enough.

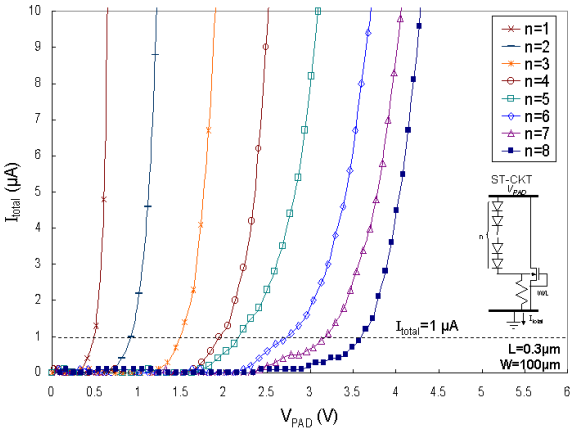

Fig. 15 The measured dc I-V characteristics of the substrate-triggered ESD clamp circuit with different number of stacked polysilicon diodes.

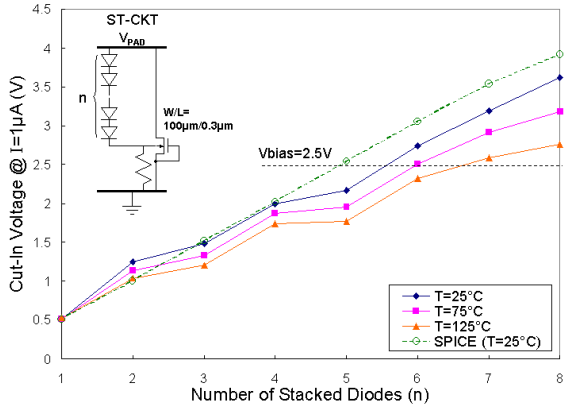

Fig. 16 The temperature effect on the cut-in voltage of ESD clamp circuit with different numbers of the stacked polysilicon diodes.

To verify the improvement on ESD robustness by substrate-triggered design, the secondary breakdown currents of the substrate-triggered ESD clamp circuit and the gate-grounded NMOS (ggNMOS) under different channel widths are measured by TLPG. The TLPG-measured I-V curves on the substrate-triggered ESD clamp circuit with 8 stacked polysilicon diodes are shown in Fig. 17. The channel

length of substrate-triggered NMOS is kept at 0.3μm. The secondary breakdown currents of the substrate-triggered ESD clamp circuit and the gate-grounded NMOS (ggNMOS) under different channel widths are compared in Fig. 18. The substrate-triggered design with 8 stacked polysilicon diodes can significantly increase It2 of the NMOS with W= 300μm from 1.5A (for ggNMOS) to 2.33A, which has a corresponding HBM ESD level of ~ 3.5kV in a 0.25-μm STI CMOS process. This has successfully verified the effectiveness of the substrate-triggered design to improve ESD robustness of the power-rail ESD clamp circuit.

In cooperation with the stacked polysilicon diodes in the input ESD protection circuit, as that shown in Fig. 3, the 2-kV ESD specification for RF input pins can be practically achieved with the substrate-triggered power-rail ESD clamp circuit. An application example of the proposed ESD protection design for a 2.4-GHz RF LNA receiver with 3 stacked polysilicon diodes on the RF input pin is demonstrated in Fig. 19.

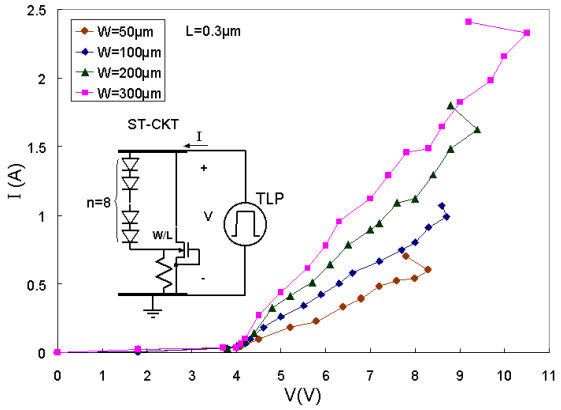

Fig. 17 The TLPG-measured I-V characteristics of the substrate-triggered ESD clamp circuit with the 8 stacked polysilicon diodes.

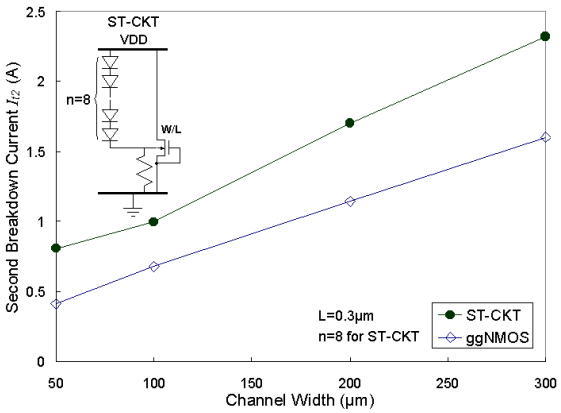

Fig. 18 Comparison on the It2 between ggNMOS and the substrate-triggered ESD clamp circuit under different channel widths.

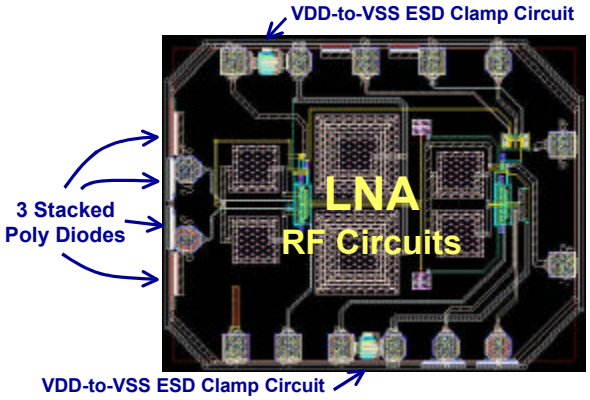

Fig. 19 Application example of the proposed ESD protection design for a 2.4-GHz LNA receiver with 3 stacked polysilicon diodes in the RF input pins.

V. Conclusion

A novel ESD protection design with stacked polysilicon diodes for RF ICs has been proposed and characterized. The polysilicon diode with an un-doped central region can be realized in general sub-quarter-micron CMOS processes. This polysilicon diode has been experimentally investigated with layout parameters, temperature variation, and pulsed I-V characteristics in a sub-quarter-micron salicided STI CMOS process. The experimental results have shown that the 4-stacked polysilicon diodes with an It2 of 9.5mA/μm in forward-biased condition is good enough to be the ESD clamp device for RF ICs. These polysilicon diodes can be further stacked to significantly reduce the total input capacitance for GHz RF circuits. A turn-on efficient power-rail ESD clamp circuit, designed with the substrate-triggered technique, has been used to significantly increase the overall ESD level of RF ICs. In cooperation with the stacked polysilicon diodes in the input ESD protection circuit, the 2-kV HBM ESD specification for RF input pins can be practically achieved with the substrate-triggered power-rail ESD clamp circuit.

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