A NEW OUTPUT BUFFER FOR 3.3-V PCI-X APPLICATION IN A 0.13-μm 1/2.5-V CMOS PROCESS

Shih-Lun Chen and *Ming-Dou Ker*
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Taiwan

ABSTRACT

An output buffer with low-voltage devices to driver high-voltage signals for PCI-X applications is proposed in this paper. Because PCI-X is a 3.3-V interface, the high-voltage gate-oxide stress is a serious problem to design PCI-X I/O circuits in a 0.13-μm 1/2.5-V CMOS process. The simulation results show that the proposed output buffer can be operated at 133 MHz without causing high-voltage gate-oxide stress problem in the 3.3-V PCI-X interface. Besides, a level converter with only 1-V and 2.5-V devices that can converter 0/1-V voltage swing to 1/3.3-V voltage swing is also proposed in this paper. The testchip to verify this new proposed output buffer is now under fabrication. The measured results will be shown in the presentation.

1. INTRODUCTION

In order to decrease the core power supply voltage (VDD), the thickness of gate oxide in the semiconductor process has been scaled down [1]. However, the board voltage (VCC) is still kept at 3.3 V or 5 V, such as PCI-X interface. Therefore, the high-voltage stress across the thinner gate oxide has become serious problem in deep submicron (DSM) processes [2]. The I/O circuit must be designed carefully to avoid the high-voltage gate-oxide stress in the mixed-voltage interface [3]-[6].

Fig. 1 shows the conventional mixed-voltage tri-state output buffer, where transistors P1 and N1 are the I/O (high-voltage (VDDQ)) devices. The voltage swing of signals IN, EN, and ENB is from GND to VDD, but the voltage swing of the output signal is from GND to VCC. If the board voltage (VCC) is equal to VDDQ, the output stage (P1 and N1) can be operated without suffering high-voltage gate-oxide stress. In Fig. 1, the level converter transforms the signals from low core voltage (VDD) to high I/O voltage (VCC) in order to prevent the high-voltage gate-oxide stress across the core devices. Fig. 2 shows the conventional level converter (CLC), where transistors P1, P2, N1, and N2 are the I/O (VDDQ) devices and transistors P3 and N3 are the core (low-voltage (VDD)) devices. If VDD is 1 V and VCC and VDDQ are 3.3 V, the voltage gap between VCC and VDD is so large that the CLC may not be operated correctly. Some techniques had been reported to overcome this problem [7]-[10]. Using precharging devices to increase driving capability was reported in [7]. A boosting technique was reported to pump the input voltage swing of the level converter [8]-[9]. The zero-Vt (or called as native-Vt) NMOS transistor was used to design the level converter for higher driving capability [10].

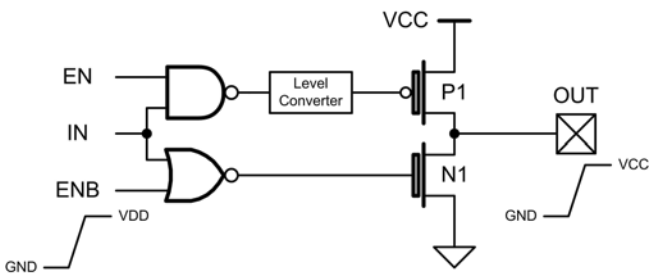

Fig. 1. Conventional mixed-voltage tri-state output buffer.

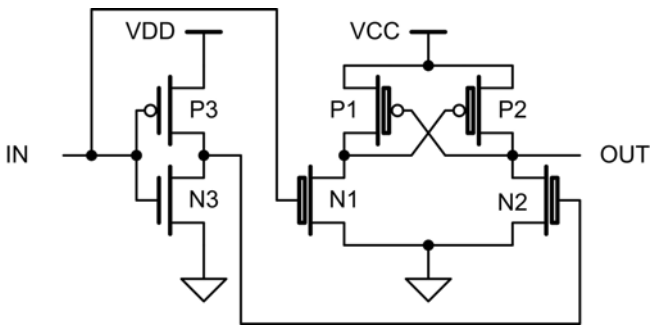

Fig.2. Conventional level converter.

However, if the board voltage (VCC) is higher than VDDQ, the output transistors P1 and N1 in Fig. 1 and these level converters [7]-[10] will suffer the high-voltage gate-oxide stress problem. In this paper, a new output buffer is proposed to solve this problem. Besides, a level converter is also presented. The proposed output buffer is designed in a 0.13-μm CMOS process with only 1-V and 2.5-V devices for 3.3-V PCI-X applications.

0-7803-8637-X/04/$20.00

2. NEW OUTPUT STAGES

Because the output buffer is designed in a 0.13-μm 1/2.5-V CMOS process, the gate-source voltages and gate-drain voltages of the core devices can not exceed 1 V. The gate-source voltages and gate-drain voltages of the I/O devices can not exceed 2.5 V. However, VCC of PCI-X specification is 3.3 V. Therefore, the output stage must be stacked and the gate voltage must be controlled to prevent high-voltage gate-oxide stress. Fig. 3 shows the new proposed output stages. In Fig. 3(a), the pull-up path and pull-down path have two stacked 2.5-V PMOS transistors and 2.5-V NMOS transistors, respectively. The gate voltages of transistors P2 and N2 are biased at VDD (1 V), so that the extra bias generator can be omitted. Because the gate voltages of transistors P2 and N2 are biased at 1 V, the gate-source voltages (Vgs) and gate-drain voltages (Vgd) of transistors P2 and N2 don't exceed 2.5 V. The maximum Vgs and Vgd of transistors P2 and N2 are around 2.3 V (3.3−1=2.3). Transistors P2 and N2 are used to protect transistors P1 and N1 against the high-voltage gate-oxide stress, respectively. However, the source voltage of transistor P1 is 3.3 V. The minimum voltage level of signal PU can't be lower than 0.8 V (3.3−2.5=0.8). Thus, the voltage swing of signal PU must be designed between 1 V (VDD) to 3.3 V (VCC). Thus, a level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing is demanded.

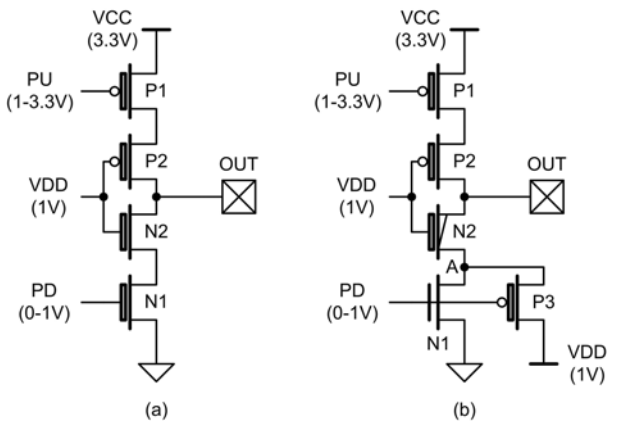

Fig. 3. The new proposed output stages (a) with all normal-Vt transistors, and (b) with a native-Vt transistor N2.

Transistors N1 and N2 in Fig. 3(a) are 2.5-V normal-Vt NMOS transistors. The threshold voltage (Vt) of 2.5-V normal-Vt NMOS transistor is still too high for high speed operation when the Vgs of the normal-Vt NMOS transistor is only 1 V. Hence, the driving capability of the pull-down path in Fig. 3(a) needs to be improved. Therefore, a modified version of output stage is shown in Fig. 3(b). Transistor N2 in Fig. 3(b) is a 2.5-V native-Vt NMOS transistor, which has a threshold voltage of −0.1 V [11]. Transistor N1 in Fig. 3(b) is a 1-V NMOS transistor. The native-Vt NMOS transistor is a standard device in a 0.13-μm CMOS process without extra process modification [11]. Therefore, the driving capability of the output buffer in Fig. 3(b) can be increased. Because the gate of transistor N2 is biased at 1 V, transistor N1 in Fig. 3(b) can be safely operated without suffering high-voltage gate-oxide stress. However, transistor N2 is a native-Vt NMOS transistor. The sub-threshold leakage current could be serious. If the voltage on the out node in Fig. 3(b) is 3.3 V, the sub-threshold current of transistor N2 may occur. Thus, the voltage on node A in Fig. 3(b) may exceed 1 V. An extra PMOS transistor P3 is added in Fig. 3(b) to keep the maximum voltage on node A at 1 V. When signals PU and PD are at logic "0" (1 V and 0 V), the voltage on the out node is VCC (3.3 V). Because signal PD is 0 V, transistor P3 is turned on to keep the voltage on node A at 1 V. Hence, the high-voltage gate-oxide stress caused by sub-threshold leakage of transistor N2 is avoided. Because transistor P3 is a weak device that keeps the voltage on node A at 1 V, it can be a 2.5-V normal-Vt PMOS transistor. Fig. 4 is the simulation waveforms of the output stages in a 0.13-μm CMOS process with only 1-V and 2.5-V devices. In this simulation, the transistor sizes of these two output stages are the same. Fig. 4 shows that the driving capability of Fig. 3(b) is better than that of Fig. 3(a).

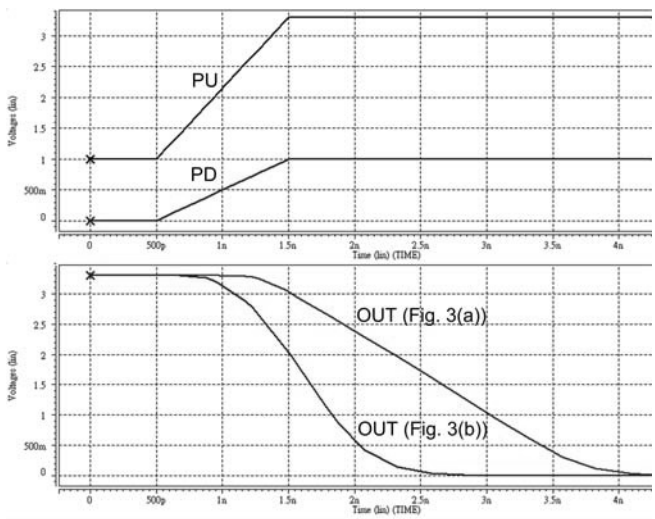

Fig. 4. Simulation waveforms of the output stages.

3. NEW LEVEL CONVERTER

Fig. 5 shows the new proposed level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing. Transistors N1A and N1B are 1-V normal-Vt NMOS transistors, whereas transistors N2A and N2B are 2.5-V native-Vt NMOS transistors, so that the driving capability can be increased. The other transistors are all 2.5-V normal-Vt transistors. Transistors P3A can keep the voltage on node A1 at 1 V when the voltage on node B1 is 3.3 V. Similarly, transistor P3B is used to keep the voltage on node

A2 at 1 V when the voltage on node B2 is 3.3 V. The swing of input signals IN and INB is from 0 V to 1 V. When signal IN is 1 V and signal INB is 0 V, the voltage on node B1 is pulled down to 0 V and transistor P5A is turned on. After transistor P5A is turned on, the voltage on node OUTB is pulled down to 1 V, and then transistors P4B and P1B are turned on. Therefore, the voltages on nodes OUT and B2 are pulled up to 3.3 V.

When signal IN is 0 V and signal INB is 1 V, the voltage on node B2 is pulled down to 0 V and transistor P5B is turned on. After transistor P5B is turned on, the voltage on node OUT is pulled down to 1 V, and then transistors P4A and P1A are turned on. Therefore, the voltages on nodes OUTB and B1 are pulled up to 3.3 V.

Only using PMOS transistors to pull down nodes OUT and OUTB is too slow, so two cross-coupled NMOS transistors N3A and N3B are added to increase the pull-down speed. Fig. 6 shows the simulation waveforms of the new proposed level converter in a 0.13-μm 1/2.5-V CMOS process. The pull-down speed of the proposed level converter with transistors N3A and N3B is faster than that of the level converter without N3A and N3B.

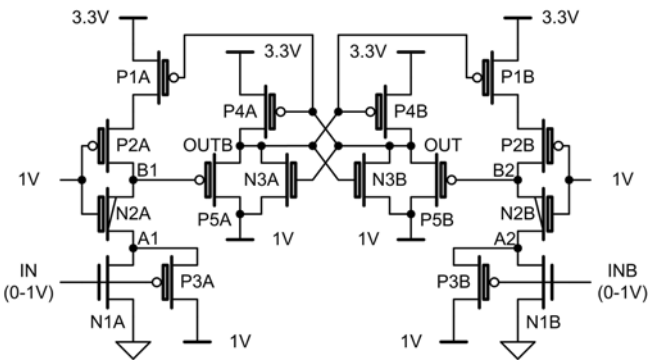

Fig. 5. The new proposed level converter which can convert the 0/1-V signal swing to 1/3.3-V signal swing.

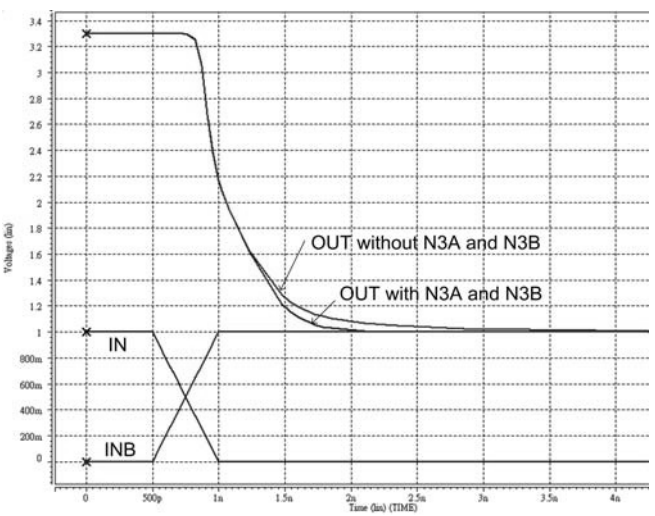

Fig. 6. Simulation waveforms of the new proposed level converter with or without transistors N3A and N3B.

4. WHOLE OUTPUT BUFFER

Fig. 7 shows the whole output buffer, which consists of an output stage, a level converter, a tri-state control circuit and two taper buffers. A CMOS NAND gate, and a CMOS NOR gate are used to implement the tri-state control circuit. When control signal EN is 0 V and control signal ENB is 1 V, the output buffer is in the high-impendence state. When control signal EN is 1 V and control signal ENB is 0 V, the output buffer drives an output voltage according the signal IN from core circuit. Another tri-state control circuit that consists of six transistors is shown in Fig. 8(a). The tri-state control circuit in Fig. 7 can be replaced by that in Fig. 8 (a). The output stage of this output buffer is the same as that in Fig. 3(b). The level converter that can convert the signal swing from 0/1 V to 1/3.3 V has been shown in Fig. 5. Taper buffer 1 and taper buffer 2 are demanded to drive the output stage because the transistors of the output stage are large-size devices. Because the swing of signal PU is from 1 V to 3.3 V, the INV1 in taper buffer 1 is shown in Fig. 8(b). The PMOS and NMOS transistors of INV1 are 2.5-V normal-Vt devices. Because the swing of signal PD is from 0 V to 1 V, the INV2 in taper buffer 2 is shown in Fig. 8(c). The PMOS and NMOS transistors of INV2 are 1-V normal-Vt transistors. In order to keep signal PU and signal PD in phase, the delay of taper buffer 1 and level converter must be equal to that of taper buffer 2. Otherwise, the output stage would consume extra short-circuit current.

Fig. 9 shows the simulation waveforms of the new proposed output buffer operating with a 133-MHz 3.3-V PCI-X output signal in a 0.13-μm 1/2.5-V CMOS process. Because the parasitic inductance of the bond wire has been also included in this simulation, the overshoot and undershoot of the output waveform can be found, as shown in Fig. 9. A testchip, which has been draw to verify the new proposed output buffer, is under fabrication in a 0.13-μm 1/2.5-V 1P8M CMOS process. The layout of the testchip is shown in Fig. 10. The measured results of the testchip will be shown in the presentation.

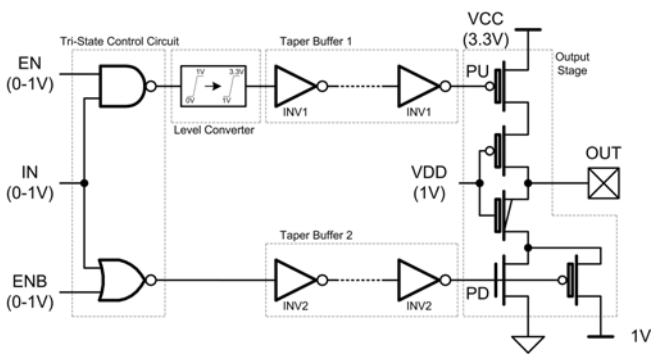

Fig. 7. The whole output buffer which drives 3.3-V output signal in the 0.13-μm CMOS process with only 1-V and 2.5-V devices.

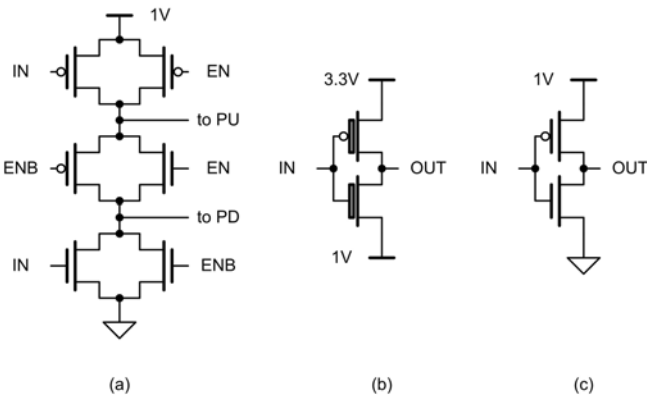

Fig. 8. Circuit implementation to realize (a) tri-state control circuit, (b) INV1, and (c) INV2.

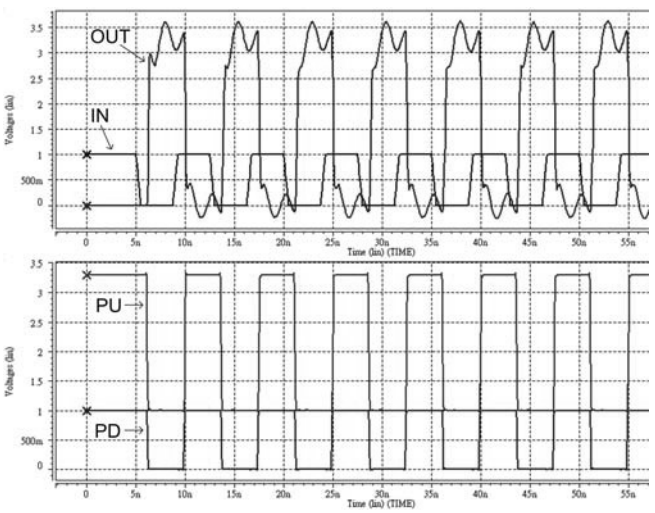

Fig. 9. Simulation waveforms of the proposed output buffer operating with a 133-MHz 3.3-V PCI-X output signal in a 0.13-μm CMOS process with only 1-V and 2.5-V devices.

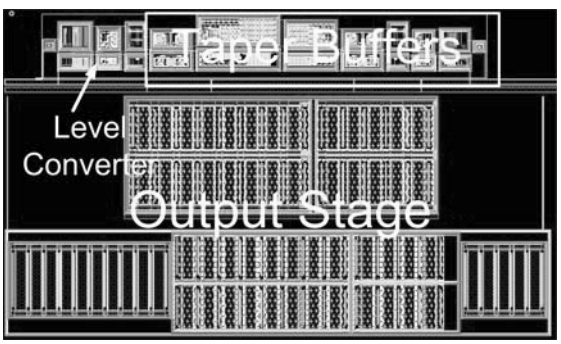

Fig. 10. Layout of the whole output buffer.

5. CONCLUSION

A new output buffer realized by low-voltage devices in a 0.13-μm CMOS process has been proposed in this paper. The new proposed circuit, which consists of low-voltage (1-V and 2.5-V) devices, can be safely operated in a 3.3-V PCI-X interface without suffering high-voltage gate-oxide stress. The simulation results show that the proposed output buffer can be operated with a 133-MHz 3.3-V PCI-X output signal. Besides, a new level converter, which can convert the 0/1-V signal swing to 1/3.3-V signal swing, has been also proposed in this paper. This new proposed output buffer is suitable for applications in the high-speed mixed-voltage interfaces.

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