

On-panel Electrostatic Discharge (ESD) Protection Design with Thin-film Transistor in LTPS Process

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Abstract

The electrostatic discharge (ESD) robustness of diode-connected n-type thin-film transistors (N-TFTs) and diode-connected p-type thin-film transistors (P-TFTs) with different layout structures in a given low-temperature polycrystalline silicon (LTPS) process is investigated. By using the wafer-level transmission line pulsing (TLP) system, the high-current transient characteristics and the secondary breakdown current (I_{t2}) levels of the diode-connected TFTs under different device parameters and layout structures are directly measured on the glass substrate. Finally, one set of design rules for on-panel ESD protection design is suggested.

Key Words: Thin-film Transistors (TFTs), Low-temperature Polycrystalline Silicon (LTPS), Electrostatic Discharge (ESD), Transmission Line Pulsing (TLP) System

1 Introduction

LTPS TFT devices have been widely used in active matrix liquid crystal display (AMLCD) because the electron mobility of the LTPS TFT device can be 100 times faster than that of the conventional amorphous silicon (a-Si: H) TFT device^[1]. Many small-size to mid-size AMLCDs fabricated by LTPS technology have been used in mobile phone, digital camera, notebook, and so on. The state-of-the-art design efforts focus on realization of system-on-panel (SOP) application^[2,3] to integrate all control and driver circuits on the glass substrate.

The electrostatic discharge (ESD) is one of the major reliability concerns in integrated circuits (ICs)^[4]. However, it has become the most critical issue on liquid crystal display (LCD) to reduce the production yield^[5]. In panel protection, glass panels or human beings could accumulate considerable static charges during back-end fabrication or automatic testing. When machines or workers touch any

input/output (I/O) pad on panel, these accumulative static charges will be discharged via any low-resistance path to ground. Such electrostatic discharge (ESD) event generates a spontaneous high-current stress within a duration of hundreds nanoseconds. If the device is not capable to sustain this ESD stress, it will reach the critical temperature of thermal runaway to cause the secondary breakdown^[6]. Unfortunately, the materials used on LCD industry, such as oxynitride, polysilicon, and glass substrate, have poor thermal conductivity^[7]. The ESD-generated heat cannot be immediately dissipated, and then it easily causes permanent damage on LCD panel. When the design rules are shrunk to make more circuits integrated on LCD panel, the ESD reliability of thin-film transistors (TFTs) becomes more important.

The earlier studies^[8-10] demonstrated the failure phenomena on threshold voltage, transconductance, and capacitance of TFTs after different over-voltage stresses. However, no high-current transient characteristics or ESD

robustness of TFTs were discussed. In this work, three different layout structures of diode-connected n-type TFTs (N-TFTs) and p-type TFTs (P-TFTs) fabricated in a given low-temperature polycrystalline silicon (LTPS) process were tested to evaluate their ESD robustness from the secondary breakdown current (I_{t2}) by wafer-level transmission line pulsing (TLP) system. Finally, layout parameters of the diode-connected TFTs are suggested for ESD protection design on LCD panel.

2 Device Fabrication

In the LTPS process, an α -Si:H film were deposited on glass substrate, and then the XeCl excimer laser was used to crystallize this film^[11]. After the active islands were defined, all the ion doping processes were carried out and activated to form source and drain regions. Following, the gate insulator and gate metal were deposited, and then patterned. After the inter-metal dielectric (IMD) layer was deposited, the contact holes and the metal pads were formed for interconnection, as shown in Fig. 1. Finally, the hydrogenation was used to improve the device performance^[12].

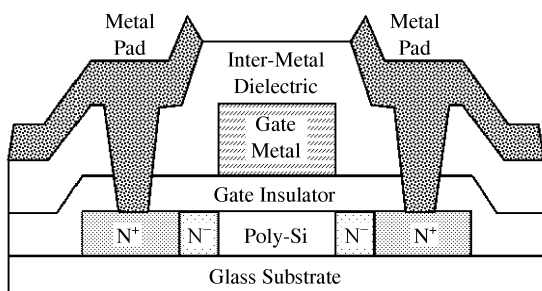


Fig. 1 The cross-section view of LTPS N-TFT

In this process, the LTPS N-TFTs with a 1 μm lightly doped drain (LDD) were drawn in finger layout style. However, the fabrication process for the LTPS P-TFTs does not have LDD structure. The total channel width is the product of the number of fingers and the unit finger width. The N-TFT and P-TFT are drawn in diode-connected configuration, where the drain node and the gate node are connected with by metal interconnection. The channel length (L) and the channel width (W) of N-TFTs and P-TFTs are varied from 5 μm to 20 μm and 100 μm to 500 μm , respectively. The N-TFTs and P-TFTs with the same W/L ratio were also drawn in different device dimen-

sions to investigate the effects on ESD robustness.

3 Measurement Setup

The configuration of wafer-level TLP system used to simulate human body model (HBM) ESD event^[13] within a period of hundreds nanoseconds is shown in Fig. 2. The transmission line is initially charged by the high voltage source, and then it generates a 100 ns current pulse with 10 ns rise time into the device under test (DUT). The current and voltage waveforms are monitored on the oscilloscope by current probe and voltage probe. By increasing the charging voltage on the transmission line step-by-step, the TLP-measured current and voltage values can be obtained to present the high-current transient characteristics of the DUTs.

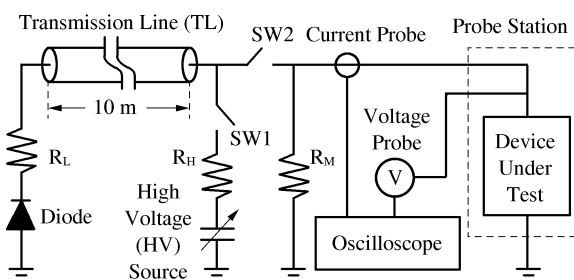


Fig. 2 The configuration of wafer-level TLP system used to measure the TLP I-V curve of LTPS TFT

In the measurement, the diode-connected N-TFT with the grounded source node is placed at DUT. The TLP energy injected from the drain node to the source node means that the diode-connected N-TFT is under forward TLP stress. The TLP waveforms show good square-like pulses before the final failure occurring. When the TLP current is increased to cause the permanent damage, as shown in Fig. 3(a), the leakage current of the diode-connected N-TFT is abruptly increased compared to that of the fresh device. Such permanent damage also results in the abnormal turn-on resistance of the diode-connected N-TFT during TLP stress, so that the abruptly changed TLP waveforms are detected in the 75% – 85% duration on the oscilloscope, as shown in Fig. 3(b). It also reflects to a break point in the TLP-measured I-V curve (shown in the later Figures). Therefore, the I_{t2} of the diode-connected N-TFT, which can sustain the maximum TLP current without permanent damage, can be determined to evaluate its ESD

robustness. From the pervious study^[14], the HBM ESD level (VESD) of LTPS TFTs can be approximated as

$$\text{VESD} \approx (1.5 \text{ k}\Omega + \text{RTLP}) \times \text{It2}, \quad (1)$$

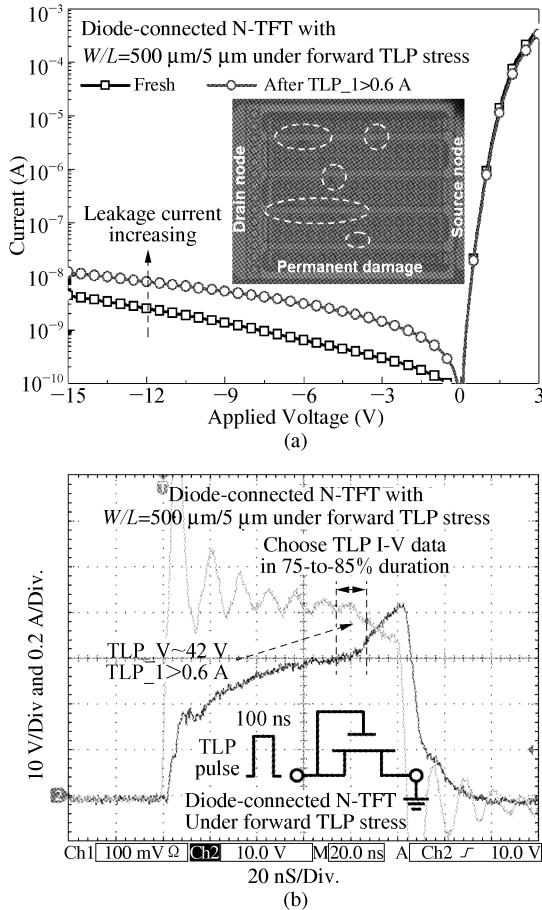


Fig. 3 (a) The permanent damage points, and (b) the TLP-measured I-V waveforms, of the diode-connected N-TFT with $W/L = 500 \mu\text{m}/5 \mu\text{m}$ after over 0.6 A forward TLP-current stress.

where $1.5 \text{ k}\Omega$ and RTLP are the equivalent resistance of human body and the DUT, respectively. Consequently, the DUT with a larger It2 value obtained from the wafer-level TLP system is expected to have a higher HBM ESD level.

4 Experimental Results

Fig. 4 and Fig. 5 show the TLP-measured I-V curves of the diode-connected N-TFTs and the diode-connected P-TFTs with different channel widths under forward TLP stress. The channel length is kept at $5 \mu\text{m}$. The diode-connected N-TFT and diode-connected P-TFT with longer

channel widths have a lower turn-on resistance, so it can sustain higher current under forward TLP stress. The It2 of the diode-connected N-TFT is increased from 0.14 A to 0.6 A, and the It2 of the diode-connected P-TFT is increased from 0.06 A to 0.25 A, when the channel width is increased from $100 \mu\text{m}$ to $500 \mu\text{m}$.

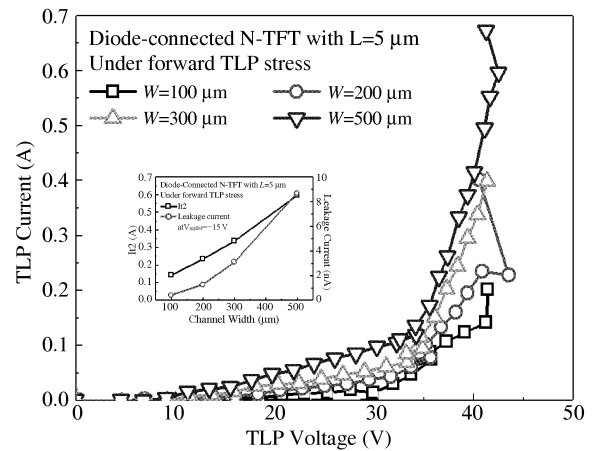


Fig. 4 The TLP-measured I-V curves of the diode-connected N-TFTs with different channel widths under forward TLP stress.

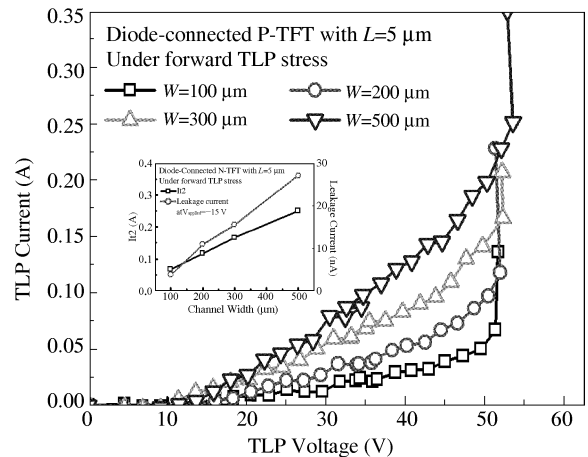


Fig. 5 The TLP-measured I-V curves of the diode-connected P-TFTs with different channel widths under forward TLP stress.

However, increasing the channel width always accompanies the increase of fresh leakage current. If the diode-connected N-TFT or P-TFT are used as an ESD protection device on LCD panel, the fresh leakage current is the standby current which causes extra standby power dissipation. Therefore, the It2 (ESD) level and the fresh leakage current form a tradeoff on the increase of channel width of

the diode-connected TFT.

The TLP-measured I-V curves of the diode-connected N-TFTs and the diode-connected P-TFTs with different channel lengths under forward TLP stress are shown in Figs. 6 and 7, respectively. From the TLP-measured I-V curves, the diode-connected N-TFTs exhibit short-circuit or open-circuit characteristic after the secondary breakdown point, especially for those with long channel length. When the channel length is increased with the channel width unchanged, the turn-on efficiency of the diode-connected N-TFT and the diode-connected P-TFT are decreased to cause a lower I_{t2} . The I_{t2} of the diode-connected P-TFT is decreased from 0.30 A to 0.13 A when the channel length is linearly increased from 5 μm to 20 μm . However, the I_{t2} of the diode-connected N-TFT is kept between 0.55 A to 0.7 A, which presents less dependence on the increased channel length. As shown in Figs. 6 and 7, the failure power ($I_{t2} \times \text{failure voltage}$) under TLP stress is increased with the increase of the channel length. The reason is that the longer channel length of the diode-connected TFTs under the same channel width can enlarge the device dimension and result in larger heat dissipation area under forward TLP (ESD) stress. Therefore, for on-panel standby current consideration under the same channel width, the diode-connected TFTs would be drawn with channel length between 10 μm to 15 μm to obtain a good ESD robustness.

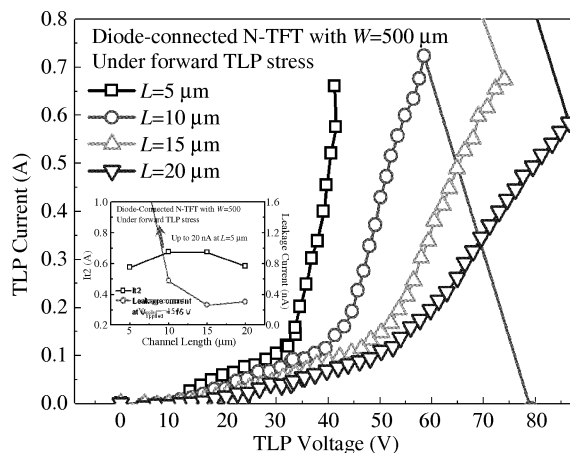


Fig. 6 The TLP-measured I-V curves of the diode-connected N-TFTs with different channel lengths under forward TLP stress.

The TLP-measured I-V curves of the diode-connected N-TFTs and the diode-connected P-TFTs with the fixed

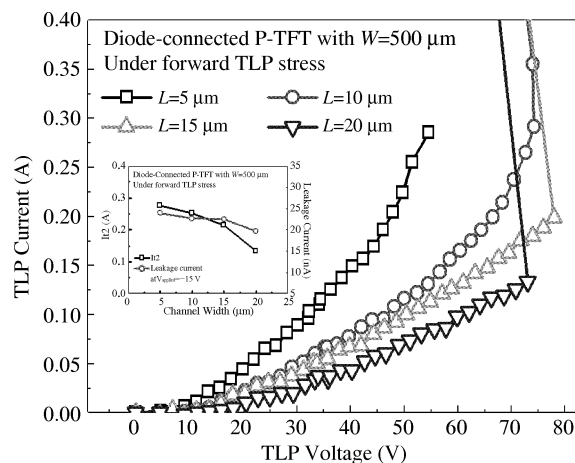


Fig. 7 The TLP-measured I-V curves of the diode-connected P-TFTs with different channel lengths under forward TLP stress.

W/L ratio of 100 under forward TLP stress are shown in Figs. 8 and 9. The diode-connected N-TFT and the diode-connected P-TFT with the longest channel width of 1 500 μm , which means the largest heat dissipation area, have the highest I_{t2} level.

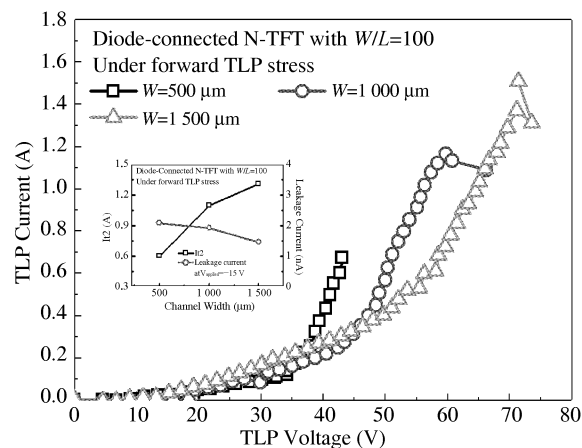


Fig. 8 The TLP-measured I-V curves of the diode-connected N-TFTs with a fixed W/L ratio of 100 under forward TLP stress.

When the channel width of the diode-connected N-TFTs and the diode-connected P-TFTs with the fixed W/L ratio of 100 is linearly increased from 500 μm to 1 500 μm , the I_{t2} of the diode-connected N-TFTs is increased from 0.6 A to 1.4 A. However, the I_{t2} of the diode-connected P-TFT is just increased from 0.27 A to 0.83 A. From (1), the HBM ESD level of the diode-connected N-TFTs with $W/L = 1 500 \mu\text{m}/15 \mu\text{m}$ is about 2.1 kV, which is larger than the basic specification of 2 kV HBM ESD level for com-

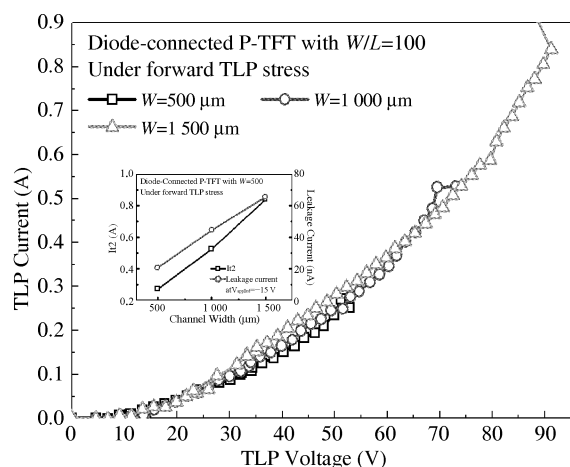


Fig. 9 The TLP-measured I-V curves of the diode-connected P-TFTs with a fixed W/L ratio of 100 under forward TLP stress.

mercial ICs products. Therefore, when the diode-connected N-TFT is used as an ESD protection device on LCD panel, its channel width can be enlarged with the fixed W/L ratio to improve the ESD robustness and to have a low fresh leakage current.

5 Conclusions

The ESD robustness among the diode-connected N-TFTs and the diode-connected P-TFTs under different layout structures in a LTPS process has been investigated by using the wafer-level TLP system. Enlarging the channel width immediately improves the I_{T2} (or ESD) level, but it also accompanies the increased fresh leakage current. On the other hand, enlarging channel length decreases the I_{T2} level and the fresh leakage current. The diode-connected N-TFTs and diode-connected P-TFTs drawn in the fixed W/L ratio with the increased channel width can greatly improve the I_{T2} level, due to the large heat dissipation area. From this investigation, the diode-connected N-TFT with $W/L = 1500 \mu\text{m}/15 \mu\text{m}$ can sustain 2.1 kV HBM ESD level, which can meet the basic ESD specification for system-on-panel applications.

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