# On-panel Analog Output Buffer for Data Driver with Consideration of Device Characteristic Variation in LTPS Technology

Yu-Hsuan Li<sup>1</sup>, Ming-Dou Ker<sup>1</sup>, Chun-Yao Huang<sup>2</sup>, Chun-Yuan Hsu<sup>2</sup>

<sup>1</sup> Nanoelectronics and Gigascale Systems Laboratory,
Institute of Electronics, National Chiao-Tung
University, Hsinchu, Taiwan, China,

<sup>2</sup> Panel Design Dept., Technology Development General Division,
R&D Center, TFT Business Unit, Chunghwa Picture Tubes,
LTD., Taoyuan, Taiwan, China

### **Abstract**

A class-A analog output buffer for the data driver with consideration of device variation in low temperature poly-silicon (LTPS) technology is proposed. With high enough mobility, LTPS thin-film transistor (TFT) has been suitable for the realization with driver circuits on the LCD panel to meet system-on-panel (SoP) applications. However, the device characteristics of poly-Si TFTs have poor uniformity and suffer from huge variations in different locations due to the poly-silicon grain structures. Besides, the variation on device characteristic of the N-type TFT is much worse than that of P-type TFT. Therefore, replacing the critical part of the analog circuit by P-TFTs is a good design solution for suppressing device characteristic variation in order to improve manufacturing yield of the analog circuit on panel. A class-A output buffer realized with P-TFTs as the input stage has been designed and fabricated in a 8-\mu m LTPS technology. From the experimental results, this proposed analog output buffer with P-TFTs as input stage can be operated at 50-kHz operation frequency with at least a 1-to-9 V output swing for using in the on-panel data drivers to provide a uniform brightness and high resolution display.

**Key Words:** Data Driver, Analog Output Buffer, LTPS, Slew Rate, Manufacturing Yield

### 1 Introduction

Low temperature poly-silicon (LTPS) thin-film transistors (TFTs) have been widely investigated as a material for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on, because the electron mobility of LTPS TFTs is about 100 times larger than that of the conventional amorphous silicon TFTs. Furthermore, LTPS can achieve slim, compact, and high-resolution display by integrating the driving circuits on peripheral area of display. If the mobility of poly-Si TFTs is further increased, this technology will become more suitable for realization of system-on-panel (SoP) applications that will integrate with memory,

CPU, and display[1,2].

At present, LTPS technology has a tendency towards integrating all control circuits and driver circuits on the glass substrate [3], [4]. In general, the LCD driver contains gate driver, data driver, and DC-DC converter. The data driver is composed of shifter registers, latch, level shifters, digital-to-analog converters (DACs), and analog output buffer. The output buffer is a critical design to achieve the low power dissipation, high resolution, and large output swing on LCD panel.

However, in spite of many advantages of LTPS technology, main applications are still limited to small size displays. The reason is that the poly-Si TFTs have poor uni-

formity and suffer from large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si thin film. The random grain boundaries and trap density exist in the channel region. This leads to some problems in real product applications such as non-uniformity brightness in panel, error reading in digital circuits, current gain mismatching in analog circuits, and so on<sup>[5]</sup>. As a result, the device characteristic variation becomes a very serious problem for analog circuit design on the LCD panel<sup>[6]</sup>.

In LTPS technology, the threshold voltages of the N-type TFT devices in different panel locations vary from 0.75 V to 2.15 V, whose variation is quite large compared with CMOS technology [7]. Besides, the device characteristic variation of the N-type TFT is more serious than that of P-type TFT [8]. For example, the mobility variation of N-type TFT and P-type TFT under the hot-carrier stress are -38.627% and +7.054%, respectively [9]. For this reason, replacing the critical part of the analog circuit by P-TFTs is a valid technique for suppressing device characteristic variation and improving the manufacturing yield of the analog circuit on panel.

In this work, a class-A analog output buffer with P-TFTs input differential pair for the data driver circuit fabricated on LCD panel in LTPS technology is proposed. The device suppression method by using P-TFTs input differential pair can effectively maintain the performance of onpanel analog output buffer and increase the manufacturing yield of the circuit.

## 2 Class-A Output Buffer

The conventional source follower output buffer has been integrated on the glass substrate for data driver  $^{[10]}$ . There are some drawbacks in such output buffer including the lower output swing and the higher input offset voltage. The output swing of the source follower output buffer is limited to  $V_{\rm DD}\text{-}V_{\rm th}$ . Besides, there is always an input offset voltage in the source follower output buffer due to the threshold voltage of the TFT. The output swing and input offset voltage of source follower output buffer are not constant values, because these are both related to the various threshold voltages of the TFTs in different panel locations. In opposition to the source follower output buffer, the unity-gain output buffer with an OP amp has lower input off-

set voltage. The relation function between the input and output of this output buffer is

$$V_{\text{out}} = \frac{A}{1 + A} V_{\text{in}}.$$
 (1)

For this reason, the inp ut offset voltage can be reduced by the large open-loop gain (A) of the unity-gain output buffer with an OP amp. In this work, the two-stage OP amp is adopted as a unit-gain output buffer, since the two-stage OP amp has higher open-loop gain, as well as the OP amp has high immunity to noise. Furthermore, the unity-gain output buffer with an OP amp has a larger slew rate for driving the capacitance load of the data bus on panel than that of source follower output buffer at the same operation frequency.

The circuit diagram of the class-A analog output buffer with N-TFTs input stage is shown in Fig. 1. As a unitygain buffer, the output node (Vo) is connected to the negative input node (Vi –) and the input signal is applied to the positive input node (Vi +). This output buffer comprises four parts as following. The first part consists of an n-channel differential pair (M1 – M2) with a p-channel current mirror load (M3 – M4) and an n-channel tail current source (M5). The second part is a common-source amplifier stage (M6 – M7), which can improve the openloop gain and reduce the input offset voltage for this output buffer. The bias generator part is a constant  $g_{\rm m}$  bias circuit (M11 – M16 and  $R_{\rm B}$ ), which can provide a more steady voltage reference for this output buffer.

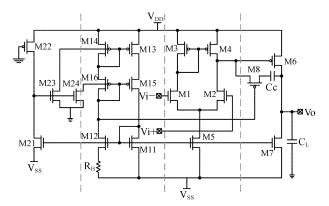


Fig. 1 The class-A analog output buffer with N-TFTs input stage

However, the bias circuit is a self-biasing circuit, it needs a start-up circuit (M21-M24) that turns on the bias circuit in the beginning and automatically be turned off

after bias circuit working.

Since there are two poles in this unity-gain output buffer circuit, the OP amp circuit needs frequency compensation to improve the phase margin and stability of the OP amp. In this work, the Miller compensation technique with nulling resistor (M8 and  $C_{\rm C}$ ) is adopted as frequency compensation circuit, which can provide a negative zero as

$$z = \frac{1}{(1/g_{m6} - R_C)C_C},$$
 (2)

where the resistor  $R_{\rm C}$  is implemented by using a P-type TFT (M8) biased in the triode region. Making the resistor greater than  $1/g_{\rm m6}$  moves the zero into the left half-plane (LHP), which can be used to provide positive phase shift at high frequencies and consequently to improve the phase margin of this output buffer. The simulated frequency response and circuit performances of this output buffer are shown in Fig. 2 and Table 1, respectively.

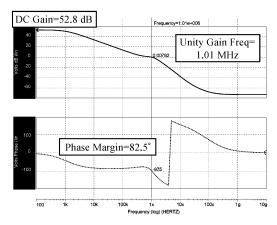


Fig. 2 The simulated frequency response of the class-A output buffer with N-TFTs input stage in open-loop condition

Tab. 1 Summary of the simulated circuit performances of the output buffer in Fig. 1.

Open-Loop Characteristics		
Differential Gain	52. 8 dB	
Phase Margin	82.5°	
Unity Gain Bandwidth	1.01 MHz	
CMRR	57.81 dB	
PSRR + ( - )	58.7 (62.2) dB	

Continuous

Close-Loop Characteristics		
Output Swing	1.8 ~ 9.2 V	
Slew Rate	1.510 V/μs	
Average Power Dissipation	1.386 mW	
Power Supply	$V_{DD} = 10 \text{ V}, V_{SS} = 0 \text{ V}$	

# 3 Output Buffer with Suppressing Device Variation

The average of mobility variation for n-channel and p-channel TFTs at different stress conditions are shown in Table 2<sup>[9]</sup>. From Table 2, the results show that the device characteristic variation of the N-type TFT is more serious than that of P-type TFT in LTPS technology. For this reason, replacing the critical part of the analog circuit by P-TFTs is a valid technique for suppressing device characteristic variation and improving the manufacturing yield of the analog circuit. In this output buffer, the differential pair is the critical part of the OP amp. The output buffer with P-TFTs input differential pair is proposed to suppress the device variation in this work.

Tab. 2 Mobility variation after stress<sup>[9]</sup>.

		Average Variation (%)	Std. Dev
Hot-Carrier	N-Channel	-38.627	6.65
Stress Condition P-Channel	+7.054	2.72	
On-Current	N-Channel	+11.828	3.28
Stress Condition P-Channel	+2.251	0.6525	

The proposed analog output buffer with P-TFTs input stage is shown in Fig. 3. These two OP amps (in Fig. 1 and Fig. 3) have the similar dc voltage gain, as shown in the following

$$A_{V}(0)_{N-input} = g_{m1-N} \cdot g_{m6-P} \cdot R_1 \cdot R_2, \quad (3)$$

$$A_{V}(0)_{P-input} = g_{m1-P} \cdot g_{m6-N} \cdot R_1 \cdot R_2, \qquad (4)$$

where  $R_1$  is the value of  $r_{o2}$  parallel with  $r_{o4}$  and  $R_2$  is the value of  $r_{o6}$  parallel with  $r_{o7}$ . From equations (3) and

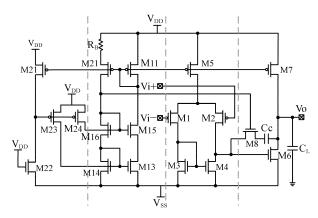


Fig. 3 The class-A analog output buffer with P-TFTs input stage

(4), the dc voltage gain of OP amp with P-TFTs input stage is almost similar to that of OP amp with N-TFTs input stage, when  $(W/L)_1$  and  $(W/L)_6$  are designed with the same device dimensions.

There are some advantages in the OP amp with P-TFTs input stage compared with the OP amp with N-TFTs input stage. The OP amp with P-TFTs input stage has larger unity-gain frequency since  $\omega_u \sim |p_2| = g_{m6}/C_L$  and  $g_{m6-N}$  is larger than  $g_{m6-P}$ . Furthermore, this OP amp with P-TFTs input stage also has better slew rate than the OP amp with N-TFTs input stage due to the larger unity-gain frequency in the OP amp with P-TFTs input stage. The OP amp with P-TFTs input stage also has more steady circuit performances, because the critical part (differential pair) of the OP amp is composed of the P-TFTs which have less device characteristic variation. The simulated frequency response and comparison on circuit performances are shown in Fig. 4 and Table 3, respectively.

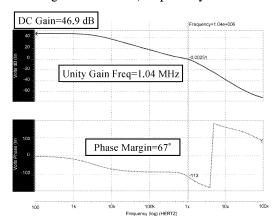


Fig. 4 The simulated frequency response of the class-A output buffer with P-TFTs input stage in open-loop condition

Tab. 3 Summary of the simulated circuit performances of the output buffers in Fig. 1 and Fig. 3.

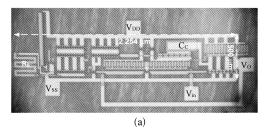
Open-Loop Characteristics				
Output Buffer Type	N-TFTs input stage OP amp	P-TFTs input stage OP amp		
Differential Gain	52. 8 dB	46.9 dB		
Phase Margin	82.5°	67°		
Unity Gain Bandwidth	1.01 MHz	1.04 MHz		
CMRR	57.81 dB	59.3 dB		
PSRR + ( -)	58.7 (62.2) dB	76.3 (52.3) dB		
Close-Loop Characteristics				
Output Swing	1.8 ~ 9.2 V	0.91 ~ 9.1 V		
Slew Rate	1.510 V/μs	1.885 V/μs		
Average Power Dissipation	1.386 mW	1.734 mW		
Power Supply	$V_{DD} = 10 \text{ V},$ $V_{SS} = 0 \text{ V}$	$V_{DD} = 10 \text{ V},$ $V_{SS} = 0 \text{ V}$		

Besides, the P-TFTs have less flicker noise (1/f noise) than that of N-TFTs, since holes are less likely to be trapped. For this reason, the proposed output buffer with P-TFTs input stage has better flicker noise (1/f noise) performance than that of the output buffer with N-TFTs input stage. Moreover, the proposed output buffer with P-TFTs input stage also has other advantages, such as larger slew rate, lower input offset voltage, and better immunity to noise, as comparing to the source follower output buffer. The proposed output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with an output voltage swing of 1-to-9 V.

### 4 Experimental Results

The class-A output buffers with N-TFTs input stage and P-TFTs input stage have been design and fabricated in a 8  $\mu$ m LTPS technology. The photographs of these buffers on glass substrate are shown in Figs. 5(a) and 5(b), respectively.

The measured results of slew rate and output swing



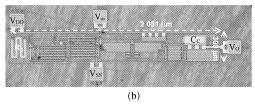


Fig. 5 The photographs of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage

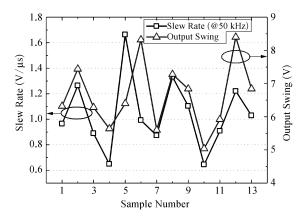


Fig. 6 The slew rate and output swing of the class-A output buffer with N-TFTs input stage, which are measured from 13 samples on glass substrate

among 13 class-A output buffers with N-TFTs input stage are shown in Fig. 6. The output buffer with N-TFTs input stage really has poor manufacturing yield and performance stability due to the wider device variation. The measured output waveforms of class-A output buffers with N-TFTs input stage and P-TFTs input stage are compared in Figs. 7 (a) and 7 (b), respectively, which are operating at 50 kHz. Obviously, the proposed output buffer with P-TFTs input stage has higher manufacturing yield and performance stability than those of the output buffer with N-TFTs input stage. The experimental results have proven that replacing the critical part of the analog circuit by P-TFTs is a valid technique for suppressing device characteristic variation on glass substrate.

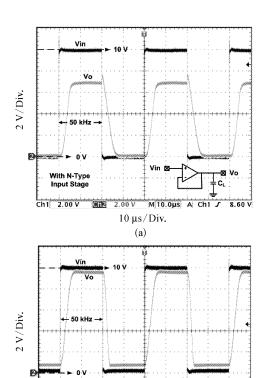


Fig. 7 The measured output waveforms of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage

 $10 \,\mu s/Div.$ 

### 5 Conclusions

2.00 V

A class-A output buffer with device variation suppressing technique in LTPS technology has been proposed and verified. The output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with at least 1-to-9 V output swing under  $V_{\rm DD}$  of 10 V and  $V_{\rm SS}$  of 0 V. The device characteristic variation has been successfully suppressed by replacing the critical part of analog circuits by the P-TFTs. The proposed output buffer with P-TFTs input stage can be used in the on-panel data drivers to provide a uniform brightness and high resolution display.

### Acknowledgments

This work was supported by the LTPS Design Department, Chunghwa Picture Tubes, LTD., Taiwan, China, and partially supported by the Ministry of Economic Af-

fair, Technology Development Program for Academia, China, under contract 95-EC-17-A-07-S1-046.

#### References

- [1] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Reliability of low temperature poly-silicon TFTs under inverter operation," *IEEE Trans. on Electron Devices*, vol. 48, No. 10, pp. 2370 2374, Oct. 2001
- [2] Y. M. Ha, "P-type technology for large size low temperature poly-Si TFT-LCDs," SID, Dig. Tech. Papers, 2000, pp. 1116-1119
- [ 3 ] Y. Nonaka, H. Haga, H. Tsuchi, Y. Kitagishi, T. Matsuzaki, M. Sugimoto, H. Hayama, and H. Asada, "A low-power SOG LCD with integrated DACs and a DC-DC converter for mobile applications," SID, Dig. Tech. Papers, 2004, pp. 1448 1451
- [4] S. H. Yeh, W. T. Sun, J. S. Yu, C. C. Chen, J. Lee, and C. S. Yang, "A 2.2-inch QVGA system-on-glass LCD using p-type low temperature poly-silicon thin film transistors," SID, Dig. Tech. Papers, 2005, pp. 352-355
- [ 5 ] Y. H. Tai, "Device variation and its influences on

- the LTPS TFT circuits," *International TFT Conference* 2005
- [ 6 ] S. C. Huang, G. F. Peng, J. L. Chern, and Y. H. Tai, "Statistical investigation on the variation behavior of low-temperature poly-Si TFTs for circuit simulation," *SID*, *Dig. Tech. Papers*, 2006, pp. 329–332
- [7] M. D. Ker, C. K. Deng, and J. L. Huang, "On-panel output buffer with offset compensation technique for data driver in LTPS technology," *IEEE J. Display Tech.*, vol. 2, No. 2, pp. 153-159, June 2006
- [8] S. I. Hsieh, H. T. Chen, Y. C. Chen, C. L. Chen, and Y. C. King, "Threshold voltage uniformity enhancement for low-temperature polysilicon thin-film transistors using tilt alignment technique," Electrochemical and Solid-State Lett., pp. H57—H60, 2006
- [9] W. Y. Guo, C. Y. Meng, A. Shih, and Y. M. Tsai, "Reliability of low temperature poly-Si thin film transistor," in *IDMC Tech. Dig.*, 2003
- [10] C. C. Pai and Y. H. Tai, "A novel analogue buffer using poly-Si TFTs for active matrix displays," in *IDMC Tech. Dig.*, 2005, pp. 483-486