

# A High-efficient Level Shifter Using Active Body-Bias Technique for LCD Driver in LTPS Technology

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## ABSTRACT

A high-efficient level shifter with active body-bias design has been proposed and implemented in a 6  $\mu\text{m}$  1P2M LTPS-TFT process. By using this active body-bias technique, the threshold voltage of the N-TFT of level shifter can be reduced during signal transition, and recovered after signal transition. The total delay time of the level shifter with the proposed active body-bias technique is at least one order smaller than that of the conventional level shifter, when input voltage level is less than 1.2 V.

## INTRODUCTION

With the high demand for portable systems such as IMT-2000 terminals, PDAs as well as notebook computers, driver circuits which are integrated in LTPS (Low Temperature Poly Silicon) TFT-LCD have recently been developed to reduce cost and complexity in manufacture. As that shown in Fig. 1, level shifters are the major circuit blocks of scan drivers and data drivers on the LCD panel. In order to implement the driving circuits on the glass in LTPS (Low Temperature Poly Silicon) technology, level shifters should be realized in LTPS first. However, there will be two problems to realize it in the future. First, the voltage level of logic input is getting lower and lower with the scaling of CMOS technology, and it may not be able to transit the level shifters in LTPS technology. Second, owing to poor driving ability of LTPS, the level shifters may not transit quickly enough when the pixels of a panel are increasing. Therefore, if the threshold voltage can be lowered during the transition period of level shifters, those above problems can be certainly solved. Some related ideas had been proposed in low-voltage high-speed SOI circuits [1]-[6].

In this work, the body-bias technique is first used in on-glass TFT circuits to improve the circuit performance of level shifters.

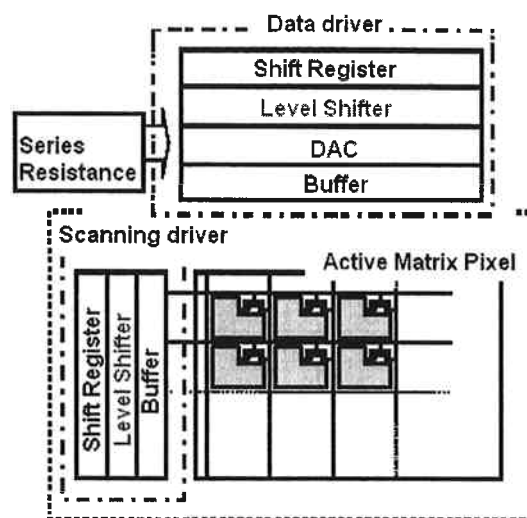


Fig. 1. Block diagram of TFT-LCD panel with integrated drivers.

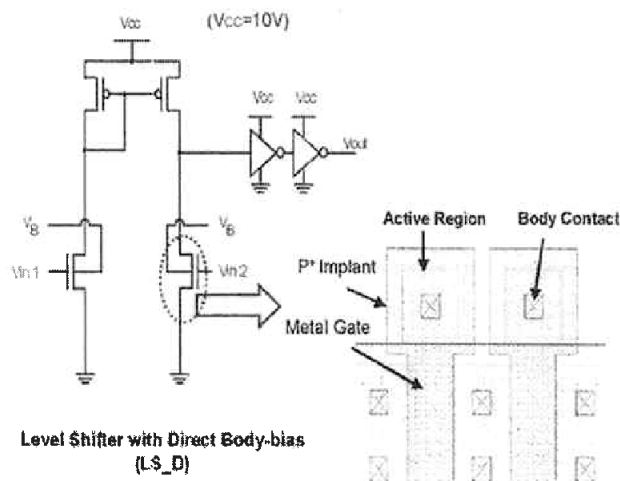
## NEW LEVEL SHIFTER

First of all, the functions of body bias on level shifter should be verified. Therefore, the level shifter with body bias directly connected to a DC voltage is under investigation. Fig.2 shows the circuit of level shifter with direct body bias (LS\_D) and the layout of body contact. Table 1 shows the major process parameters of this 6  $\mu\text{m}$  LTPS-TFT technology. Fig. 3 is the experimental setup for measuring circuit performance of LS\_D. The pulse generator creates an uncorrelated and differential input signal, and the output is connected to an oscilloscope. Besides, a power supply is used to generate the desired voltage level for biasing the body of the level shifter.

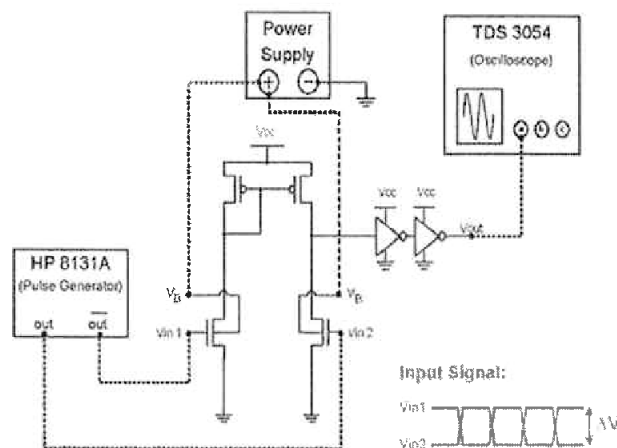
Table 1.

Device parameters of the LTPS-TFT technology.

	NMOS	PMOS
Zero-bias threshold voltage, $V_{T0}$	1 V	-1.4 V
High field mobility, $\mu_{U0}$	110 $\text{cm}^2/\text{Vs}$	80 $\text{cm}^2/\text{Vs}$

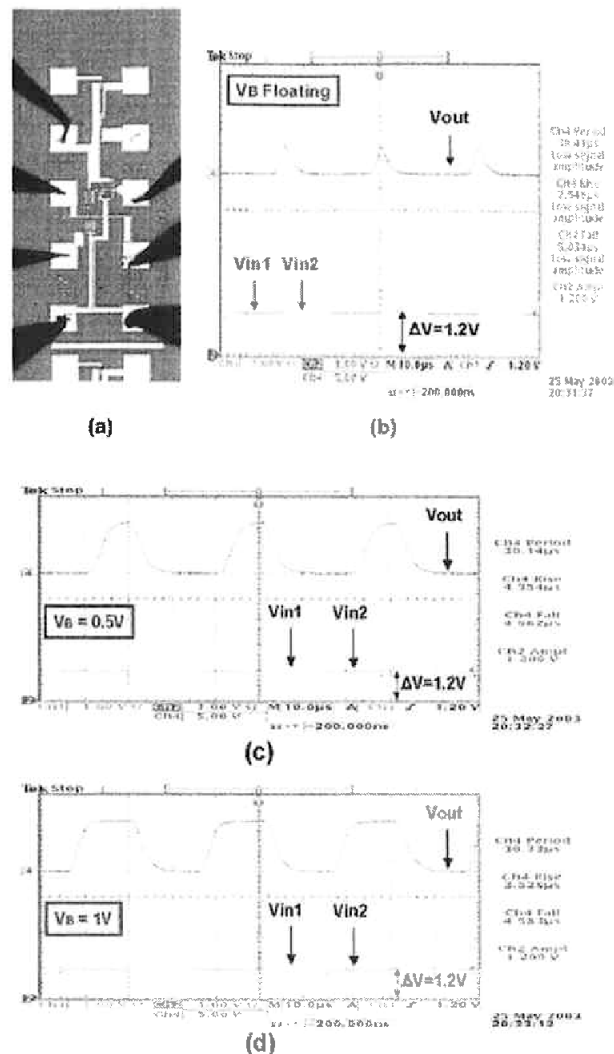


**Fig. 2. The circuit and layout of level shifter with direct body bias (LS\_D).**



**Fig. 3. Experimental setup for measuring circuit performance of level shifter with direct body bias (LS\_D).**

The probe-view microphotography to measure the level shifter with direct body bias through microscope is shown in Fig. 4(a). Fig. 4(b) shows the output waveform when the input swing is 1.2 V and the body of LS\_D is floating. Figs. 4(c) and 4(d) show the output waveforms when input swings are still 1.2 V, but the bodies are applied with 0.5 V and 1V DC voltage, respectively. Comparing with the waveforms in Fig. 4(b), the output waveforms in Figs. 4(c) and 4(d) are significantly improved. This has verified the effectiveness of body bias to improve circuit performance of the on-glass level shifter.



**Fig. 4. (a) Microphotography of probe view to measure the on-glass level shifter. (b) Output waveform of LS\_D when  $V_B$  is floating, (c)  $V_B=0.5V$ , and (d)  $V_B=1V$ .**

Furthermore, the maximum operating frequencies of LS\_D with different body-bias voltages are measured and shown in Fig. 5, when the input voltage is decreased step by step. According to Fig. 5, it is clearly illustrated that the maximum operating frequency of LS\_D is greatly improved by the body-bias technique, when the input differential voltage is below 1.5 V. For example, if the input differential voltage is 1.2 V, the maximum operating frequency of LS\_D is lower than 10 kHz with the floating body. Nevertheless, the maximum operating frequency can be improved more than 50 kHz with the body bias of 2 V. According to the measured results, the

LS\_D under body bias of 2 V can be operated at 49.3 kHz when input signal is only a 580 mV square wave. The level shifter operated at 48.4 kHz can be used in the scan driver for XGA resolution.

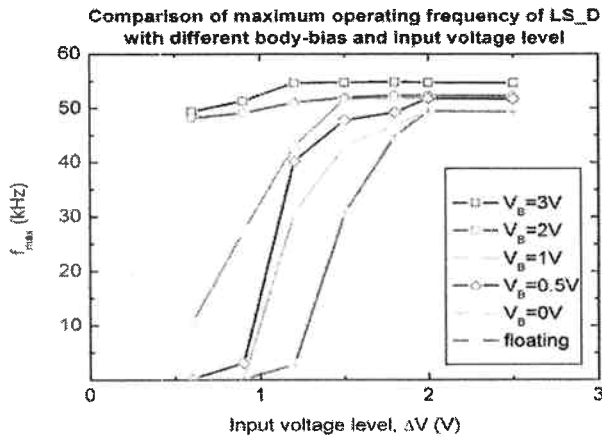


Fig. 5. Comparison of maximum operating frequency of level shifter (LS\_D) under different direct body-bias voltages.

Fig. 6 illustrates the relationship between body bias and differential input swing under different operating frequencies. For instance, in order to operate the level shifter with 50 kHz differential input signals under the body bias of 0 V, the minimum input differential voltage must be large than 1.8 V. However, when the body is biased at 2 V, the required minimum differential input voltage is only 0.6 V. Moreover, when the voltage applied to body is increased from 2 V to 3 V, the required minimum differential swing at each operating frequency is almost the same.

Since the function of body-bias technique has been verified, the circuit design for level shifter with active body-bias technique is also developed in this work. The mechanism of active body bias can lower the threshold voltage in active mode, when the input signals are transiting. In addition, the threshold voltage can be recovered in static mode, when the input signals remain unchanged. The conventional level shifter is shown in Fig. 7(a) as a reference, which is also fabricated in the same glass substrate in the LPTS technology. The proposed level shifter with active body bias (LS\_A) is shown in Fig. 7(b). In this circuit, the bodies of the main N-TFT, (Mn1 and Mn2), are connected to the sources of the auxiliary N-TFT, (Mn1\* and Mn2\*), respectively. The

size of auxiliary N-TFT is designed to be small to reduce the input capacitance of the level shifter.

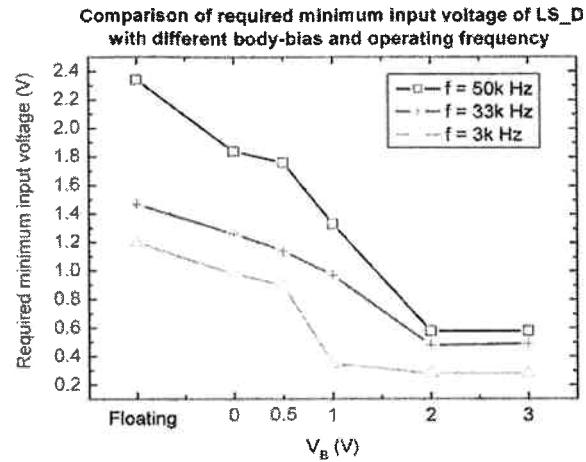


Fig. 6. Comparison of the required minimum input voltages of LS\_D under different body-bias voltages.

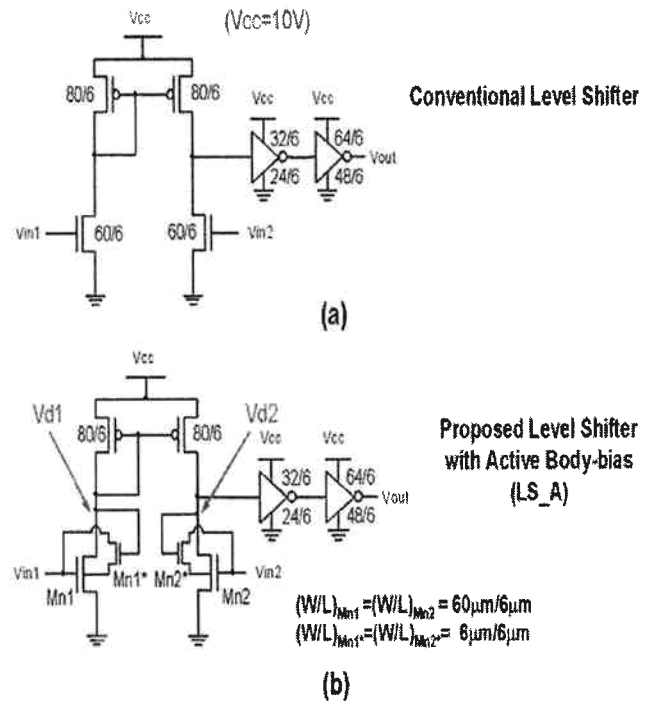


Fig. 7. (a) Conventional level shifter and (b) the new proposed level shifter with active body bias.

Initially, when Vin1 is "High" and Vin2 is "Low", Mn1\* is off and Mn2\* is weakly on. Therefore, the body potential of Mn1 is floating and Mn2 is "Low". On the other hand, when Vin1 falls from "High" to "Low" and Vin2 rises

from “Low” to “High”, both Mn1\* and Mn2\* are turned on in the meanwhile. Then, the body potential of Mn1 and Mn2 will be charged up. Owing to the body bias, the threshold voltage of Mn1 and Mn2 will be lowered, and then their drain currents will be enhanced. Also, the time for pull-down transition can be decreased because of the charge injection from Mn1\* (Mn2\*) and drain-to-body coupling effect of Mn1 (Mn2). After the signal transition, the Mn1\* and Mn2\* will be turned off and the threshold voltage of Mn1 and Mn2 will be recovered. By this way, no static power will be consumed when the transition is finished.

Similarly, the Mn2\* is off and Mn1\* is weakly on when Vin1 is “Low” and Vin2 is “High”. Thus, the body potential of Mn1 becomes “Low” and Mn2 begins floating. If the Vin1 rises from “Low” to “High” and Vin2 falls from “High” to “Low”, the body potential of Mn1 and Mn2 will be increased. That is due to the charge injection from Mn1\* (Mn2\*) and the drain-to-body capacitive coupling of Mn1 (Mn2). Therefore, the rising time of level shifter can be highly reduced. Of course, the threshold voltage of Mn1 and Mn2 will be recovered after the signal transition.

## EXPERIMENTAL RESULTS

The pull-down delay time and pull-up delay time are measured and summed as the total delay time of the level shifter in Fig. 8. The picture of the fabricated level shifter LS\_A on glass substrate is also shown in Fig. 8. The trend certainly fits that of prediction. When input differential signal level is larger than 2 V, the improvement between level shifters of LS\_A and conventional structure is not very strong. But, when the input differential swing is lowered, the total delay time of level shifter LS\_A is certainly less than that of conventional level shifter. Finally, According to the measured results, the total delay time of level shifter LS\_A is at least one order smaller than that of conventional level shifter, when the input signal is less than 1.2 V, especially.

## CONCLUSION

The function of body-bias technique to lower the threshold voltage of N-TFT has been successfully verified in a LTPS TFT technology. A high-efficient level shifter with active body-bias design to improve circuit

performance has been proposed and verified. The threshold voltage of the N-TFT of level shifter can be lowered during signal transition. After signal transition, the threshold voltage can be recovered. With an uncorrelated differential input signal, the total delay time of the new proposed level shifter with active body-bias technique has been measured, which is at least one order smaller than that of the conventional level shifter, when input voltage is less than 1.2 V.

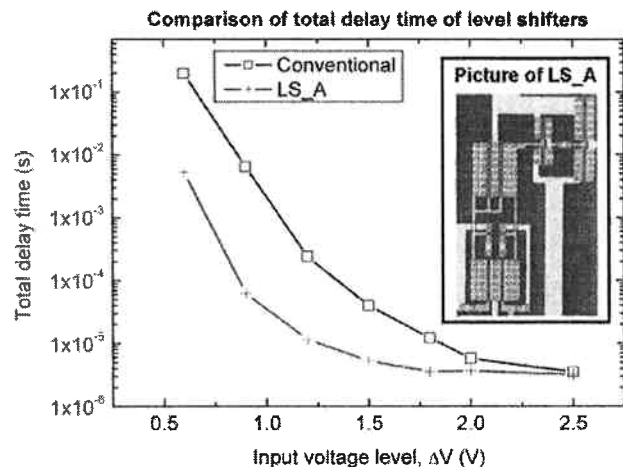


Fig. 8. Comparison of total delay between the conventional level shifter and the new proposed level shifter (LS\_A) with active body-bias technique.

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