Degradation of LTPS TFT Devices Caused by Electrostatic Discharge

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ABSTRACT

The impact of electrostatic discharge (ESD) on Low Temperature Poly-Si (LTPS) Thin-Film-Transistor (TFT) devices is investigated in this paper. The ESD-caused degradations on the on-current, the threshold voltage, and the subthreshold swing are measured after the transmission-line-pulsing (TLP) stresses with increasing zapping voltages. The variations of device parameters under the low-ESD-current and the high-ESD-current conditions are compared to find the degradation behaviors. The experimental results have confirmed that the TFT device for ESD protection must be drawn with a large enough device dimension to avoid serious degradation for safe protection operation.

INTRODUCTION

LTPS TFT devices have been widely used in active matrix liquid crystal display (AMLCD), because the electron mobility of the LTPS TFT device is about 100-times larger than that of the conventional amorphous silicon (α-Si) TFT device. The system on panel (SOP) is a main application for the LTPS TFT device in the near future with process progress [1]. Since the large glass insulating layer where TFT devices are fabricated on is the low thermal conductivity, the heat generated by large ESD current cannot be dissipated easily. For this reason, ESD reliability issues of LTPS TFT devices will become more serious, when more circuits are integrated on the panel. Some papers related to ESD degradation of TFT devices had been reported [2]-[6]. The TFT devices in those reports [4], [5] are not suitable for ESD protection applications, because such small -dimension device could not sustain high current when the ESD event is occurring. At the device level, the transmission line pulse generator (TLPG) system with a pulse width of 100 ns has been widely used to evaluate ESD robustness of the TFT device [5]. The purpose of this paper is to investigate the deterioration phenomena under forward and reverse TLP stresses on LTPS TFT devices with large dimensions.

DEVICE STRUCTURE AND FABRICATION

The LTPS TFT device with lightly doped drain (LDD) structure is shown in Fig. 1. The LDD length of the device is 0.8 μm which is the minimum design rule in the LTPS process of this work. The thickness of poly-Si film is 50 nm, and the effective oxide thickness (EOT) of gate insulator (SiN_X/SiO_X) is 100 nm. Mo is used as metal gate, and the channel length of TFT device is 10 μm. The layout of device is drawn in multiple-finger style with each unit finger width of 50 μm, and the total channel width is 600 μm for TFT device in the I/O or ESD protection applications. The transfer characteristic of TFT device has been measured, where the typical threshold voltage is about 1.1 V, the drain breakdown voltage is about 40 V, and the subthreshold swing is about 180 mV/decade.

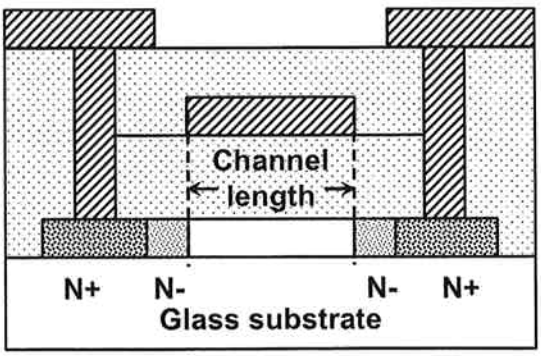

Fig. 1. The schematic cross-sectional view of LTPS TFT device.

The TFT device is zapped with step-by-step increasing TLP stresses to investigate the degradation of device characteristic. If the TLP (ESD) current is injected from drain to source with the gate of TFT device connected to source, the device is under reverse TLP stress. On the contrary, when the TLP (ESD) current is injected from source to drain, the device is under forward TLP stress. The schematic symbols of TFT devices under

forward and reverse TLP stresses are shown in Figs. 2(a) and 2(b), respectively. Between every two TLP stresses, the transfer characteristic of LTPS device is monitored in the linear regime by the HP4155B semiconductor parameter analyzer. The degradation is estimated from the behaviors of measured transfer characteristics. The threshold voltage (V_{TH}) is estimated at the gate voltage (V_{GS}) that required to achieve a normalized drain current of I_{DS} = (W/L) × 1 nA, when the drain voltage (V_{DS}) is 0.1 V [7]. The subthreshold swing (S) is measured as the maximum value of $\{\partial V_{GS}/\partial(\log_{10} I_{DS})\}$ at V_{DS} = 0.1 V. The turn-on current (I_{ON}) is extracted at V_{DS} = 0.1 V and V_{GS} = 10 V. The leakage current (I_{OFF}) is defined at V_{DS} = 0.1 V and V_{GS} = -2 V. All parameters are normalized to their corresponding initial values for comparison.

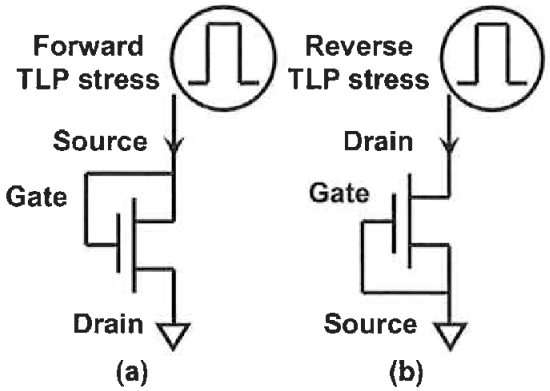

Fig. 2. The schematic symbols of TFT devices under (a) forward and (b) reverse TLP stresses.

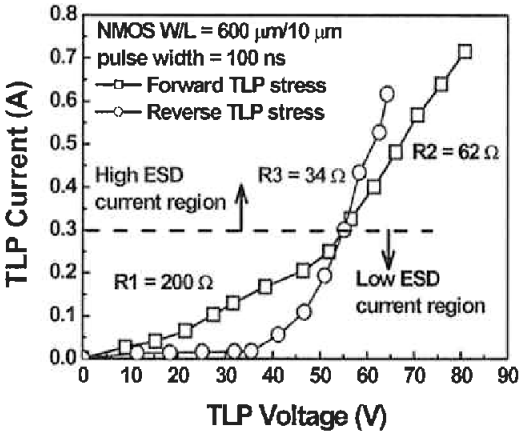

Fig. 3. The measured I-V curves of TFT devices under forward and reverse TLP stresses.

EXPERIMENTAL RESULTS

The TLP measured I-V curves of TFT devices under forward and reverse stresses are plotted in Fig. 3. The curves can be divided into two stages which represent different turn-on behaviors. Under the forward TLP stress, the turn-on resistance of the first stage in the low ESD current region is 200 Ω, but that of the second stage in the high ESD current region is about 62 Ω. The device almost has no TLP current before 40 V under reverse TLP stress. A too small TLP current through the TFT device zapped by reverse TLP voltage below 40V cannot be actually measured by the oscilloscope current probe (CT1) with a sensitivity of 5mV/1mA. Moreover, the turn-on resistance of TFT device under reverse TLP stress is about 34 Ω which is smaller than that under forward TLP stress, when the TLP current is over 0.3 A. When the ESD current is beyond 0.7 A, the device has visible damage from the microscope after both forward and reverse TLP stresses [8]. This visible damage can be seen as the secondary breakdown of device which is the permanent damage of device.

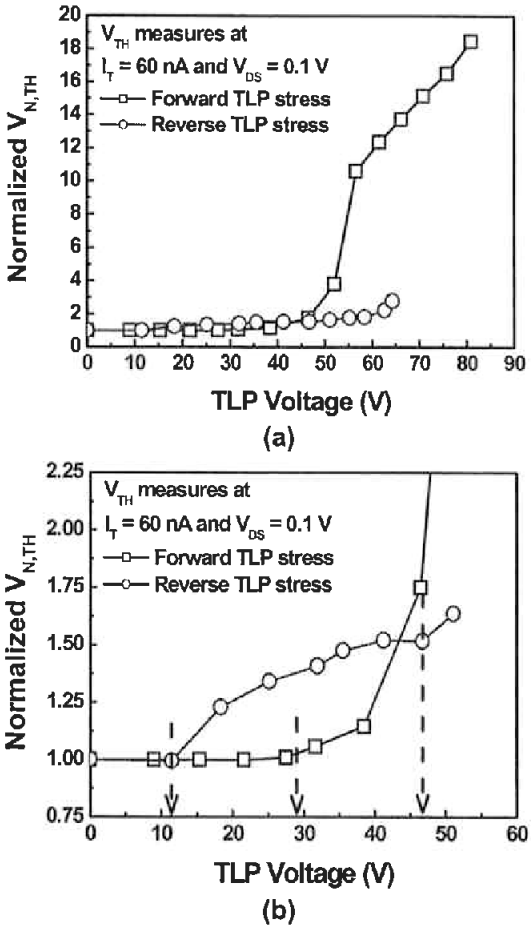

Fig. 4. Variations in the normalized V_{TH} of TFT devices during (a) the low-to-high TLP voltage range and (b) the low TLP voltage range.

Variations in the normalized threshold voltage, the normalized subthreshold swing, and the normalized turn-on current of TFT devices under forward and reverse TLP stresses are compared in Figs. 4(a), 5(a), and 6, respectively. Variations in the normalized V_{TH} and the normalized S of TFT devices in the low TLP voltage range are also shown in Figs. 4(b) and 5(b). When the TLP voltage

is below 30 V under forward TLP stress and that is below 10 V under reverse TLP stress, there are no obvious changes in all parameters (V_{TH}, S, and I_{ON}). Moreover, the device can sustain about 0.15 A TLP current under forward TLP stress, as shown in Fig. 3, without any variation of parameters. All parameters of the device under forward TLP stress begin to degrade, when the TLP voltage is beyond 30 V across drain and source.

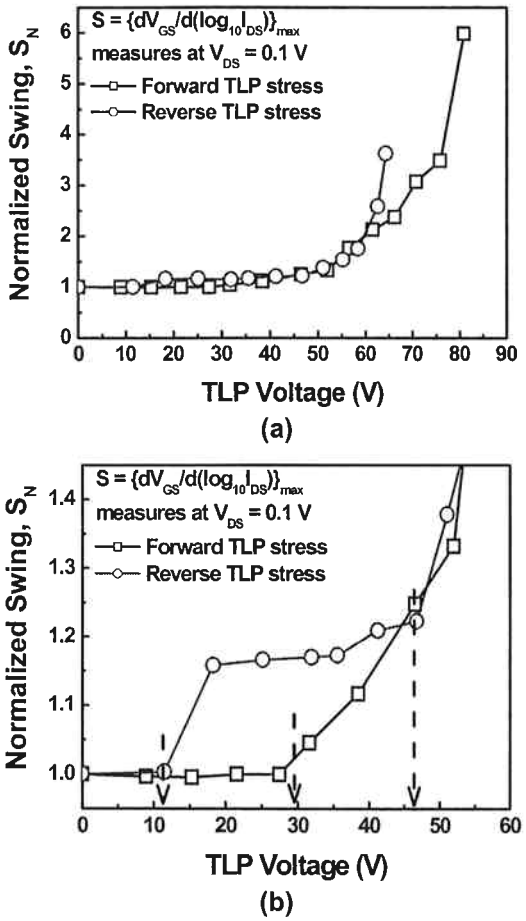

Fig. 5. Variations in the normalized S of TFT devices during (a) the low-to-high TLP voltage range and (b) the low TLP voltage range.

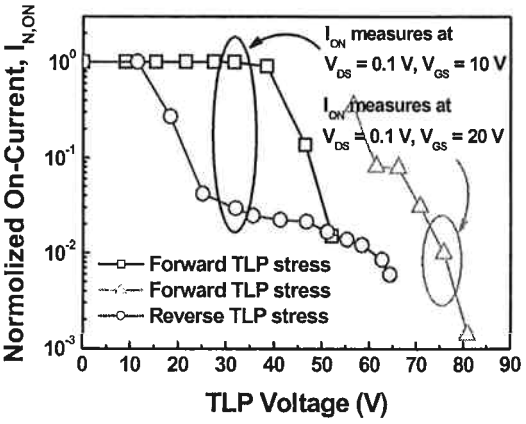

Fig. 6. Variations in the normalized I_{ON} of TFT devices under different TLP voltages.

The device under reverse TLP stress starts to conduct the TLP current by drain junction breakdown, until the TLP voltage is larger than 40 V. Fig. 6 shows that the turn-on current (I_{ON}) declines after 10 V, and then saturates after 30V under reverse TLP stress. From Figs. 4(b) and 5(b), the variations of V_{TH} and S are the same in those regions. As a result, the degradation mechanism under reverse TLP stress could be concluded that the interface state generation or the state generation in grain boundaries is located near the drain [9]. The tail states from grain regions in the gate insulator interface mainly cause the degradation of transconductance, and the transconductance is also in response to I_{ON} in the linear regime. Fig. 6 displays that the device under forward TLP stress between 30 V to 50 V has the same I_{ON} degradation as that under reverse TLP stress between 10 V to 30 V. This degradation under forward TLP stress between 30 V to 50 V range can be seen as the interface state generation or the state generation in grain boundaries, too.

It has been reported that the V_{TH} has a negative shift when the small-dimension α-Si TFT device with the nitride gate insulator is zapping by reverse TLP stress [10]. The negative V_{TH} shift can be attributed to the channel shorting effect by positive charges at the gate insulator interface, where increases inversion carriers to enhance effective mobility of the device. Different from previous experimental results [4], the V_{TH} and the S degradations observed in this study indicate that there are negative charges trapped at gate insulator/channel interface under reverse TLP stress. Those different shifting directions of the V_{TH} may be caused by different gate insulators (which are SiN_X/channel versus SiO_X/channel) and different grain sizes formation (which are solid phase crystalline versus excimer laser anneal).

Figs. 4(a) and 5(a) exhibit that both of V_{TH} and S increase greatly under forward TLP stress, until the device burns out with visible damage. V_{TH} shifts about 10 V under forward TLP stress with the stress voltage beyond 50 V. The turn-on current, which is measured at V_{GS} = 20 V after forward TLP stress, is depicted in Fig. 6, where it degrades with the increasing TLP voltage. Therefore, the degradation mechanisms under forward TLP stress are not dominated by interface state generation, but dominated by large number of negative charges injecting into the gate insulator. Besides, it has been reported that this shift is induced by joule heating [11]. This reason can be verified by V_{TH} shift of TFT devices with different channel lengths under high voltage stress. When the thermal heating is more serious in the TFT device with shorter channel length, the defect creation in the gate insulator plays a dominated role in deterioration mechanism [11].

This TFT device, which conducts ESD current under forward stress, would not turn on quickly again due to the large V_{TH} shift under previous large forward ESD current stress when the next ESD event occurs. The turn-on resistance of TFT device under low ESD current region (shown in Fig. 3) becomes larger than that under previous forward TLP stress. Therefore, the device needs more voltage drop to conduct the same forward ESD current. It leads ESD protection device easily to enter in the high ESD current region which causes large V_{TH} shift. To avoid large V_{TH} shift caused by electron injection into the gate insulator, the TFT device could not be subjected to such high forward-stress ESD current.

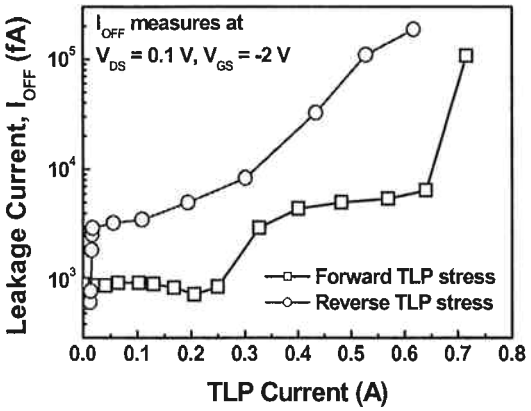

Fig. 7. Variations in the I_{OFF} of TFT devices under different TLP currents.

Fig. 7 reveals that the leakage current varies with TLP currents. There is no leakage current through gate insulator, when the TFT device is measured in the linear regime between every two TLP stresses. Fig. 7 also indicates that the leakage current increases monotonically, when the TLP current is over 0.3 A under reverse TLP stress, but it increases abruptly when the TLP current over 0.6 A under forward TLP stress. Besides, the variation of V_{TH} shown in Fig. 4(b) has no change, and that of S shown in Fig. 5(b) rises gradually, under small reverse TLP stress. Consequently, this degradation mechanism under reverse TLP stress can be attributed to the intra-grain defect generation near the drain junction. Moreover, the leakage current under large forward TLP current stress is lower than that under reverse TLP stress. The reason is that the degradation under large forward TLP current stress is dominated by large amount of electrons injection into the gate insulator but not by the junction breakdown. Under the normal circuit operation, the ESD protection device must be kept on off-state, and the leakage current should not affect the internal circuits operation. From the experimental results, this LTPS TFT device with a size (W/L) of 600μm/10μm only can sustain reverse ESD current below 0.3 A without causing a serious device degradation.

CONCLUSION

The degradation analysis on LTPS TFT devices due to TLP stress has been investigated in this paper. Both forward and reverse TLP stresses cause little interface states generation or state generation in grain boundaries during the low ESD voltage stress. When the large ESD current comes up, it would cause large negative charges injecting into the gate insulator during forward TLP stress, but cause intra-grain defect generation during reverse TLP stress. To obtain a good ESD robustness of LTPS TFT devices in output buffers, the size of LTPS TFT devices must be drawn large enough with an optimized layout.

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