# ESD Protection Design by Using Only 1×VDD Low-Voltage Devices for Mixed-Voltage I/O Buffers with 3×VDD Input Tolerance

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***Abstract* - A new electrostatic discharge (ESD) protection design by using only 1×VDD low-voltage devices for mixed-voltage I/O buffer with 3×VDD input tolerance is proposed. A special ESD detection circuit has been proposed to improve ESD protection efficiency of ESD clamp device by substrate-triggered technique to achieve high ESD level. This design has been successfully verified in a 0.13-μm CMOS process to provide an excellent circuit solution for on-chip ESD protection in the mixed-voltage I/O buffers with 3×VDD input tolerance.**

## I. Introduction

With the decrease of the power supply voltage for low-power applications, the thickness of gate oxide in advanced CMOS technologies has been scaled down to improve circuit performance and to increase circuit operating speed. For whole system integration, the I/O buffers must drive or receive high-voltage signals to communicate with other ICs in the microelectronic system. Thus, the I/O buffers should be designed with high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of the I/O devices [1]-[3]. To avoid gate-oxide reliability issue without using additional thick gate oxide process, the stacked NMOS configuration has been widely used in the mixed-voltage I/O buffers. However, the stacked NMOS configuration usually has a lower electrostatic discharge (ESD) level and slow turn-on speed of the parasitic lateral n-p-n device, as compared with the single NMOS [4]-[5]. The disadvantages result from the longer base width of the lateral n-p-n BJT in the stacked NMOS devices. Therefore, additional ESD protection design must be provided to protect the stacked NMOS in the mixed-voltage I/O buffer.

The mixed-voltage I/O buffer realized with only 1×VDD devices has been proposed to receive 3×VDD input signals without suffering gate-oxide reliability [6], where the ESD protection design was not considered. Recently, an ESD protection scheme with ESD bus for the 1.2/2.5-V mixed-voltage I/O buffer with only 1.2-V devices has been successfully verified in 0.13μm CMOS process [7]. However, ESD protection design for such mixed-voltage I/O buffer with 3×VDD input signals was not reported in the literature.

In this work, a new ESD protection design realized with only 1×VDD devices to protect the mixed-voltage I/O buffer with 3×VDD input tolerance is proposed. This new ESD protection design has an efficient ESD detection circuit to trigger on the ESD clamp device, so that the turn-on efficiency of ESD clamp device can be substantially increased. The proposed ESD protection design has been successfully verified in a 0.13-μm CMOS process.

## II. ESD Protection Scheme for 3×VDD Mixed-Voltage I/O Buffer

To improve ESD robustness of the mixed-voltage I/O interfaces, an ESD design concept by using the on-chip dummy ESD bus had been reported [8]. However, in this prior art, the gate-oxide reliability was not considered in its circuit design. With consideration on the gate-oxide reliability, the new ESD protection scheme for mixed-voltage I/O buffer with 3×VDD input tolerance is proposed in Fig. 1. The circuit design for 3×VDD I/O buffer has been reported in [6]. To receive the input signals with 3.3-V voltage level, the traditional ESD protection with direct diode connection from I/O pad to VDD of 1.2V is forbidden. Therefore, the ESD protection circuit is realized with diodes Dp, Dn, D1, ESD bus, ESD detection circuit, the ESD clamp device, and the power-rail ESD clamp circuit between VDD and VSS.

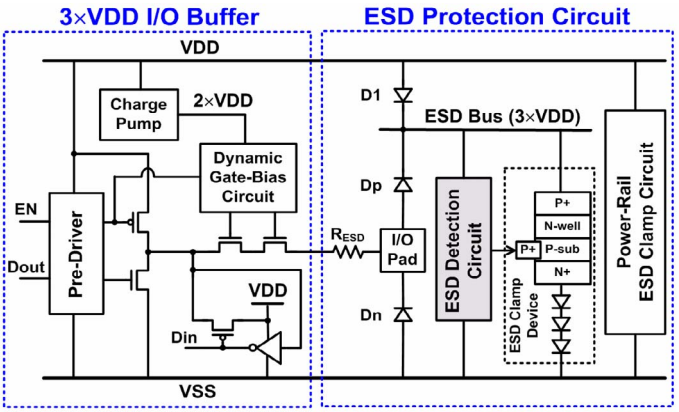


Fig. 1. The proposed ESD protection scheme for mixed-voltage I/O buffer with 3×VDD input tolerance realized with only 1×VDD devices.

Under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current can be discharged through the diode Dp to the ESD bus and then through the ESD clamp device (SCR) to the grounded VSS power line instead of through stacked NMOS in the I/O buffer to ground. Under positive-to-VDD (PD-mode) ESD stress on I/O pad, the ESD current can be discharged through Dp, ESD bus, and the ESD clamp device to VSS power line, and then through the power-rail ESD clamp circuit

between VDD and VSS to grounded VDD power line. Under negative-to-VSS (NS-mode) ESD stress on I/O pad, the negative ESD current can be discharged through the diode Dn in forward-biased condition to the grounded VSS power line. Under negative-to-VDD (ND-mode) ESD stress on I/O pad, the negative ESD current can be discharged through Dn to the floating VSS power line, and then through the power-rail ESD clamp circuit between VDD and VSS to the grounded VDD power line. The four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the proposed ESD protection scheme. The $R_{ESD}$ in Fig.1 should be designed a little larger than some critical value (~10Ω), so that most ESD current is discharging through the diode Dp, ESD bus, and the ESD clamp circuit with ESD detection circuit to the grounded VSS under the PS-mode ESD stress. Therefore, the stacked NMOS in the mixed-voltage I/O interface will not be damaged. Moreover, the pin-to-pin ESD stress can be effectively discharged through the proposed ESD protection scheme.

The power-rail ESD clamp circuit between VDD and VSS can be realized by the traditional RC-based ESD detection circuit. The silicon control rectifier (SCR) device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback, with a low holding voltage can sustain a high ESD level within a small silicon area in CMOS technology. However, the main concerns of the SCR device as the ESD clamp device are the slow turn-on speed, high switching voltage, and latch-up issue [9]. To solve the latch-up issue, three diodes are added in series with SCR as the ESD clamp device to increase its overall holding voltage for such (3.3-V) mixed-voltage I/O buffer. To avoid the damage of I/O buffer before ESD clamp device is turned on, the substrate-triggered technique is used to quickly trigger on the ESD clamp device. Because ESD bus line will be biased at 3.3V through the diode Dp when 3.3-V input signals reach to the I/O pad, the ESD detection circuit connected between ESD bus and VSS must sustain the high-voltage (3.3V) stress during normal circuit operating condition. Some ESD detection circuits proposed to increase the turn-on speed of SCR device will suffer gate-oxide reliability issue under 3.3-V bias with only 1.2-V low-voltage devices [9]-[10]. Therefore, how to design a turn-on-efficient ESD detection circuit with only 1.2-V devices to sustain 3.3-V bias becomes a quite significant challenge to this 1.2/3.3-V mixed-voltage I/O buffer.

## III. 3×VDD-Tolerant ESD Clamp Circuit

The ESD detection circuit that can be operated under 3.3-V bias with only 1.2-V low-voltage devices is shown in Fig. 2. Under normal circuit operating condition, the diode-connected PMOS (Mp1~Mp3) are used as the voltage divider to bias the substrate driver (Mn1, Mp4, and Mp5) of the ESD detection circuit, where a deep N-well is used in Mn1 to avoid the gate-oxide overstress between gate and bulk. The NMOS (Mn2) is used to keep the voltage level of the trigger node at VSS, so the ESD clamp device is turned off in the normal circuit operating condition. Here, the RC time constant of R1 and Mp7 should be designed around the order of ~1μs to distinguish the normal circuit operating condition from the ESD transition.

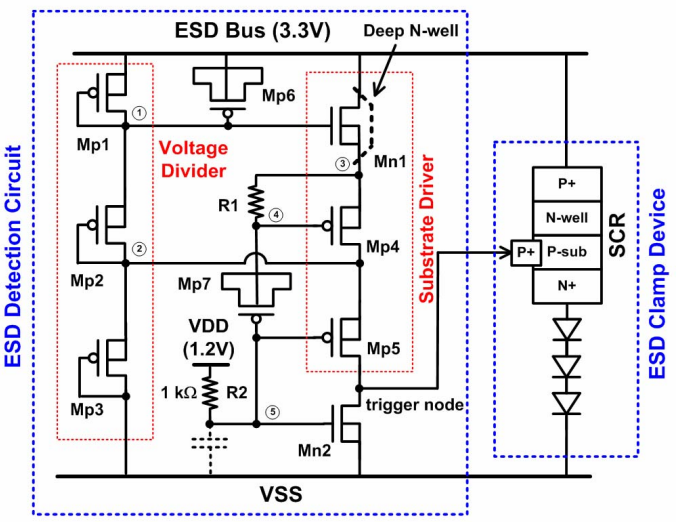


Fig. 2. Circuit implementation of the 3×VDD-tolerant ESD clamp circuit realized with 1×VDD devices.

### A. Circuit Operation under Normal Power-on Transition

During normal circuit operating condition with 1.2-V VDD power supply, when a 3×VDD (3.3-V) input signal applied to the I/O pad, the voltage level at ESD bus will be charged up to 3.3V, and then the node 1 and node 2 in the ESD detection circuit will be biased at 2.2V and 1.1V, respectively. The node 5 is biased at 1.2V through the 1kΩ resistor of R2 to VDD, so that Mp5 is turned off. There is no trigger current generated from the ESD detection circuit into the ESD clamp device. In addition, the Mn2 in the turned-on state, whose gate is connected to VDD through the resistor of R2, can increase the noise margin of the ESD detection circuit to guarantee the ESD clamp device against false triggering during the normal circuit operating conditions. All devices in the proposed ESD detection circuit with 1.2-V gate oxide can be free from gate-oxide reliability issue under the ESD bus of 3.3V.

In this ESD detection circuit, the drain-to-gate voltage of Mn1 is (3.3V-2.2V), where Mn1 is working at inversion region under the normal circuit operating conditions. But the induced channel region of Mn1 could be insufficient to shade the strength of the electric field across the gate and bulk if its bulk region is grounded. In other words, there could be gate-oxide reliability concern on the gate of Mn1 if its bulk is grounded. Therefore, to avoid this possible issue, the bulk of Mn1 is connected to its own source node. To avoid the leakage current path through the bulk (p-well) of Mn1 to the grounded p-substrate, the bulk (p-well) of Mn1 is isolated by the deep N-well with 3.3-V bias from the common p-substrate, as the diagram shown in Fig. 3. Fig. 3 also marks with the Spice-simulated voltages at the nodes of the ESD detection circuit during normal circuit operating condition. From these simulated voltages, the voltages between each two adjacent nodes of devices do not exceed their voltage extreme (1.32V for 1.2-V devices). Therefore, the ESD detection circuit is free from the gate-oxide reliability issue.

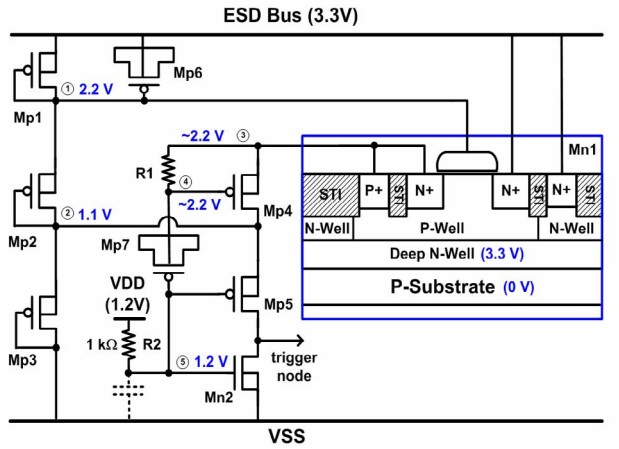


Fig. 3. Cross-sectional view of NMOS Mn1 and the Spice-simulated voltages at the nodes of ESD detection circuit under the normal circuit operating condition.

### *B. Circuit Operation under ESD Transition*

When ESD voltage is applied to the I/O pad with VSS relatively grounded, such ESD transient voltage will be conducted into ESD bus through the Dp diode in forward-biased condition. Therefore, the ESD bus will have a fast rising-up ESD voltage. The capacitor (Mp6) will couple some ESD transient voltage to the node 1 to turn on Mn1 and to pull up the node 3. The RC delay from R1 and Mp7 in the ESD detection circuit will keep the gate of Mp4 (node 4) at a relatively low voltage level compared to the node 3 for a long time. The VDD is initially floating with an original voltage level of 0V during a PS-mode ESD stress at I/O pad. Some ESD transient voltage would be coupled to VDD through the parasitic capacitance during ESD zapping, but the R2 and the parasitic capacitance at the gates of Mp5 and Mn2 will hold the gate of Mp5 at a low voltage level for a long time to keep Mp5 in on state. Therefore, Mp4 and Mp5, whose initial gate voltages are at low voltage level, can be quickly turned on by ESD energy to generate the substrate-triggered current into the substrate of SCR. Then, the ESD clamp device can be quickly triggered on to discharge ESD current from ESD bus to VSS.

Fig. 4 shows the Spice-simulated voltages and the substrate-triggered current of the ESD detection circuit under ESD transition. A 0-to-6V ESD-like voltage pulse with a rise time of 10ns is applied to the ESD bus to simulate the ESD transient voltage. The Spice-simulated results show that the gate voltage of Mn1 (node 1) is quickly pulled high through Mp6 and the gate voltage of Mp4 (node 4) is kept low due to the RC time delay from R1 and Mp7. Therefore, the ESD clamp device can be triggered on to discharge ESD current from ESD bus to VSS. The substrate driver can provide the substrate-triggered current larger than 35mA within 10ns when the 0-to-6V transient voltage is applied to ESD bus, as shown in Fig. 4.

## IV. Experimental Results

The proposed ESD protection design has been fabricated in a 0.13-μm CMOS process with only 1.2-V devices. The active areas of the 1.2/3.3-V mixed-voltage I/O buffer and the proposed ESD protection circuit are 70μm×150μm and 30μm×150μm, respectively. However, the proposed ESD protection circuit can be shared with other mixed-voltage I/O cells which have the same input/output voltage levels. Therefore, the layout area increased by adding the proposed ESD protection circuit will not be a major concern in whole chip design.

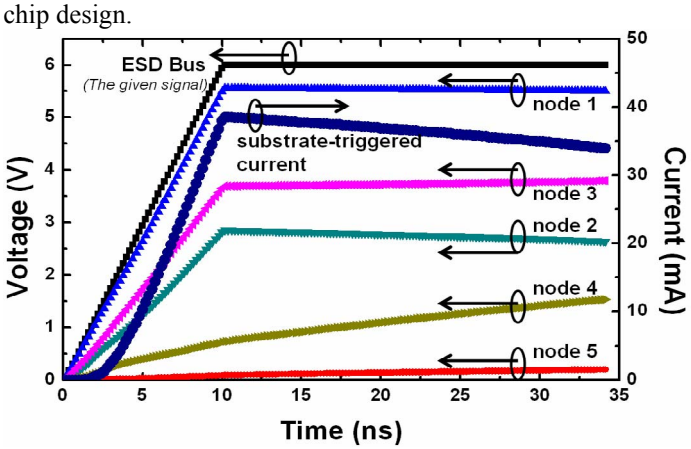


Fig. 4. Spice-simulated voltages on the nodes of ESD detection circuit and the substrate-triggered current through Mp5 under 0-to-6V ESD-like transition on ESD bus.

### *A. Turn-on Verification*

To verify the effectiveness of the proposed ESD detection circuit, a measurement setup is shown in the inset of Fig. 5 to observe the substrate-triggered current generated by the ESD detection circuit. In the specially drawn testchip, the trigger node of the ESD detection circuit and the substrate trigger node of the ESD clamp device are separately connected to different bond pads, and then wired to each other with a current probe on it, for measuring the transient current. With such measurement setup, the measured substrate-triggered current generated by the ESD detection circuit under a 0-to-6V voltage pulse with a rise time of 10ns on the ESD bus is shown in Fig. 5. The substrate-triggered current appears simultaneously with a peak current of ~35mA, when the 0-to-6V voltage pulse is applied to ESD bus. So, the ESD clamp device with ESD detection circuit can be quickly triggered on to clamp the overstress ESD voltage.

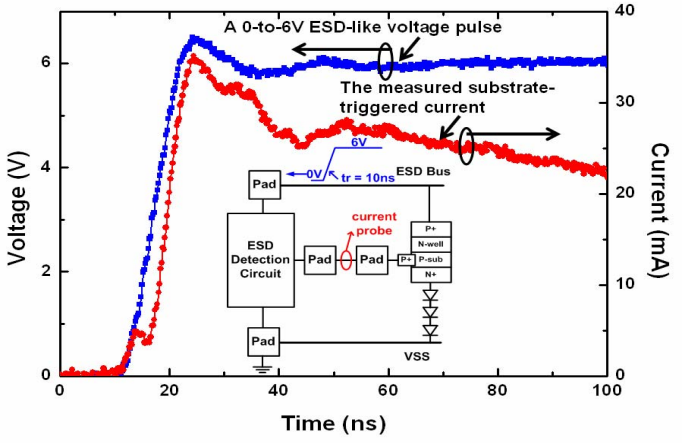


Fig. 5. The measured substrate-triggered current generated by the ESD detection circuit under a 0-to-6V ESD-like voltage pulse with a rise time of 10ns on the ESD bus.

Fig. 6 shows the measured voltage waveforms under PS-mode ESD event and under normal circuit operating condition with overshooting noise pulse while applying a 0-to-6V voltage pulse with a rise time of 10ns to I/O pad. During PS-mode ESD event (VDD is floating), the overshooting voltage waveform at I/O pad is clamped by the Dp and ESD clamp device to ~4V, which is lower than the breakdown voltage of the stacked NMOS in the mixed-voltage I/O buffer. The time to clamp the 0-to-6V voltage pulse to the holding voltage level (~4V) by the ESD clamp device is about ~20ns. So, the 3×VDD I/O buffer can be effectively protected by the proposed ESD protection design. Under normal circuit operating condition (VDD is 1.2V), the voltage waveform at I/O pad is still kept at 6V, so the ESD clamp device is not triggered on even with an overshooting noise at I/O pad. Therefore, from the measured voltage waveform in Fig.6, the excellent turn-on efficiency and noise immunity of the proposed ESD protection design has been successfully verified.

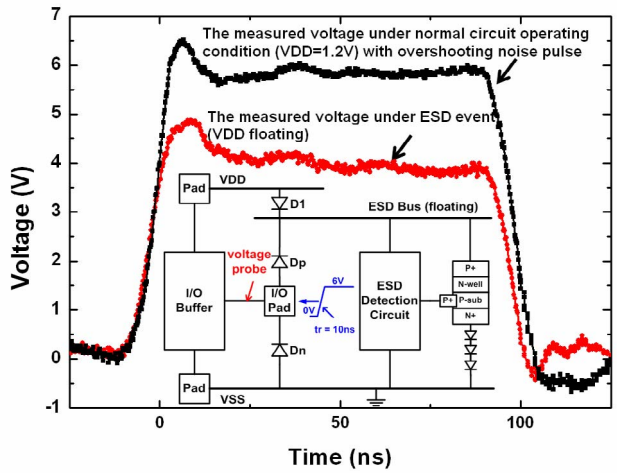


Fig. 6. The measured voltage waveforms at I/O pad by applying a 0-to-6V overshooting voltage pulse to I/O pad under PS-mode ESD event (VDD floating) and normal circuit operating condition (VDD = 1.2V).

### *B. ESD Robustness*

The TLP-measured secondary breakdown current (It2) and human-body-model (HBM) ESD level of the I/O buffer with and without the proposed ESD protection under PS-mode ESD stress are compared in Table I. The HBM ESD levels are measured by *KeyTek ZapMaster* and the failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level. When the width of SCR device in ESD clamp device is 45μm, the secondary breakdown current (It2) of the I/O buffer with the proposed ESD protection scheme can be increased from 0.2A to 4A, as comparing with the I/O buffer without ESD protection. In addition, the HBM ESD level of the I/O buffer with the proposed ESD protection scheme can be improved from 500V to 6kV. When the width of SCR device in ESD clamp device is increased to 90μm, the It2 and HBM ESD level of the I/O buffer with the proposed ESD protection scheme can be further increase to larger than 6A and 8kV, respectively. Therefore, the proposed ESD protection scheme can significantly improve the It2 and HBM ESD level of the I/O buffer.

TABLE I
ESD ROBUSTNESS OF I/O BUFFER WITH OR WITHOUT ESD PROTECTION

| 3×VDD I/O Buffer | It2 | HBM ESD Level |
|---|---|---|
| I/O Buffer without ESD Protection Circuit | 0.2A | <500V |
| I/O Buffer with ESD Protection Circuit (SCR Width = 45μm) | 4A | 6kV |
| I/O Buffer with ESD Protection Circuit (SCR Width = 90μm) | >6A | >8kV |

## V. CONCLUSION

A novel circuit solution on ESD protection design realized with 1×VDD devices for mixed-voltage I/O buffer with 3×VDD input tolerance and single VDD supply has been successfully verified in a 0.13-μm CMOS process. The four-mode (PS, NS, PD, and ND) ESD stresses and pin-to-pin ESD stresses on the 1.2/3.3-V mixed-voltage I/O buffer can be effectively discharged by the proposed ESD protection scheme without gate-oxide reliability issue. The turn-on behavior of the ESD clamp device has been measured to verify the effectiveness of the ESD detection circuit. The experimental results have confirmed that the ESD robustness of the 3×VDD mixed-voltage I/O buffer can be significantly increased up to 8kV with the proposed ESD protection scheme.

## ACKNOWLEDGMENT

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