

New Matching Methodology of Low-Noise Amplifier with ESD Protection

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Abstract—A new matching design of Low-Noise Amplifier (LNA) with ESD protection is proposed and implemented in an ESD-protected LNA, which manipulates the parasitic capacitance of ESD protection device as a core part of LNA matching network. Without significant degradation on RF performance, 4.5-kV Human-Body-Model (HBM) and 250-V Machine-Model (MM) ESD levels can be achieved. The low RF-performance degradation and high ESD immunity can be simultaneously realized in a simple matching structure without extra circuit components dealing with ESD parasitics in a multi-GHz LNA.

I. INTRODUCTION

RF IC rapidly evolves in wireless communication during recent years. Every IC product has to include ESD protection for good production yield and reliability, so does RF IC. LNA is located on the front stage of RF receiver and usually equipped with on-chip ESD protection circuit. Inducing parasitics such as dominant parasitic capacitance, ESD protection device may severely degrade the RF performance. To alleviate such influence, co-design strategies of LNA with ESD protection have been developed. Low-capacitance ESD devices with power-rail ESD clamp circuit has been proved as an effective solution [1]. As LNA operates at higher frequencies, another bottleneck emerges. Parasitic capacitance of proper-sized ESD protection devices cannot be reduced unlimitedly. The limitation causes difficult trade-off between RF performance and ESD immunity. Since ESD device is attached to the input-signal path of LNA, input matching becomes a challenge in LNA that operates at frequency of multi-GHz.

Circuit solution in co-design strategies exists as an important role to deal with the parasitic capacitance for multi-GHz LNA. Inductive-degeneration architecture is a typical LNA structure that can provide proper input impedance for matching [2]. Two classified techniques, matching compensation and inductor resonance, were employed to overcome the input matching issue for the typical LNA structure [3],[4]. The circuit solutions help LNA capable to perform adequate input matching condition and enough ESD immunity. However, these two approaches

complicate the matching structure and need extra components for implementation. One off-chip capacitor and one on-chip spiral inductor are required, respectively. Additionally, complicated matching network could significantly degrade RF performance of LNA.

A new matching design is proposed in this work to simplify the matching structure of LNA with ESD protection. Handling parasitic capacitance of ESD device as a substantial matching component, this design does not complicate the matching network and does not require extremely low-capacitance ESD device. ESD devices can be designed without too small dimensions for high ESD immunity. An ESD-protected LNA was also successfully implemented to verify the new proposed methodology. Experimental results prove that not only the adequate input matching is achievable, but the maximum-gain and noise-figure degradations are merely 0.5 dB. Besides, the LNA can sustain 4.5-kV human-body-model (HBM) and 250-V machine-model (MM) ESD stresses.

II. CONVENTIONAL MATCHING TECHNIQUES OF LNA WITH ESD PROTECTION

One of the useful methods is matching compensation, which can successfully mend degraded input matching due to parasitic capacitance of ESD protection device [3]. The technique is illustrated in Fig. 1. The real part of impedance Z_{i1} is designed at 50 Ω . Parasitic capacitance $C_{P,ESD}$ of ESD protection device and input pad moves Z_{i1} to another impedance A, causing the real part below 50 Ω . L_G adjusts impedance A to a proper value B via the A-B path. Ultimately, extra capacitor C_C compensates the impedance toward 50 Ω via B- Z_{i2} path, shown in Fig. 1(b).

Inductor resonance is the other matching technique [4]. As shown in Fig. 2, the real part of Z_{i1} is designed at 50 Ω as well. There exist two functions on inductor L_T , drawing off ESD current and tuning out parasitic capacitance $C_{P,ESD}$. Resonance of L_T and $C_{P,ESD}$ generates high impedance so that the parasitic effect is almost negligible. L_G subsequently eliminates the imaginary part of Z_{i1} toward Z_{i2} of 50 Ω .

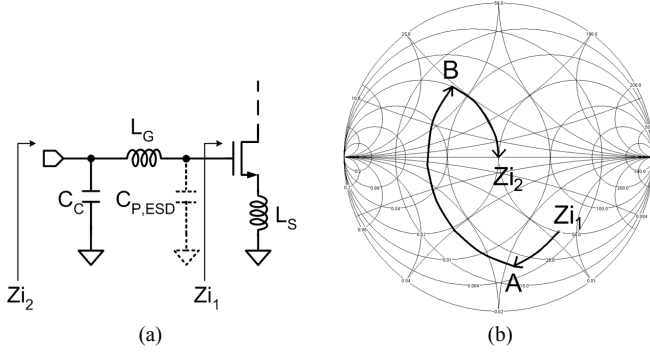


Fig. 1. (a) Circuit schematic and (b) Smith-chart illustration of matching compensation [3].

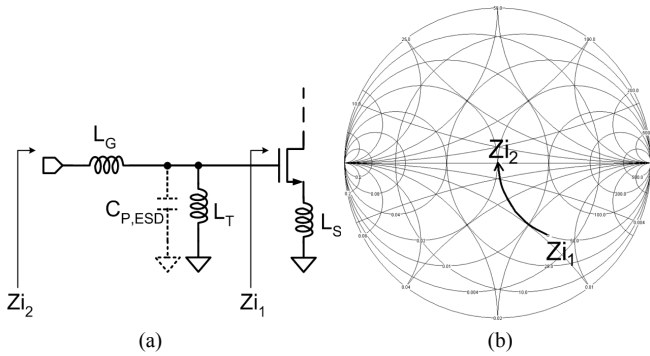


Fig. 2. (a) Circuit schematic and (b) Smith-chart illustration of inductor resonance [4].

Extra circuit components are necessary to implement these two techniques. One more off-chip capacitor was added on the input-signal path to compensate the input matching [3]. One more spiral inductor was laid on chip and occupied a large chip area [4]. The passive components before the input-stage transistor of LNA not only complicate the matching structure but also likely cause notable RF-degradation such as gain or noise figure.

III. NEW PROPOSED MATCHING METHODOLOGY OF LNA WITH ESD PROTECTION

Fig. 3 illustrates an idea of the new matching methodology. The real part of Z_{i1} is well known as the following formula.

$$\text{Re}\{Z_{i1}\} = \frac{g_m}{C_{gs}} \cdot L_S$$

g_m and C_{gs} respectively denote the transconductance and parasitic gate capacitance of the MOS transistor. The real part of Z_{i1}' , including $C_{P,ESD}$ term, is considered to be 50Ω . According to the next formula presenting the real part of Z_{i1}' , the real part of Z_{i1} should be designed at a value over 50Ω . For a given MOS transistor that is identical to those in Fig. 1 and Fig. 2, the value and location of Z_{i1} on Smith chart can be varied by different L_S designs. $C_{P,ESD}$ is anticipated to change Z_{i1} to Z_{i1}' , as shown in Fig. 3. L_G subsequently eliminates the imaginary part via the Z_{i1}' - Z_{i2} path to complete the input matching. Precise parasitic-capacitance estimation on ESD protection device and input pad is

essential for this approach, because exact designed value on the real part of Z_{i1} depends on $C_{P,ESD}$ capacitance.

$$\text{Re}\{Z_{i1}'\} = \frac{\left[\left(\frac{g_m}{C_{gs}} \cdot L_S \right)^2 + \left(\omega \cdot L_S - \frac{1}{\omega \cdot C_{gs}} \right)^2 \right] \cdot \left(\frac{g_m}{C_{gs}} \cdot L_S \right)}{\left(\frac{g_m}{C_{gs}} \cdot L_S \right)^2 + \left\{ \omega \cdot L_S - \frac{1}{\omega \cdot C_{gs}} - \left[\left(\frac{g_m}{C_{gs}} \cdot L_S \right)^2 + \left(\omega \cdot L_S - \frac{1}{\omega \cdot C_{gs}} \right)^2 \right] \cdot C_{P,ESD} \right\}^2}$$

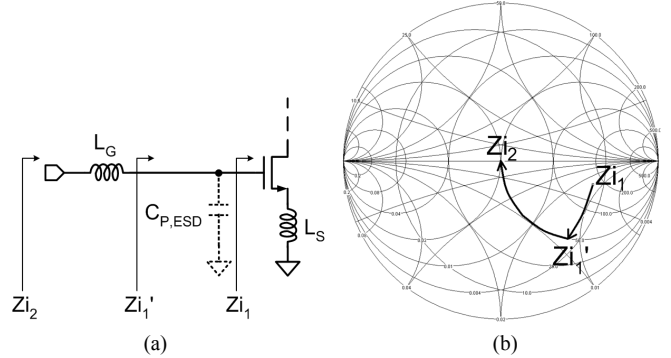


Fig. 3. (a) Circuit schematic and (b) Smith-chart illustration of the new proposed matching approach.

There exists a conceptual difference between the conventional techniques and the new matching methodology. The conventional techniques compensate or tune out the effect of parasitic capacitance $C_{P,ESD}$. The new matching methodology directly manipulates the parasitic capacitance as a substantial component of the input matching network. Extra circuit components and extremely low parasitic capacitance are not stringently required. ESD protection circuit can be properly designed with larger-dimension device to effectively enhance ESD immunity of LNA.

IV. IMPLEMENTATION IN AN ESD-PROTECTED LNA

A 2.4-GHz LNA with ESD protection circuit was implemented by the new proposed matching design in 0.25- μm CMOS process. The schematic is shown in Fig. 4. M1 dimension was particularly designed for noise optimization because that dominantly determines noise performance of LNA [2]. M2 of the cascode structure was employed to enhance reverse isolation and alleviate Miller effect. R1 is required to protect M2 gate from ESD pulse. The whole input matching stage comprises M1, L_S , parasitic capacitance of ESD devices D_{pi} and D_{ni} , parasitic capacitance of input pad, parasitic inductance of input bondwire, and an off-chip inductor. The off-chip inductor belongs to a part of the typical matching structure of LNA, not an extra circuit component. Parasitic inductance of the bondwire can be combined to the off-chip inductor. Transconductance of M1 and resonant impedance of L_d and C_d generate gain. M3, R2, C_b , D_{po} and D_{no} were designed as parts of output buffer for measurement. The four I/O ESD diodes were realized in P+/N-well or N+/P-well structures. The power clamp, shown in Fig. 5, comprises an ESD-detection circuit and a substrate-triggering field oxide device (STFOD) to provide an effective ESD path between V_{DD} and

V_{SS} [5]. A well-designed power clamp quickly turns on and discharges ESD current to prevent ESD overstress from damaging internal circuits. The turn-on simulation, shown in Fig. 6, illustrates the ESD detection-circuit that outputs sufficient current to trigger STFOD.

As shown in Fig. 4, no extra circuits component are required to deal with the parasitic capacitance of ESD protection devices. According to the analysis in the new matching design, even if D_{pi} , D_{ni} , and input pad introduce the parasitic capacitance up to 0.5 pF to M1 gate node, an adequate value of input impedance is available.

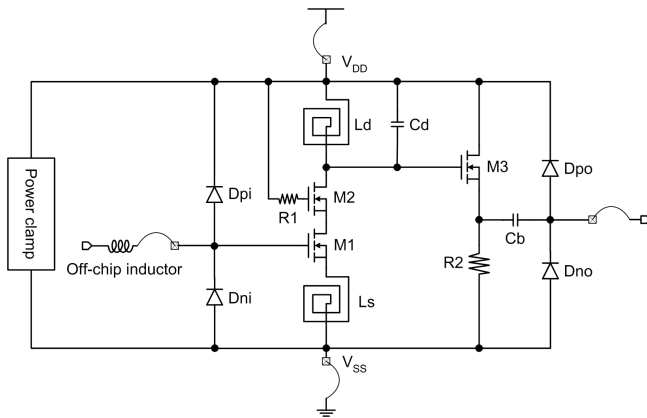


Fig. 4. Schematic of the ESD-protected LNA with ESD protection circuit.

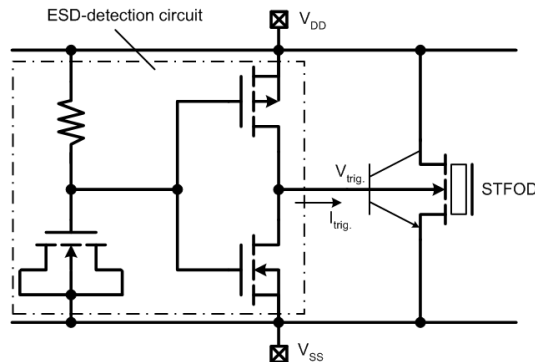


Fig. 5. Power-clamp circuit for ESD protection.

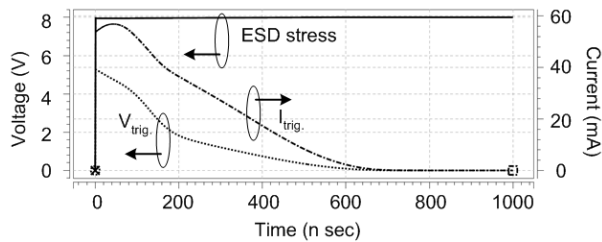


Fig. 6. Turn-on simulation of the power clamp.

V. EXPERIMENTAL RESULTS

Two LNA designs were fabricated in a standard 0.25- μm 1P5M CMOS process to verify the new proposed matching. One is LNA without ESD protection (LNA-1) and the other is LNA with ESD protection (LNA-2). Integrated

components of LNA-1 and LNA-2 are identical except the ESD protection circuit. The photographs of the fabricated chips of LNA without and with ESD protection are shown in Fig. 7. In ESD test, packaged chips were measured by Transmission Line Pulse (TLP) and zapped by an ESD simulator that includes HBM [6] and MM [7]. ESD test was completed on I/O pins with pin combinations, including positive-to- V_{SS} (PS-mode), positive-to- V_{DD} (PD-mode), negative-to- V_{SS} (NS-mode), and negative-to- V_{DD} (ND-mode) ESD stresses. The chips were also tested by V_{DD} -to- V_{SS} ESD stresses. According to the TLP-measured I-V characteristics in PS mode shown in Fig. 8, the ESD protection circuit apparently increases the maximum sustainable current (I_{t2}) over 3 A. Results of HBM and MM ESD robustness are listed in TABLE I and TABLE II, respectively. LNA-2 passes 4.5-kV HBM and 250-V MM levels, which satisfy ESD specifications for commercial ICs.

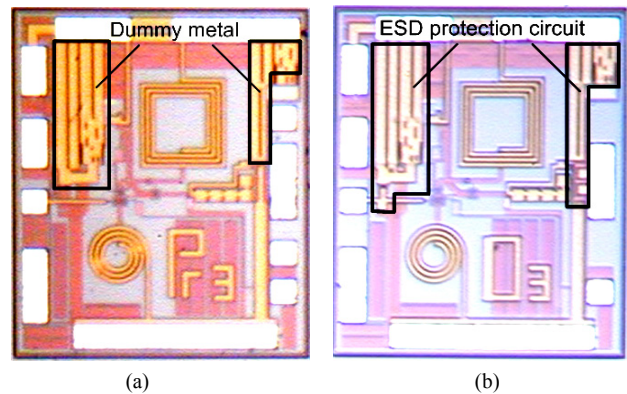


Fig. 7. Chip photographs of (a) LNA-1 without ESD protection and (b) LNA-2 with ESD protection.

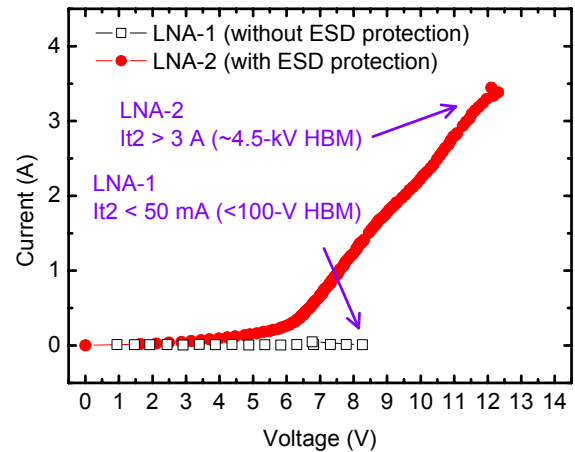


Fig. 8. TLP measured I-V characteristics of LNA-1 and LNA-2.

TABLE I
HBM ESD ROBUSTNESS OF LNA-1 AND LNA-2

	PS	PD	NS	ND	V_{DD} -to- $V_{SS}(+)$	V_{DD} -to- $V_{SS}(-)$
LNA-1		< 100 V			1.2 kV	2.0 kV
LNA-2	4.5 kV	4.7 kV	4.5 kV	4.5 kV		> 8.0 kV

TABLE II
MM ESD ROBUSTNESS OF LNA-1 AND LNA-2.

	PS	PD	NS	ND	$V_{DD-to-V_{SS}(+)}$	$V_{DD-to-V_{SS}(-)}$
LNA-1		< 50 V			100 V	150 V
LNA-2	300 V	300 V	250 V	250 V	450 V	750 V

In RF measurement, chips were bonded on board with bondwire connection. Both of LNA-1 and LNA-2 operate with 2.5-V power supply and consume 17.5-mW DC power. As shown in Fig. 9, LNA-1 and LNA-2 perform S11 below -11 dB and -14 dB in 2.4-GHz band, respectively. S11 denotes input matching condition and the value below -10 dB is adequate for general RF applications. S21 is introduced to estimate insertion gain of a two-port circuit. The S21 curves of LNA-1 and LNA-2 are compared in Fig. 10. The ESD protection circuit lowers the maximum S21 by 0.5 dB, from 11 dB at 2.52 GHz to 10.5 dB at 2.50 GHz.

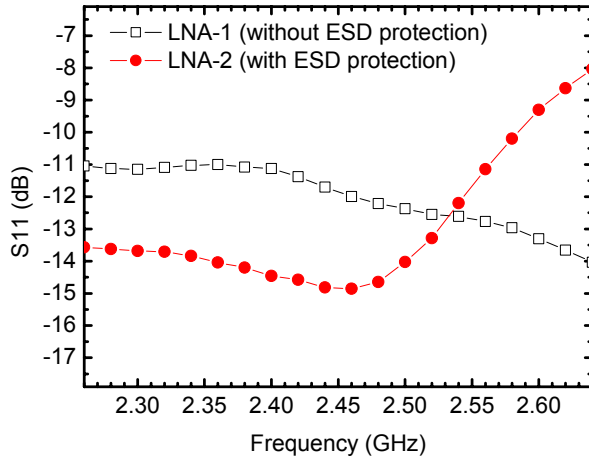


Fig. 9. Comparison on S11 between LNA-1 and LNA-2.

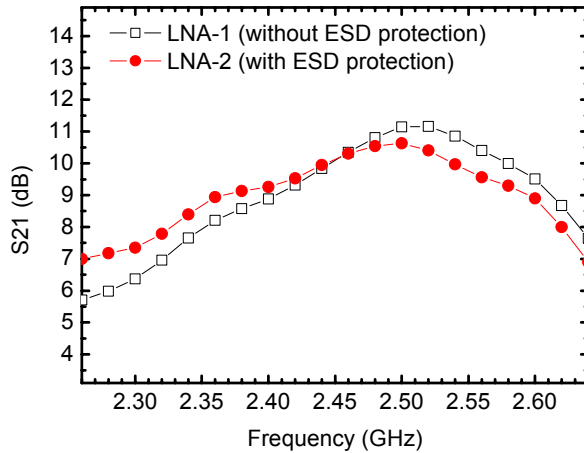


Fig. 10. Comparison on S21 between LNA-1 and LNA-2.

A comparison of noise figure is shown in Fig. 11. Input impedances of LNA-1 and LNA-2 samples were fine-tuned with off-chip inductors for optimized measurement on noise figures. So, the measured results around 5 dB are mainly dominated by the limitation of process characteristic. According to Fig. 11, the ESD protection circuit slightly degrades the noise figure by no more than 0.5 dB.

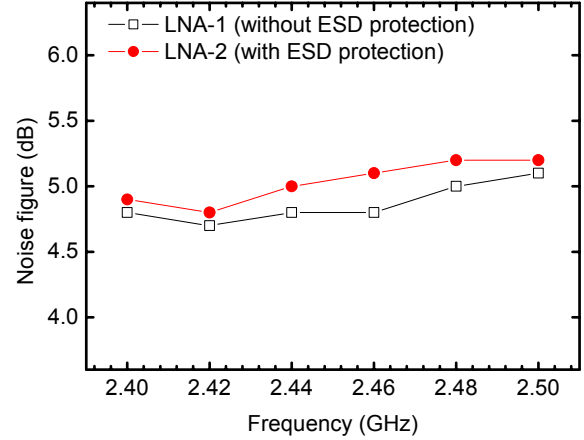


Fig. 11. Comparison on noise figure between LNA-1 and LNA-2.

VI. CONCLUSIONS

A new matching methodology of LNA with ESD protection was implemented and verified in a 2.4-GHz LNA. The matching methodology conceptually combines the parasitic capacitance into the input matching network of core LNA circuit without complicating the matching structure. The main advantages are avoiding significant RF-performance degradation, omitting extra circuit components, and saving chip area. The experimental results unveil an achievement that a multi-GHz LNA can perform high ESD immunity of 4.5-kV HBM and 250-V MM levels without significant RF degradation due to ESD protection devices. This new matching design leads to a simple and effective solution of LNA with ESD protection.

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