On-Chip ESD Protection Design for GHz RF Integrated Circuits by Using Polysilicon Diodes in sub-quarter-micron CMOS Process

Chyh-Yih Chang [1] and Ming-Dou Ker [2]

[1] Analog IP Section
System-on-Chip Technology Center
Industrial Technology Research Institute, Hsinchu, Taiwan

[2] Integrated Circuits & Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan

ABSTRACT

ESD protection in RF integrated circuits has several considerations: low parasitic capacitance, constant input capacitance, and insensitive to substrate coupling noise. In this paper, a new ESD protection design with polysilicon diodes for RF IC applications is proposed and characterized. The proposed polysilicon diode is constructed by polysilicon layer in a general CMOS process with a central un-doped region. The polysilicon diode with variation on the width of the central un-doped region is characterized at different temperatures. An on-chip ESD protection circuit realized with the stacked polysilicon diodes to reduce the total input capacitance for GHz RF application is demonstrated.

INTRODUCTION

ESD phenomena continue to be a reliability issue in CMOS IC's because of technology scaling and high frequency requirements. For RF IC's, the ESD protection has some limitations: low parasitic capacitance, constant input capacitance, insensitive to substrate coupling noise [1], and high ESD robustness. A typical request of an RF input pad with maximum loading capacitance is only 200 fF for circuit operation at 2 GHz [2]. This 200 fF target not only includes the ESD protection device but also the pad itself. In order to fulfill these requirements, diodes are commonly used for ESD protection in I/O circuits. Besides, to deal with these challenges, low capacitance bond pad and low capacitance ESD protection circuitry had been reported with some specific techniques [3]-[4]. By using the broken shape metal layers and additional diffusion layers, the bond pad capacitance has been successfully reduced 50% without extra process modification [3]. By adding a turn-on efficient ESD clamp circuit across the power rails of the input ESD protection circuit formed by the diodes, the input capacitance of the ESD protection circuit can be significantly reduced [4]. However, the ESD protection diodes are realized by the p-n junction on a common substrate of IC. The substrate noise generated from other circuits may couple into the RF input node through the ESD protection junction diodes. This often degrades RF circuit performance. Still now, there is no report addressing the substrate noise coupling issue of ESD protection circuit in RF circuits.

In this paper, a new diode structure constructed in polysilicon layer for ESD protection in RF applications is proposed. The polysilicon diode can be connected in series to further reduce the total parasitic capacitance seen from the input pad. Moreover, the polysilicon diode isolated from the substrate by field-oxide layer is free from the substrate noise coupling problem.

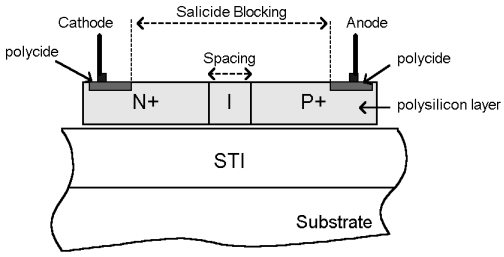

Fig.1 The device structure of the polysilicon diode realized in a sub-quarter-micron CMOS process.

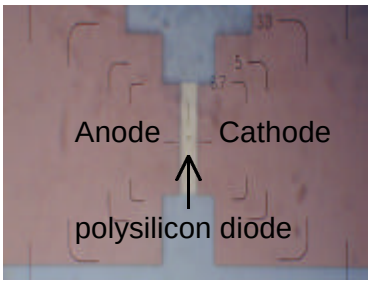

Fig.2 Photography of the fabricated polysilicon diode.

POLYSILICON DIODE STRUCTURE

The device structure of the proposed polysilicon diode is shown in Fig.1. Between the N-type high doping region, N+, and the P-type high doping region, P+, is a region indicated "I" without impurity doped. The region I is an un-doped region of the polysilicon layer fabricated in a salicide CMOS process. The doping concentrations of P+/N+ regions in the polysilicon diodes are the same as those of the NMOS/PMOS devices in the CMOS process. Therefore, the proposed polysilicon diode can be process-compatible to general CMOS process without extra process modification. In order to form the p/n junction of diode on polysilicon layer, the salicide blocking mask layer must be used on the polysilicon diode to prevent the polycide growing in a typical 0.25-μm CMOS process. To examine the polysilicon diode device, test chips had been fabricated in a standard salicide 0.25-μm CMOS process. The spacing between the N+ and P+ regions can affect the device characteristics and will be investigated in

the experimental test chips. The polysilicon diode constructed in polysilicon layer is located over the field oxide layer formed by the Shallow Trench Isolation (STI) process. The polysilicon diode has no junction in the substrate, therefore the substrate noise coupling issue can be eliminated. Fig.2 shows the photography of the polysilicon diode in a fabricated test chip.

DEVICE CHARACTERISTICS

A. DC Characteristics

To use polysilicon diode as an effective ESD protection device in the integrated circuits, the DC I-V characteristics must be investigated to prevent leakage issue. The measured current-voltage features with different spacing between N+ and P+ regions are shown in Fig.3. The polysilicon diode with a spacing of 0 μm has the direct connection of N+ and P+ regions without the non-doped central region. The polysilicon diode with a negative spacing has the overlap between the N+ and P+ regions in the test chip. In Fig.3, the polysilicon diode with a spacing of 0.5 μm has a forward-biased cut-in voltage of 0.64 volts and a reverse-biased breakdown voltage of -5.02 volt, which are both defined at the 1-μA current. When the spacing decreases from 0.5 μm to -0.5 μm, the forward-biased cut-in voltage and the reverse-biased breakdown voltage are both decreased. Therefore, for the IC' s with different power voltage levels, the layout spacing between N+/P+ regions of the polysilicon diodes can be adjusted to meet different applications.

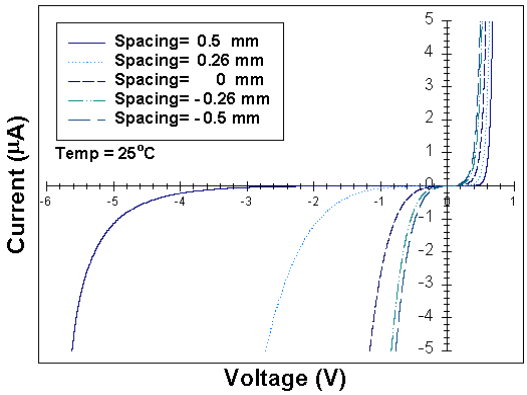

Fig.3 The DC characteristics of the polysilicon diodes with different N+/P+ layout spacing.

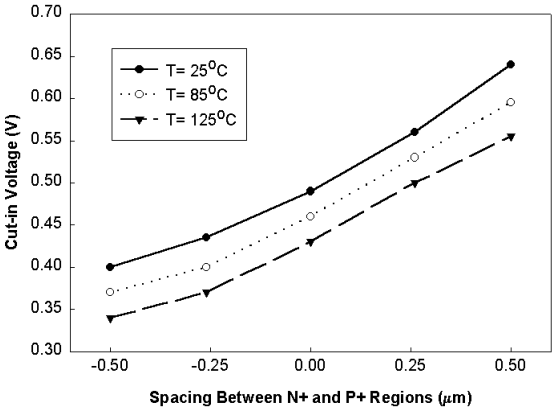

Fig.4 The cut-in voltage variation versus the spacing between N+ and P+ regions of the polysilicon diode under different temperatures. The cut-in voltage is defined as the forward voltage at 1-μA current.

B. Temperature Effect

Because the IC applications may cover a range of temperature, the temperature dependence on the proposed polysilicon diodes is also investigated in this work. The temperature dependence of the forward-biased cut-in voltage and the reverse-biased breakdown voltage on the fabricated polysilicon diodes are measured and shown in Fig.4 and Fig.5, respectively. In Fig.4, when the temperature increases from 25 °C to 125 °C, the cut-in voltages of polysilicon diodes are all reduced about 0.1 volts. In Fig.5, the reverse-biased breakdown voltage of the fabricated polysilicon diodes is not obviously reduced (only 1.9% at maximum), while the temperature increases from 25 °C to 125 °C. But the breakdown voltage of the polysilicon diode is obviously reduced by the decrease of the spacing between N+/P+ regions in the polysilicon diode structure. From the measured results, the polysilicon diode with specified layout spacing between N+/P+ regions has stable device characteristics for safe application in integrated circuits.

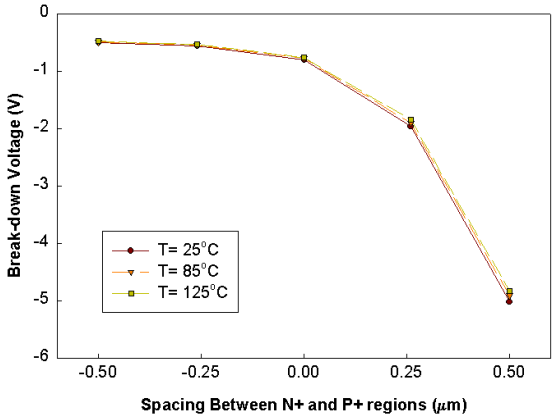

Fig.5 The breakdown voltage variation versus the spacing between N+ and P+ regions of the polysilicon diode under different temperatures. The breakdown voltage is defined as the reverse voltage at 1-μA current.

C. Second-Breakdown Current (It2)

The second-breakdown current (It2) of semiconductor device is often used for ESD benchmarking, and measured by Transmission Line Pulsing System (TLP System) with a pulse width of 100 ns [5]. In general, the HBM ESD level of semiconductor device related to its pulsed second breakdown current (It2) is expressed as [6]

$$V_{ESD} = (1500 + R_{device}) \times It2,$$

where R_{device} is the device resistance during the pulse stress. This R_{device} is usually much smaller than HBM ESD equivalent resistor of 1500 ohms. Therefore, the ESD level of

a semiconductor device almost equals to the product of 1500 ohms and its TLP-measured It2 value.

By measuring the It2 of device with the TLP system, the HBM ESD level can be predicted. The TLP-measured I-V characteristics of polysilicon diodes under forward-biased condition are shown in Fig.6. In forward-biased condition, the second breakdown current of polysilicon diode is about 9 mA/μm. The It2 of polysilicon diode under forward-biased condition only has a little variation when the spacing between

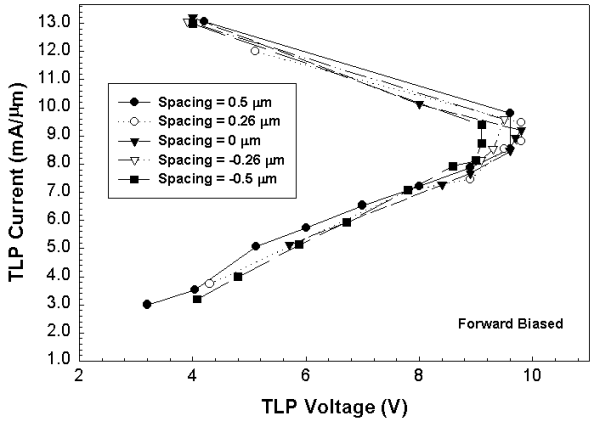

Fig.6 The TLP-measured I-V characteristics of the polysilicon diodes under the forward-biased condition.

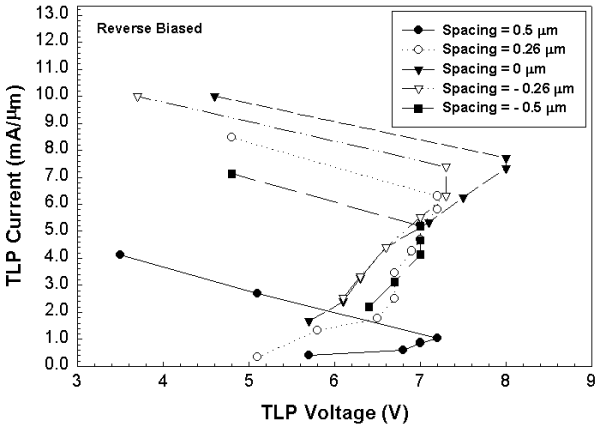

Fig.7 The TLP-measured I-V characteristics of the polysilicon diodes under reverse-biased condition.

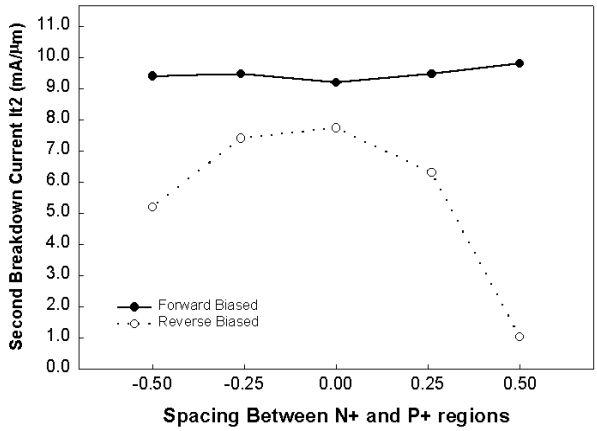

Fig.8 The second breakdown current variation of polysilicon diodes versus different spacing between N+ and P+ regions under both forward and reverse biased conditions.

N+/P+ regions varies from -0.5 to 0.5 μm. To sustain an HBM ESD stress of 2kV (It2=1.33A), the total junction perimeter of polysilicon diode must be drawn as 150 μm. The TLP-measured I-V characteristics of polysilicon diodes under reverse-biased condition are shown in Fig.7. The It2 of polysilicon diode under reverse-biased condition has obvious variation when the spacing between N+/P+ regions is changed. The relations between second-breakdown current and the spacing between N+/P+ regions of the fabricated polysilicon diodes in a 0.25-μm salicide STI CMOS process under forward- and reverse-biased conditions are summarized in Fig.8. The polysilicon diode operating in forward-biased condition has a much higher It2 than it operating in the reverse-biased condition. Typically, when the spacing between N+/P+ regions is 0.5 μm, the polysilicon diode has a It2 of 9.8 mA/μm under forward-biased condition, but it degrades to only 1.03 mA/μm under the reverse-biased condition. If the polysilicon diode in the on-chip ESD protection circuit can be arranged to operate in the forward-biased condition, it can sustain a high ESD level.

ESD Protection Design for RF IC's

The whole-chip ESD protection design for RF IC's is shown in Fig.9, where the polysilicon diodes are used as the input ESD clamp devices. When a pin-to-pin ESD zapping occurs on the RF IC, the polysilicon diodes cooperated with the turn-on efficient VDD-to-VSS ESD clamp circuit can provide a low-impedance path to discharge the ESD current. When the ESD zap is applied to the pad 1 with the pad 2 relatively grounded, the ESD current is conducted to the VDD power rail through the forward-biased polysilicon diode Dp1. The ESD current on VDD is discharged to the VSS power rail by the efficient VDD-to-VSS ESD clamp circuit [7]. Finally, the ESD current is conducted to grounded pad 2 through the forward-biased diode Dn2. The ESD current discharging path has been indicated by the bold line in Fig.9. With such a design, the polysilicon diodes operate in their forward-biased condition to discharge ESD current, therefore they can sustain a higher ESD level.

When the IC operates in normal condition with power supplies, all the ESD clamp diodes are operated in the reverse-biased condition. With a suitable layout spacing between the N+/P+ regions, the polysilicon diodes can kept off actually.

Because the polysilicon diodes are located above the STI field-oxide layer, it is far from the common IC substrate. The noise coupled from the substrate to the RF input pad can be significantly reduced if the input ESD clamp devices are realized by the proposed polysilicon diodes. The traditional p-n junction diodes can also provide the desired ESD protection function as that indicated in Fig.9. But, the traditional p-n junction diodes are very susceptible to substrate noise, because they are directly fabricated in the substrate. Such traditional p-n junction diodes are not suitable for ESD protection in the GHz RF circuits.

For GHz RF applications, the total input capacitance of an input pad including ESD clamp devices is limited to only 200fF [2]. To further reduce the capacitance generated from the polysilicon diodes is an important design task. For a given

ESD specification of the input pin, the polysilicon diodes should be drawn large enough to sustain the corresponding ESD current. The required device dimension of a polysilicon diode to sustain a specified ESD current can be calculated from its It2. If the polysilicon diode is drawn with a smaller dimension, it has a smaller capacitance but also a lower ESD level. It is very difficult to meet both of high ESD level and a low enough input capacitance. However, a new design solution is proposed in Fig.10 to further reduce the total input capacitance, as well as to sustain a high enough ESD level, for GHz RF input pin [8]. The polysilicon diodes have isolated junction regions from the common IC substrate, therefore they can be directly stacked to reduce the total input capacitance. In Fig.10(b), two stacked diodes are placed from the pad to VSS and VDD, therefore the total input capacitance can be

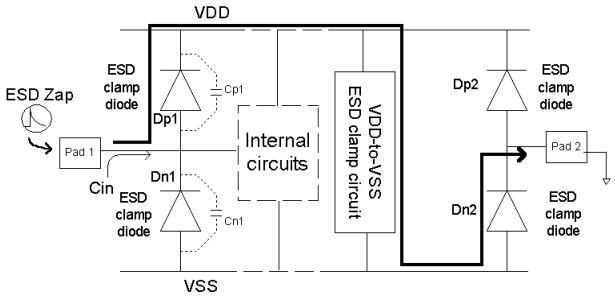

Fig.9 The ESD protection scheme for RF IC' s with the polysilicon diodes as input ESD clamp devices.

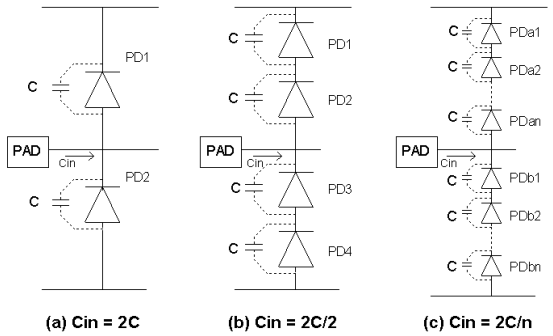

Fig.10 Polysilicon diodes connected in series to reduce the total input capacitance for a RF input pin.

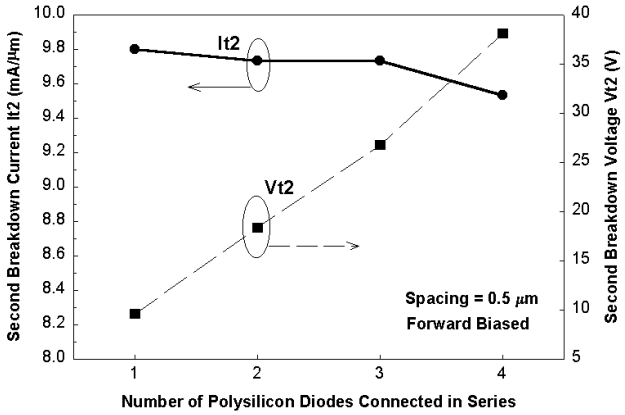

Fig.11 The TLP-measured second breakdown current and voltage of the polysilicon diodes with different numbers of polysilicon diodes connected in series.

reduced 50%. In Fig.10(c), there are n stacked diodes placed from the pad to VSS and VDD. The total input capacitance becomes only 2C/n, where C is the capacitance of a polysilicon diode. By using this design, both the ESD level and input capacitance can meet the requirements of GHz RF circuits.

To verify the ESD immunity of stacked polysilicon diodes under forward-biased condition, the TLP-measured It2 and Vt2 of the polysilicon diodes with N+/P+ spacing of 0.5 μm are shown in Fig.11. Increasing the number of polysilicon diodes connected in series only causes a very little degradation on the It2. But the second breakdown voltage increases apparently when the number of polysilicon diodes connected in series is increased. The reason is that increasing the number of stacked polysilicon diodes will increase the total resistance, therefore to increase the voltage drop across the diodes. However, the stacked diodes still have high enough It2 to sustain the desired ESD level. With a significantly reduced input capacitance but still to sustain a high ESD level, the proposed ESD protection design is very suitable for GHz RF circuits.

CONCLUSION

The polysilicon diode for ESD protection in RF IC applications is proposed and characterized. The polysilicon diode has neither substrate coupling noise nor substrate leakage current. This polysilicon diode has been experimentally investigated with layout parameters, temperature variation, and pulsed I-V characteristics in a 0.25-μm salicide STI CMOS process. The experimental results show that the polysilicon diode is good enough to be the ESD clamp device for on-chip ESD protection for RF applications. The polysilicon diodes can be further stacked to reduce the total input capacitance for GHz RF IC.

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