Methodology to Evaluate the Robustness of Integrated Circuits under Cable Discharge Event

Tai-Xiang Lai and Ming-Dou Ker

Abstract – **Cable Discharge Event (CDE) has been the main cause which damages the Ethernet interface. The transmission line pulsing (TLP) system has been the most important method to observe electric characteristics of the device under human-body-model (HBM) ESD stress. In this work, the long-pulse transmission line pulsing (LP-TLP) system is proposed to simulate the influence of CDE on the Ethernet integrated circuits, and the results are compared with conventional 100-ns TLP system. The experimental results have shown that the CDE robustness of NMOS device in a 0.25-μm CMOS technology is much worse than its HBM electrostatic discharge robustness.**

I. Introduction

Cable Discharge Event (CDE) is a critical reliability issue that requires recognition at all levels in the networking industry. The characteristics of twisted-pair cable in different environments play an important role in understanding CDE. Frequently changing cable environments also increase the challenge of preventing CDE event. With more understanding on CDE characteristics and discharge waveforms, the designers can achieve the best protection against CDE event through a good chip layout skill and a careful selection of protection components.

Electrostatic charges accumulate on a cable primarily through triboelectric (friction) effects or electromagnetic induction. For instance, the friction will result in accumulated charges as a cable is dragged across a floor or through the conduit. The positive tribo-charges on the outside surface of the cable attract negative charges in the twisted pair across the dielectric region, and then sweep the induced positive charges to the ends of the cable. Note that there is no net charge in the twisted-pair cable. Electromagnetic induction effects can be observed when cable accumulates charges from adjacent electromagnetic field. CDE is similar to the electrostatic discharge (ESD) event that happens when the cable filled with accumulated charges is plugged into electronic equipment or Ethernet interface. Such high-energy discharge of CDE event could damage the connectors, the electronic equipments, or the Ethernet interfaces. This phenomenon is illustrated in Fig. 1. Some international corporations and organizations have started to discuss such CDE issues [1]-[6]. Most CMOS IC products are routinely tested following the EIA/JEDEC Standard No.78 [7] to evaluate for latchup robustness. However, the CDE-induced latchup is a more severe condition [1]. Currently, there is no established component-level standard for CDE tests [3]. In this work, the long-pulse transmission line pulsing (LP-TLP) system is proposed as the efficient measurement setup to investigate the CDE reliability of IC products.

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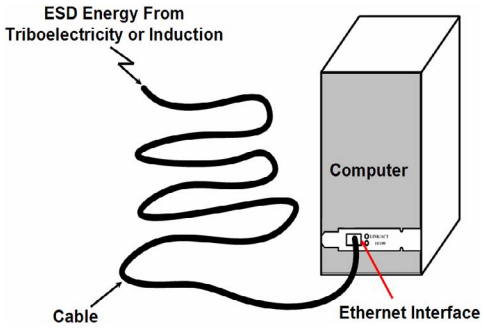

Fig. 1. The Ethernet interface is damaged from CDE.

II. Cable Discharge Test

Telecommunication Industry Association (TIA) has proposed the equipment to measure discharge waveforms of unshielded twisted pair (UTP) cables [5], [6]. A human-body-model (HBM) ESD gun, following the IEC 61000-4-2 Standard [8], was used to inject an 8kV contact-discharge pulse into a conductor pair of an assortment of category 5, category 5e, and category 6 UTP cables with a length of 56m. After the UTP cables are charged, their measured discharge waveforms have been mesaured in Fig. 2 [5]. The corresponding diagram of the mesurement setup is also depicted in the inset of Fig. 2. From the measured results, the discharge properties of these UTP cables are not obviously different because dielectric materials and capacitances associated with category 5, category 5e, and category 6 cables are almost the same. Moreover, the pulse width of all discharge currents of these UTP cables is approximately 475ns. This pulse width provides us a way to find the efficient component-level measurement method for investigating CDE robustness of I/O devices in IC products.

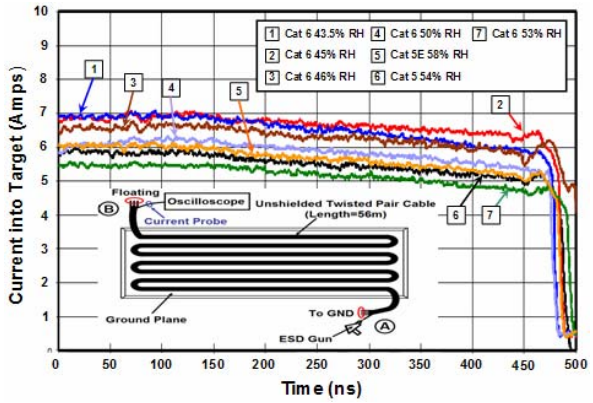

Fig. 2. Cable discharge waveforms for unused pairs connected together and grounded [5].

III. LP-TLP Measurement Setup

In 1985, T. J. Maloney and N. Khurana of Intel Corporation first proposed transmission line pulsing (TLP) system to measure the snapback I-V characteristics and the secondary breakdown current (It2) of CMOS devices [9]. The TLP system provides a single and continually-increasing voltage pulse to the device-under-test (DUT). The pulse width is as short as 100ns to simulate the HBM ESD stress. Because the relationship between the secondary breakdown current and HBM ESD level is linear, the TLP system has been widely used to observe the HBM ESD robustness of CMOS devices [10], [11].

By utilizing these characteristics of TLP system, long-pulse transmission line pulsing (LP-TLP) system is proposed in this work. The proposed LP-TLP system with a long pulse width of 500ns is evidently different from the traditional TLP system with a short pulse width of 100ns. Therefore, the LP-TLP system can be utilized to examine the damage situation on the DUT under CDE stress. Fig. 3 sketches the measurement setup for the proposed LP-TLP test. The measurement setup includes a diode, a load resistance (R_L), a 50-m transmission line, two switches (SW1 and SW2), a high-voltage DC supply, a current probe, a voltage probe, and an oscilloscope.

The diode and the load resistance (R_L) are defined as the polarization end to absorb the reflection wave. This principle of systematic operation is described as following. In the initial state, the switch SW1 is short-circuit and the switch SW2 is open-circuit. Through high-voltage resistance R_H, the high-voltage DC supply provides the long-pulse transmission line with a fixed voltage, such as 1V. The switch SW1 is open-circuit and the switch SW2 is short-circuit in the next state. The stored energy on the long-pulse transmission line transfers to the DUT by the electromagnetic wave, and then the current and voltage pulses on the DUT are measured by the oscilloscope to obtain the first group data of the LP-TLP measured I-V curve. Afterward, the switch SW1 returns to short-circuit and the switch SW2 reverts to open-circuit. Through the high-voltage resistance R_H, the high-voltage DC supply provides the long-pulse transmission line with a higher fixed voltage, such as 2V. The second group of current/voltage data is measured by repeating the aforementioned steps. The foregoing procedures are continuously duplicated until all I-V characteristics are measured. A permanent damage happens when the DUT is over-heated. With the aid of LP-TLP system, the characteristics of the secondary breakdown point of semiconductor devices under CDE stress can be measured.

A 50-Ω resistor is used as the DUT to verify that the LP-TLP system can generate a long current pulse similar to cable discharge waveform. The LP-TLP measured current waveforms are shown in Fig. 4. When the long-pulse transmission line is charged 450V, 640V, and 880V by the high-voltage DC supply, it will generate the corresponding LP-TLP currents of 6A, 9A, and 12A into the 50-Ω resistor at DUT, respectively. So, the amplitude of current pulse is obviously increased while the charged voltage provided by the high-voltage DC supply is increased. Furthermore, all of three current pulse widths are 500ns, so the proposed LP-TLP system with a long current pulse width has been proven.

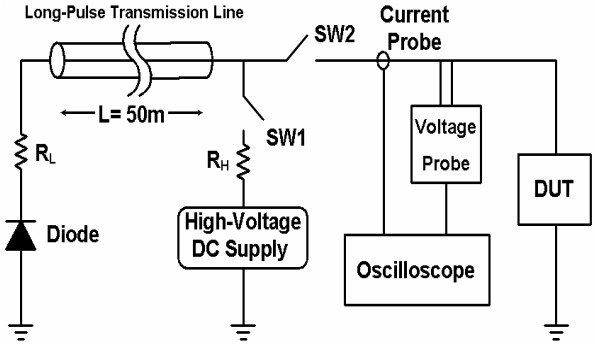

Fig. 3. The measurement setup for the proposed LP-TLP test.

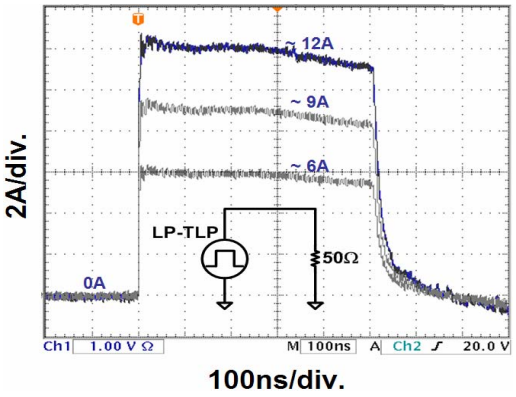

Fig. 4. The LP-TLP current waveforms on the 50-Ω resistor at DUT under different charged voltages.

The gate-grounded NMOS (GGNMOS) device (which has been widely used as the on-chip ESD protection device in CMOS ICs) is regarded as the DUT to demonstrate that LP-TLP system can accurately measure its snapback characteristics and its secondary breakdown current (It2). The LP-TLP measured I-V characteristics of GGNMOS with a device dimension of W/L= 240μm/0.3μm is shown in Fig. 5. The I-V curves of the GGNMOS device will shift from the initial point (A) to the trigger point (B) as the high-voltage DC supply

constantly provides the higher energy. After passing through the trigger point (B), the I-V curve will enter the snapback region because the parasitic lateral BJT is turned on. The point C and the point D are the initial point and middle point in snapback region, respectively. Afterward, the curve will reach the critical point (E) called the secondary breakdown point of GGNMOS device. Here, the It2 current is defined when the leakage current of DUT exceeds 1μA after the LP-TLP stress. If the high-voltage DC supply further raises the charged voltage, the I-V curve will reach the point F into the secondary breakdown region, which causes the permanent damage on the GGNMOS device. From the measured results, the LP-TLP system can efficiently measure the snapback characteristics of GGNMOS device under CDE-like stress. Fig. 5 shows that the trigger voltage is 5.9V, the holding voltage is 4.2V, and the It2 current is 2.3A. From the aforementioned tests, the LP-TLP system could be effectively used to observe the CDE robustness of the DUT.

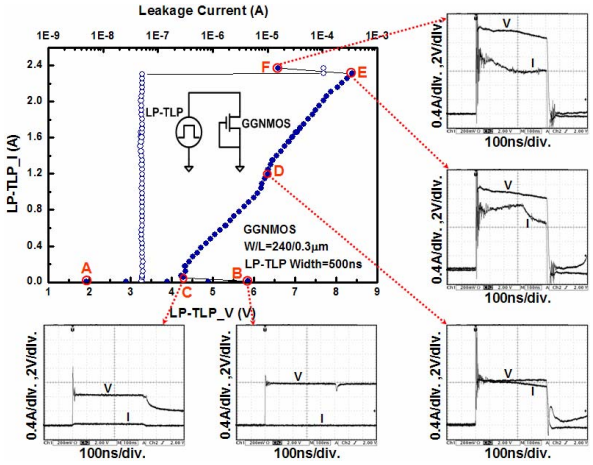

Fig. 5. The LP-TLP-measured I-V characteristic of the GGNMOS device.

IV. Experimental Result

The GGNMOS device fabricated in a 0.25-μm CMOS process is studied in this work. The LP-TLP system with a pulse width of 500ns is used to measure the snapback I-V curves of the GGNMOS device. Fig. 6 exhibits that the LP-TLP measured I-V characteristics and the corresponding leakage currents of the GGNMOS devices with different channel widths. From the measured results, all GGNMOS devices with different channel widths have distinct snapback characteristics. In addition, the It2 current of the GGNMOS device is linearly increased by increasing the channel width, but the turn-on resistance of GGNMOS device in snapback region is decreased by increasing the channel width. The It2 current of GGNOS devices with different widths of 240μm, 300μm, 360μm, and 600μm under proposed LP-TLP test are 2.3A, 2.9A, 3.3A, and 5.1A, respectively.

The It2 currents of the GGNMOS devices with different channel widths under traditional 100-ns TLP test and the proposed LP-TLP test are compared in Fig. 7. Both of these It2 currents are linearly increased while the channel width increases. Besides, the It2 current of the GGNMOS device under traditional 100-ns TLP test is much greater than that under the proposed LP-TLP test. Attributed to the longer LP-TLP pulse width, the stronger energy is injected into the DUT device, which causes a weak robustness of the device under CDE events.

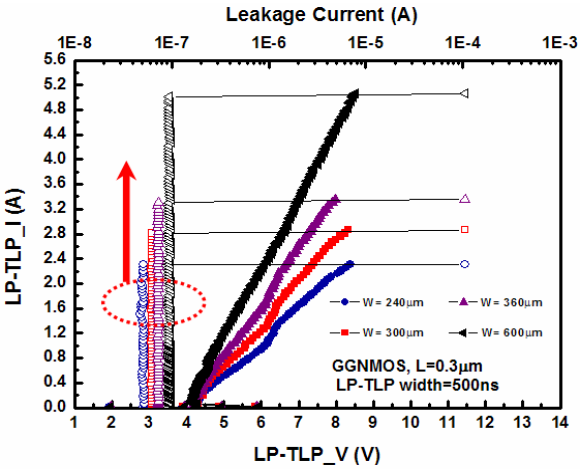

Fig. 6. The LP-TLP measured I-V characteristics and the leakage currents of the GGNMOS devices with different channel widths.

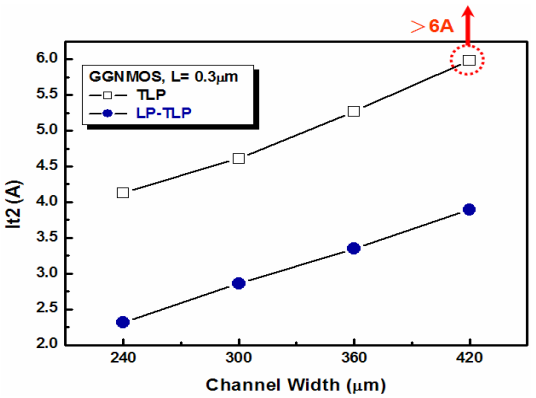

Fig. 7. The It2 currents of the GGNMOS devices with different channel widths under traditional 100-ns TLP test and the proposed LP-TLP test.

Fig. 8 shows the relationship between the It2 current of the GGNMOS devices with different channel lengths under traditional 100-ns TLP test and the proposed LP-TLP test. The It2 currents of the GGNMOS devices with different channel lengths under traditional 100-ns TLP test and the proposed LP-TLP test are quite different. If the GGNMOS device has a shorter enough channel length under TLP test, the efficiency and performance of its parasitic lateral BJT can be significantly improved [12]. Therefore, the GGNMOS device with a short channel length (0.25μm) can sustain much higher HBM ESD level than that with a medium channel length of ~0.5μm. On the contrary, the GGNMOS device with a shorter channel length under the proposed LP-TLP test has a lower It2 current, especially with a channel length of 0.25μm. Such different results will provide us to consider different

layout rules for Ethernet ICs against CDE events.

Figs. 9(a) and 9(b) reveal the scanning electron microscope (SEM) photographs of the GGNMOS device (W/L=360μm/0.3μm) to observe the failure locations under traditional 100-ns TLP test and the proposed LP-TLP test. As shown in Fig. 9(a), the failure locations are uniformly distributed among all fingers via traditional 100-ns TLP test. Fig. 9(b) shows an obvious local failure region because the GGNMOS device is directly burned out from drain to source in one finger under the proposed LP-TLP test. From the SEM pictures, the fingers in the GGNMOS device can not be uniformly turned on during the proposed LP-TLP test with higher pulse energy. This causes an evident reduction on the It2 of GGNMOS device under CDE events. By using the proposed LP-TLP test, one set of optimized design rules on chip layout in IC products can be estiablished in the given CMOS process to sustain CDE stress.

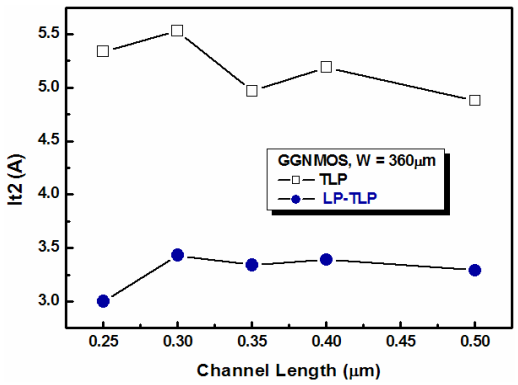

Fig. 8. The relationship between the It2 current of the GGNMOS devices with different channel lengths under traditional 100-ns TLP test and the proposed LP-TLP test.

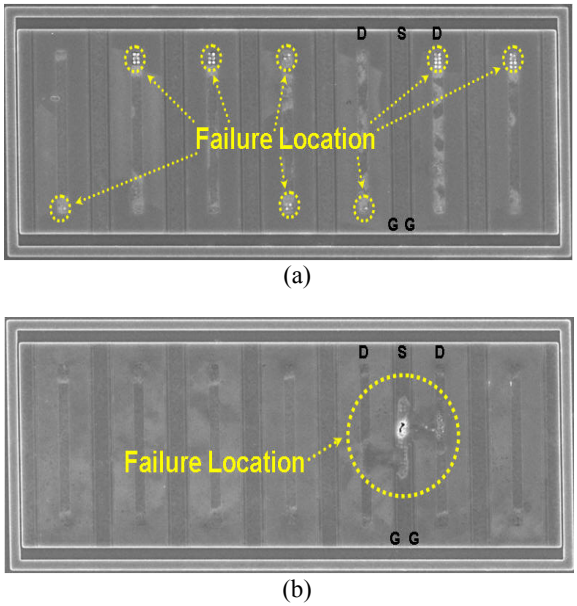

Fig. 9. SEM photographs on the GGNMOS device (W/L= 360μm/0.3μm) to observe its failure locations after (a) the traditional 100-ns TLP test and (b) the proposed LP-TLP test.

V. Conclusion

A new proposed LP-TLP system with a long pulse width of 500ns is utilized to investigate the phenomenon of CDE event on IC products. The snapback characteristics and the It2 current of devices in CMOS ICs can be measured through the proposed LP-TLP system. Moreover, the proposed LP-TLP system can be successfully observed the CDE robustness of the DUT. From the measured results, the It2 of GGNMOS under the proposed LP-TLP test is much lower than that under the traditional 100-ns TLP test. Hence, CDE event has been confirmed to cause a significant degradation on the relaibility level of ESD-protection IC products. An efficient protection design to overcome CDE events on IC prodcuts should be further studied.

References

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