ESD Protection Design for Mixed-Voltage I/O Interfaces -- Overview

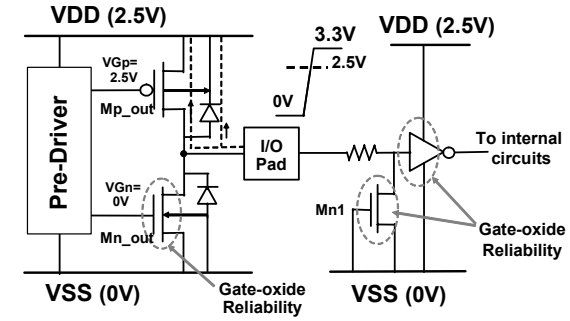
Ming-Dou Ker and Kun-Hsien Lin

Abstract – **Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces has been one of the key challenges of system-on-a-chip (SOC) implementation in nanoscale CMOS processes. This paper presents an overview on the design concept and circuit implementations of the ESD protection designs for mixed-voltage I/O interfaces without using the additional thick gate-oxide process. The ESD design constraints in mixed-voltage I/O interfaces, the classification and analysis of ESD protection designs for mixed-voltage I/O interfaces are presented and discussed.**

I. INTRODUCTION

With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mix semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the interfaces between semiconductor chips or sub-systems which have different internal power supply voltages. For example, a 3.3-V I/O interface is generally required by the ICs realized in CMOS processes with the normal internal power-supply voltage of 2.5V or 1.8V. The traditional CMOS I/O buffer with VDD of 2.5V is shown in Fig. 1(a) with both output and input stages. When an external 3.3-V signal is applied to the I/O pad, the channel of the output pMOS (Mp_out) and the parasitic drain-to-well junction diode in the Mp_out cause the leakage current paths from the I/O pad to VDD, as the dashed lines shown in Fig. 1(a). Moreover, the gate oxides of the output nMOS (Mn_out), the gate-grounded nMOS (Mn1) for input electrostatic discharge (ESD) protection, and the input inverter stage are over-stressed by the 3.3-V input signal to suffer the gate-oxide reliability issue. By using the additional thick gate-oxide process (or called as dual gate-oxide CMOS process), the gate-oxide reliability issue can be avoided. However, the process complexity and fabrication cost are increased.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-MOS configuration has been widely used in the mixed-voltage I/O circuits [1]-[3]. The typical 2.5V/3.3V-tolerant mixed-voltage I/O circuit is shown in Fig. 1(b) [1]. The independent control on the top and bottom gates of stacked-nMOS device allows the devices to meet reliability limitations during normal circuit operation. The gate of top nMOS (Mn_top) in the stacked-nMOS device is biased at VDD (e.g. 2.5V in a 2.5V/3.3V mixed-voltage I/O interface). The gate of bottom nMOS (Mn_bot) is biased at VSS by the pre-driver circuit to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g. 3.3V in a 2.5V/3.3V mixed-voltage I/O interface), the common node between the Mn_top and Mn_bot in the stacked-nMOS structure has approximately a voltage level of VDD-Vth (~ 1.9V), where Vth (~ 0.6V) is the threshold voltage of nMOS device. Therefore, the stacked-nMOS can be operated within the safe range for both dielectric and hot-carrier reliability limitations. The pull-up pMOS (Mp_mix), connected from the I/O pad to the VDD power line, has the



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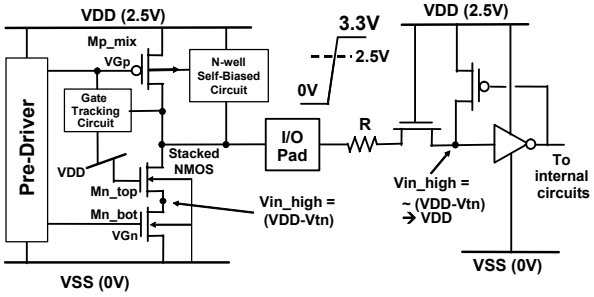

(b)

Fig. 1. Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-nMOS and the N-well self-biased pMOS.

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gate tracking circuits for tracking the gate voltage and the n-well self-biased circuits for tracking n-well voltage, which are designed to ensure that the Mp_mix does not conduct current when the 3.3-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

In this paper, an overview on the ESD protection designs for mixed-voltage I/O interface circuits without using the additional thick gate-oxide process is presented. The content covers the ESD design constraints in mixed-voltage I/O circuits, the classification and analysis of the proposed ESD protection designs for mixed-voltage I/O circuits.

II. ESD Design Constraints in Mixed-Voltage I/O Circuits

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode). The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit is shown in Fig. 2(a), where a PS-mode ESD pulse is applied to the I/O pad. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [4]. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits. Without the diode connected from the I/O pad to VDD in the mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. The ESD current path in the mixed-voltage I/O circuits with power-rail ESD clamp circuit under PS-mode ESD stress in illustrated in Fig. 2(b). Such ESD current at the I/O pad is mainly discharged through the stacked-nMOS by snapback breakdown. However, the nMOS in stacked configuration has a higher trigger voltage and a higher snapback holding voltage, but a lower secondary breakdown current (It2), as compared to that of the single nMOS [5], [6]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD level under PS-mode ESD stress, as compared to the traditional I/O circuits with a single nMOS [5]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses.

Although the ESD robustness of stacked-nMOS device can be somewhat improved by layout optimization, the stacked-nMOS device by snapback breakdown still cannot provide efficient ESD protection in the mixed-voltage I/O circuits. By using extra process modification such as ESD implantation, the ESD robustness of stacked-nMOS device can be further improved [7], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top nMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-nMOS device in the mixed-voltage I/O circuits [8]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.

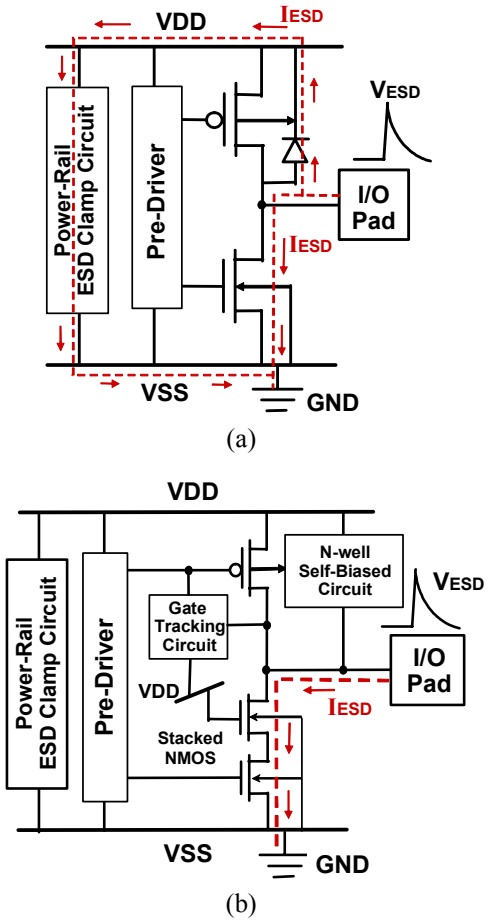


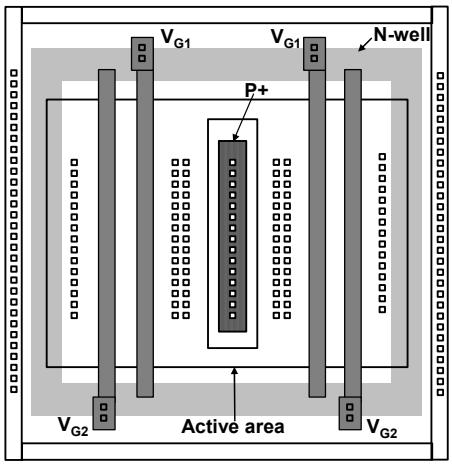
Fig. 2. The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the PS-mode ESD stress.

III. ESD Protection Designs for Mixed-Voltage I/O Circuits

A. Substrate-Triggered Stacked-nMOS Device

The snapback operation of the parasitic n-p-n BJT in the stacked-nMOS structure can be controlled by its substrate potential. The substrate-triggered technique [9] can be used to generate the substrate current in ESD protection circuits. With the substrate-triggered current, the trigger voltage of the stacked-nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

The finger-type layout pattern of the substrate-triggered stacked-nMOS device is shown in Fig. 3(a). As shown in the layout top view, an additional p+ diffusion is inserted into the center drain region of stacked-nMOS device as the substrate-triggered node. The trigger current is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance for improving turn-on efficiency of the parasitic lateral BJT in the stacked-nMOS device. The measured current-voltage (I-V) characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents are shown in Fig. 3(b). The trigger voltage of the parasitic n-p-n BJT in the stacked-nMOS device can be effectively decreased while the substrate-triggered current is increased. The substrate-triggered circuit should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough trigger current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked-nMOS device.



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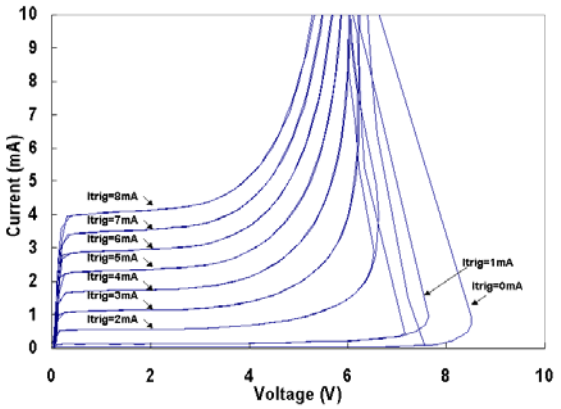
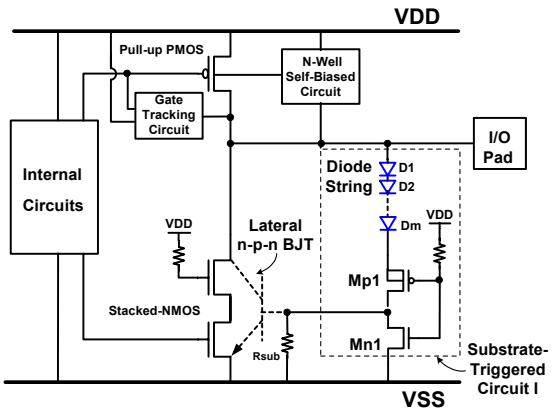


(b)

Fig. 3. (a) Finger-type layout pattern of the substrate-triggered stacked-nMOS device for mixed-voltage I/O circuits. (b) Measured I-V characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (Itrig).



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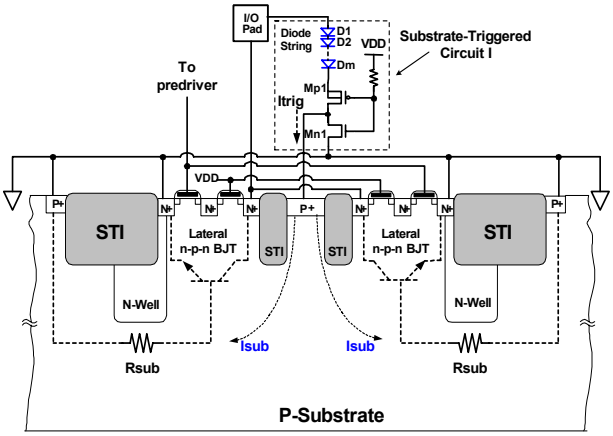


(b)

Fig. 4. (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit I for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit I.

The substrate-triggered circuit I for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 4(a) [10]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate-triggered circuit I is shown in Fig. 4(b). The substrate-triggered circuit I is composed of the diode string, a pMOS Mp1, and an nMOS Mn1, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. Under normal circuit operating condition, the turn-on voltage of the substrate-triggered circuit roughly equals to Vpad $\geqq V_{string}(I)$ +|Vtp|+VDD, where $V_{string}(I)$ is the total voltage drop across the diodes and Vtp is the threshold voltage of the pMOS. The turn-on voltage can be adjusted by varying the numbers of the diodes in the diode string. To satisfy the requirement in the 2.5V/3.3V mixed-voltage application, the number of the diodes in the diode string should be adjusted to make the turn-on voltage greater than 3.3V. When a 3.3-V input voltage is applied at I/O pad, Mp1 is kept off, and the local substrate of the stacked nMOS is biased at VSS by the turn-on of Mn1. With the diode string to block the 3.3-V input voltage at the I/O pad, the Mp1 with thin gate oxide has no gate-oxide reliability issue under normal circuit operating condition. The Mp1 in

conjunction with the diode string is used to reduce the leakage current through the substrate-triggered circuit in normal operating condition. The choice of a particular diode string is also determined by the specified pin leakage current at a given temperature. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Under PS-mode ESD stress condition, the gate of the Mp1 has an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the Mp1 into the p-substrate, when Vpad $\geqq V_{string}(I)$ + |Vtp|. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of Mp1. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be discharged from the I/O pad to VSS.

Another substrate-triggered circuit II for stacked-nMOS device in the mixed-voltage I/O circuits is shown in Fig. 5(a) [11]. The cross-sectional view of the substrate-triggered stacked-nMOS device with such a substrate-triggered circuit II is shown in Fig. 5(b). The substrate-triggered circuit II is composed of the pMOS Mp1, pMOS Mp2, nMOS Mn1, and nMOS Mn2, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-nMOS device during ESD stress. The gates of Mp1 and Mp2 are connected together to VDD through a resistor Rd. In the 2.5V/3.3V mixed-voltage IC application, the gates of Mp1 and Mp2 are biased at 2.5-V VDD supply under normal circuit operating condition. When the input voltage transfers from 0V to 3.3V at the I/O pad, the gate voltage of Mn1 could be increased through the coupling capacitor C. However, the Mn2 and Mp2 can clamp the gate voltage of Mn1 between VDD-Vtn and VDD+|Vtp|, where Vtn is the threshold voltage of nMOS. Once the gate voltage of Mn1 is over VDD+|Vtp|, the Mp2 will turn on to discharge the over-coupled voltage and to keep the gate voltage within VDD+|Vtp|. Since the upper boundary on the gate voltage of Mn1 is within VDD+|Vtp|, the source voltage of Mp1 is clamping below VDD, which keeps the Mp1 always off under normal circuit operation condition. The Mn2 and Mp2 can further clamp the gate voltage of Mn1 to avoid gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level. Under PS-mode ESD-stress condition, the gates of Mp1 and Mp2 have an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The positive ESD transient voltage on the I/O pad is coupled through the capacitor C to the gate of Mn1. In this situation, both of the Mn1 and Mp1 are operated in the turn-on state. Therefore, the substrate-triggered circuit II will conduct some ESD current flowing from I/O pad through Mn1 and Mp1 into the p-substrate. The trigger current provided by the substrate-triggered circuit II is determined by the size of Mn1, Mp1, and the capacitor C. Once the parasitic n-p-n BJT in the stacked-nMOS device is triggered on, the ESD current will be mainly discharged from the I/O pad to VSS.

Both two substrate-triggered designs can significantly reduce the trigger voltage and ensure effective ESD protection for the mixed-voltage I/O circuits. By using such substrate-triggered designs, the gates of stacked-nMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n-p-n BJT in the stacked-nMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

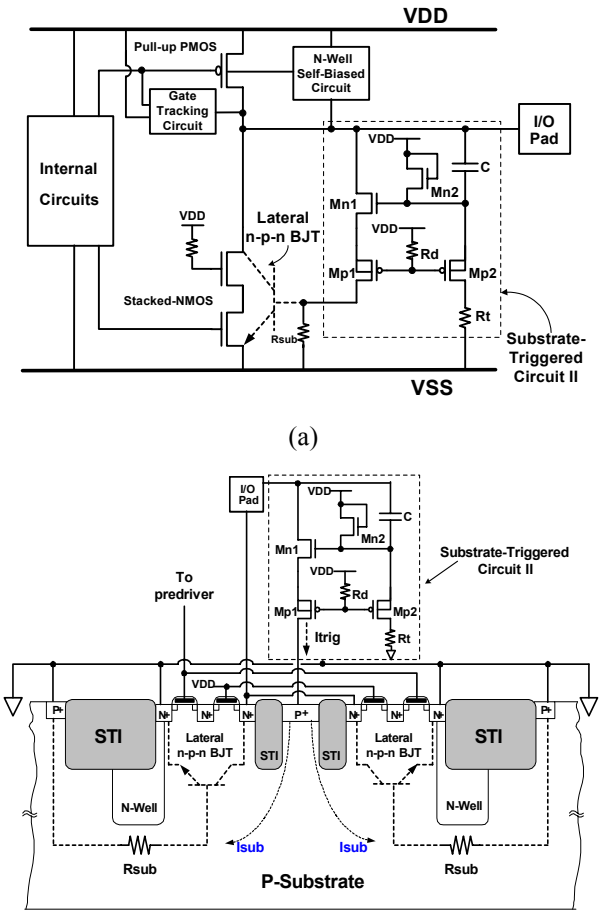
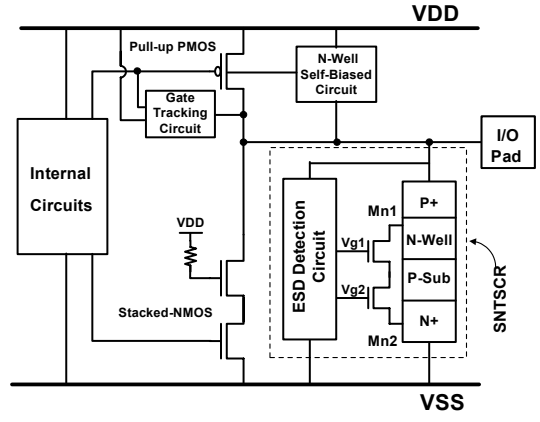


Fig. 5. (a) Schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit II for the mixed-voltage I/O circuits. (b) Cross-sectional view of the substrate-triggered stacked-nMOS device cooperating with substrate-triggered circuit II.

B. Extra ESD Device between I/O pad and VSS

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VSS power line. The ESD protection design, by using the additional stacked-nMOS triggered silicon controlled rectifier (SNTSCR), has been reported to protect the mixed-voltage I/O circuits [12]. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 6(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 6(b). The ESD detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD

detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the Mn3 in Fig. 6(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2 and Mn4. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the Mp1 is turned on but Mn3 is off since the initial voltage level on the floating VDD line is ~0V. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage of nMOS to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced, so the SNTSCR can be quickly triggered on to discharge ESD current. From the experimental results in a 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8kV, as compared with that (~2kV) of the original mixed-voltage I/O circuits with only stacked nMOS device.



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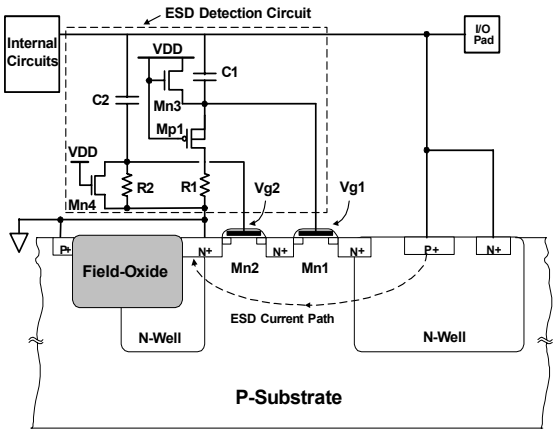

(b)

Fig. 6. (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

C. Extra ESD Device between I/O pad and VDD

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [13]. The ESD protection design with the diode string connected between the I/O pad and VDD power line for the mixed-voltage I/O circuits is shown in Fig. 7. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the VDD supply voltage. To reduce the turn-on resistance from I/O pad to VDD during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to VDD through the stacked diodes could trigger on the parasitic vertical p-n-p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p-n-p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 7, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [13].

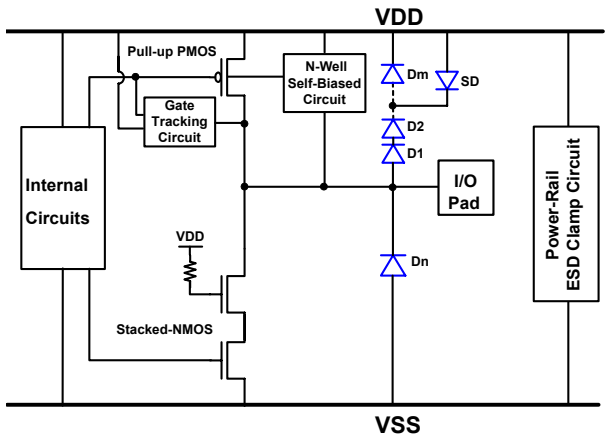

Fig. 7. ESD protection design with the diode string connected between the I/O pad and VDD power line to protect the mixed-voltage I/O circuits.

D. ESD Protection Design with ESD Bus

The whole-chip ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application has been reported in [15]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 8. The additional ESD bus line is realized by a wide metal line in CMOS IC [15], [16]. To save layout area, the ESD bus can be realized by the different metal layer, which overlaps the VDD power line. The ESD bus is not directly connected to an external power pin, but biased to VDD through the diode D1 in Fig. 8. The diode D1 connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The diode Dp is connected between I/O pad and ESD bus, whereas the diode Dn is connected between VSS power line and I/O pad. One (the

first) power-rail ESD clamp circuit is connected between VDD power line and VSS power line. Another (the second) power-rail ESD clamp circuit is connected between the ESD bus and VSS power line. The second power-rail ESD clamp circuit connected between ESD bus and VSS power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode Dp to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode Dp to the ESD bus, the second power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded VDD. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus.

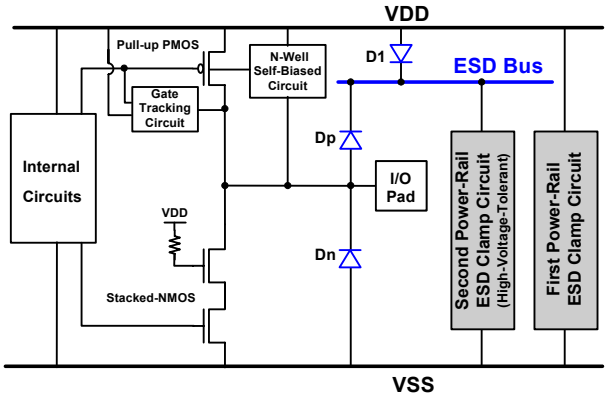

Fig. 8. The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits.

IV. Conclusion

This paper presents a comprehensive overview on the ESD protection designs for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. To design the efficient ESD protection circuit for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important challenge to SOC implementation in the nanoscale CMOS technology.

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