ESD Self-Protection Design on 2.4-GHz T/R Switch for RF Application in CMOS Process

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Abstract – **An RF transceiver front-end for 2.4GHz applications realized by a fully integrated T/R switch with ESD self-protection capability is presented in this work. Experimental results show that the proposed design without using any additional ESD protection device can provide enough ESD self-protection capability with good RF performances.**

Keywords – Electrostatic discharges (ESD), radio-frequency (RF), transceiver, transmit/receive (T/R) switch.

I. INTRODUCTION

In a radio-frequency (RF) transceiver, the front-end circuit between antenna and mixer includes the transmit/receive (T/R) switch, low-noise amplifier (LNA), and power amplifier (PA), as shown in Fig. 1. Process scaling enables SoC integration of the RF front-end circuit, and CMOS technologies have been widely used to implement the fully-integrated RF front-end circuits [1]-[3]. However, the MOS transistors are very sensitive to the overstress of electrostatic discharge (ESD) events. In order to sustain the required ESD robustness, on-chip ESD protection circuits must be added at the RF transceiver that may be stressed by ESD. Of course, adding ESD protection circuit causes RF performance degradation. The conventional dual-diode ESD protection scheme has been generally used for gigahertz RF circuits, since it can meet the typical specification on ESD robustness and RF performance [4]-[6]. In this work, a more efficient design with ESD self-protection capability to improve ESD robustness is proposed. With the ESD self-protection design on T/R switch, the ESD robustness of RF front-end circuit can be improved without using any additional ESD protection device.

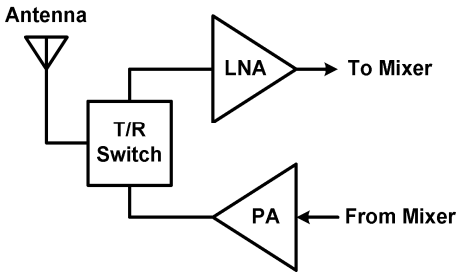


Fig. 1. RF transceiver front-end circuit.

II. DESIGN OF RF TRANSCEIVER FRONT-END CIRCUIT

In this work, the RF front-end circuit is designed to operate at 2.4GHz with V_{DD} supply of 1.8V. The circuit schematic of transceiver front-end with T/R switch, LNA, and PA is shown in Fig. 2. The series-shunt T/R switch with two identical arms is the most commonly used topology [7]. In this topology, the series and shunt MOS transistors dominate the insertion loss and isolation, which are the key figures of merit of T/R switch. Low insertion loss and high isolation can be achieved by using the larger MOS transistors. However, the larger MOS transistors with significant large parasitic capacitances will limit the bandwidth. Therefore, the dimension of each MOS transistor is designed according to the trade-off among insertion loss, isolation, and bandwidth.

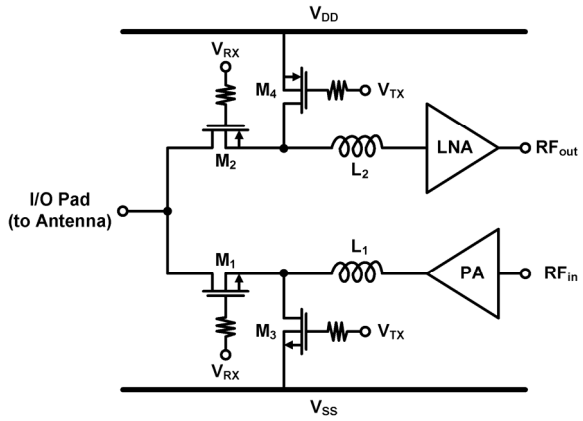


Fig. 2. Design of transceiver front-end circuit without ESD protection.

III. DESIGN OF ESD PROTECTION

Fig. 3 shows the conventional dual-diode ESD protection scheme with diodes at I/O pad and the power-rail ESD clamp circuit between V_{DD} and V_{SS}. Under positive I/O-to-V_{DD} (PD) or negative I/O-to-V_{SS} (NS) ESD stresses, ESD current is discharged through the forward-biased diode. During positive I/O-to-V_{SS} (PS) ESD stress, ESD current is discharged from the I/O pad through the forward-biased diode to V_{DD}, and discharged to the grounded V_{SS} through the power-rail ESD clamp circuit. Similarly, during negative I/O-to-V_{DD} (ND) ESD stress, ESD current is discharged from the V_{DD} through the power-rail ESD clamp circuit and the forward-biased diode to the I/O pad.

Fig. 4 shows the proposed ESD self-protection design on T/R switch. The parasitic diode exists in each MOS transistor. The parasitic diodes of M_1 and M_3 (D_{N1} and D_{N2}) provide ESD current path from V_{SS} to I/O, and the parasitic diodes of M_2 and M_4 (D_{P1} and D_{P2}) provide ESD current path from I/O to V_{DD}. In addition, the power-rail ESD clamp circuit provides ESD current path between V_{DD} and V_{SS} to achieve the whole-chip ESD protection. To further improve the ESD self-protection capability, the parasitic diodes can be enlarged by increasing the drain area of MOS transistors (M_1~M_4) in layout, as shown in Fig. 5.

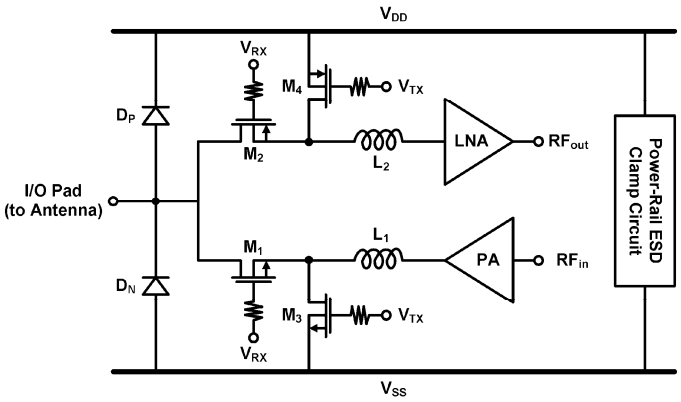


Fig. 3. Design of transceiver front-end circuit with traditional dual-diode ESD protection.

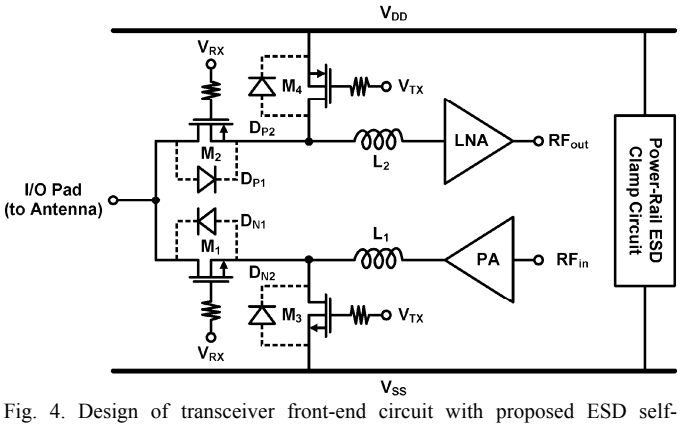
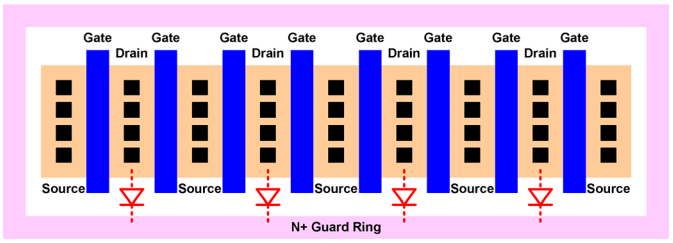
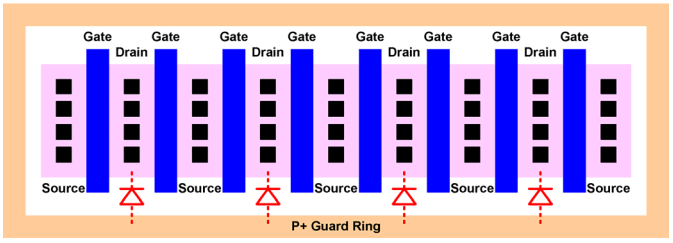


Fig. 4. Design of transceiver front-end circuit with proposed ESD self-protection.



(a)



(b)

Fig. 5. Layout top view of (a) RF PMOS and (b) RF NMOS with parasitic diodes.

IV. Simulation Results

The transceiver front-end circuits with T/R switch, LNA, and PA have been simulated in a 0.18µm CMOS process. Three test circuits include T/R switch without ESD protection, T/R switch with dual-diode ESD protection, and T/R switch with proposed ESD self-protection. The width/length (W/L) of M_1, M_2, M_3, and M_4 are 200µm/0.18µm, 400µm/0.18µm, 25µm/0.18µm, and 25µm/0.18µm, respectively. The active area of each parasitic and ESD diode is listed in Table I. The simulated forward transmission coefficients of three test circuits in Tx and Rx modes are shown in Figs. 6 and 7. The T/R switch with proposed ESD self-protection does not degrade the performances of RF transceiver front-end circuit.

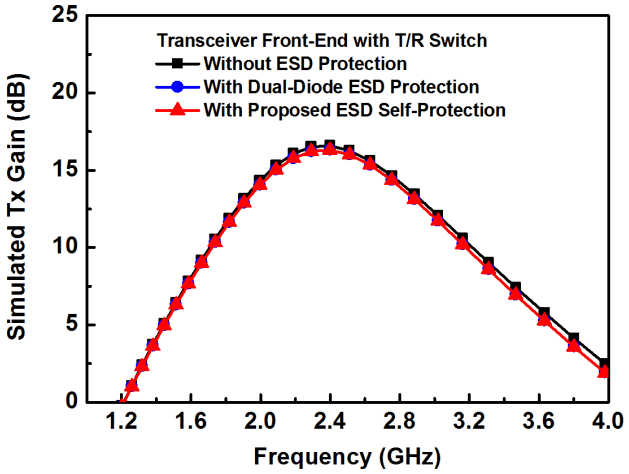


Fig. 6. Simulated forward transmission coefficients in Tx mode.

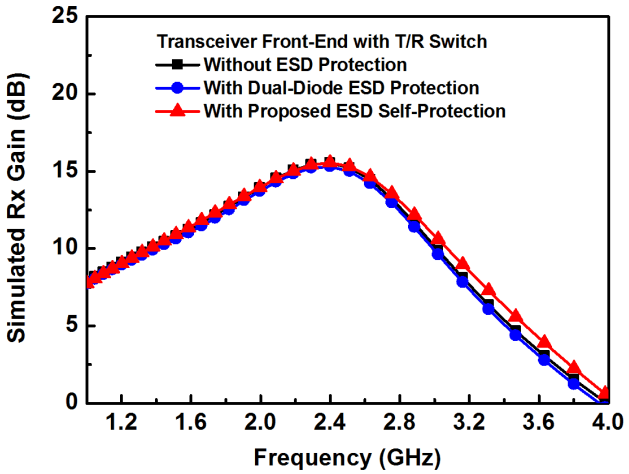


Fig. 7. Simulated forward transmission coefficients in Rx mode.

V. Experimental Results

Three test circuits of 2.4GHz RF transceiver front-end have been fabricated in the 0.18µm CMOS process. The area of each test circuit is 900x1335µm^2, including all pads. Fig. 8 shows the chip photo of transceiver front-end circuit with proposed ESD self-protection.

The RF characteristics among these three test circuits are measured on wafer through G-S-G-S-G microwave probes. The measured forward transmission coefficients are shown in Figs. 9 and 10. The peak gain in Tx mode (Tx gain) of all test circuits are about 15 dB, and the peak gain in Rx mode (Rx gain) of all test circuits are about 21 dB. The T/R switch with proposed ESD self-protection does not degrade its RF performances.

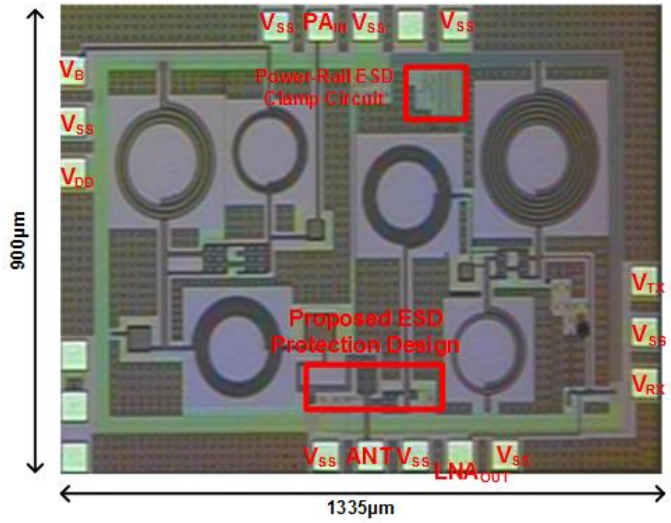


Fig. 8. Chip photo of transceiver front-end circuit with proposed ESD self-protection.

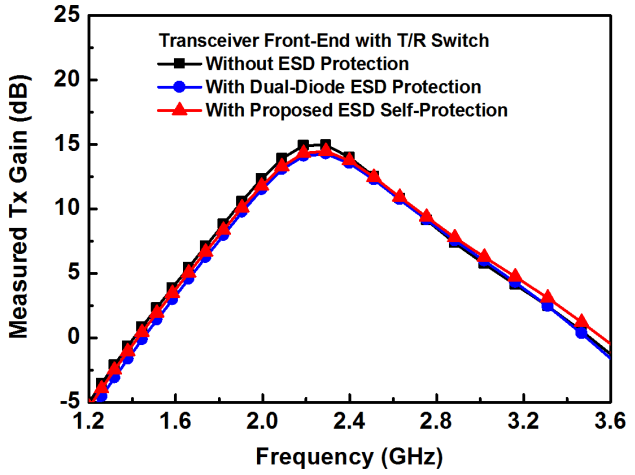


Fig. 9. Measured forward transmission coefficients in Tx mode among three fabricated transceiver front-end circuits.

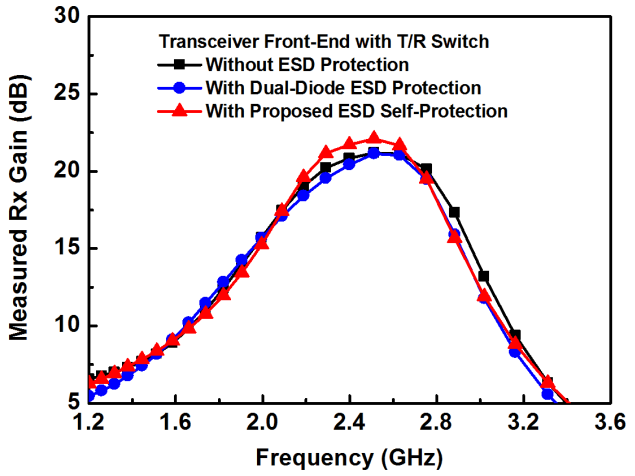


Fig. 10. Measured forward transmission coefficients in Rx mode among three fabricated transceiver front-end circuits.

To verify the ESD protection ability, the positive I/O-to-V_{DD} (PD), positive I/O-to-V_{SS} (PS), negative I/O-to-V_{DD} (ND), and negative I/O-to-V_{SS} (NS) modes of human-body-model (HBM) ESD stresses are performed onto the test circuits. The HBM ESD robustness can be obtained from the lowest levels among PD, PS, ND, and NS modes of ESD tests. The test circuit without ESD protection is severely degraded after 0.5kV HBM ESD test, while the test circuit with dual-diode ESD protection and the test circuit with proposed ESD self-protection can pass 1.5kV HBM ESD tests.

To investigate the turn-on behavior and the I-V characteristics of the test circuits in the time domain of HBM ESD event, the transmission-line-pulsing (TLP) system with 10ns rise time and 100ns pulse width is used. The secondary breakdown current (I_{t2}), which indicates the current-handling ability of each test circuit, can be extracted from the TLP-measured I-V curves. The TLP-measured I-V characteristics of test circuits under PS mode of stresses are shown in Fig. 11.

After HBM ESD test, the scanning electron microscope (SEM) was used to find the failure locations. Fig. 12 shows the SEM photo of T/R switch with proposed ESD self-protection after 2kV HBM ESD test. The failure location is located at M_3 in the T/R switch. The failure mechanism indicates that the ESD robustness can be further improved by increasing the drain area of M_3 in layout.

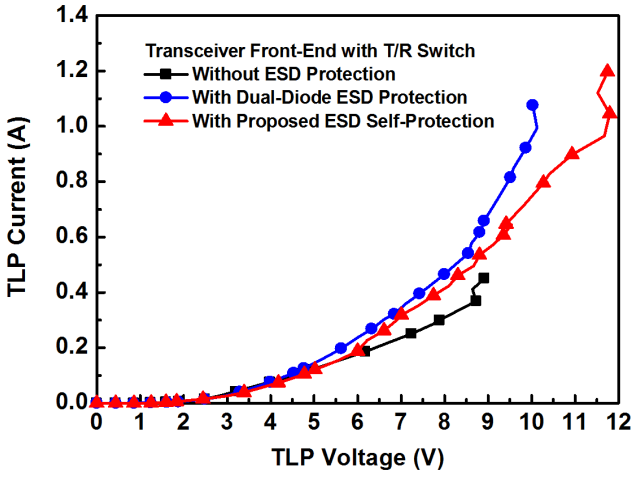


Fig. 11. TLP-measured I-V characteristics of test circuits under PS mode of stresses (positive stresses to I/O pad with grounded V_{SS}).

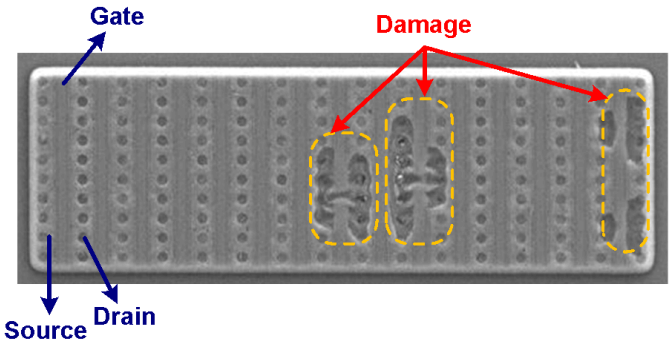


Fig. 12. SEM photo on M_3 in T/R switch with proposed ESD self-protection after 2kV HBM ESD test.

Table I. Test Circuits and Measurement Results

2.4GHz RF Transceiver Front-End	Active Area of Parasitic Diode ($M_1/M_2/M_3/M_4$)	Active Area of ESD Diode (D_P/D_N)	Measured Tx Peak Gain	Measured Rx Peak Gain	HBM ESD Level
T/R Switch without ESD Protection	92.8 / 168 / 11.6 / 11.6 μm^2	N/A	15.0 dB	21.2 dB	<0.5 kV
T/R Switch with Dual-Diode ESD Protection	92.8 / 168 / 11.6 / 11.6 μm^2	37.6 / 37.6 μm^2	14.3 dB	21.1 dB	1.5 kV
T/R Switch with Proposed ESD Self-Protection	92.8 / 168 / 32.6 / 32.6 μm^2	N/A	14.5 dB	22.1 dB	1.5 kV

VI. Conclusion

The new ESD self-protection design on T/R switch of fully integrated 2.4GHz transceiver front-end has been developed. The test circuits have been designed, realized, fabricated, and characterized in the 0.18μm CMOS process. The HBM ESD robustness of RF front-end circuit without ESD protection is only 0.5kV. Without using any additional ESD protection device, the HBM ESD robustness of RF front-end circuit with the ESD self-protection design on T/R switch can be improved to 1.5kV, as good as that with dual-diode ESD protection. Besides, the proposed ESD self-protection design does not degrade the performances of RF transceiver front-end circuit. Therefore, the proposed ESD self-protection design can be used to achieve good RF performance and high ESD robustness simultaneously.

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