Latchup-Like Failure of Power-Rail ESD Clamp Circuits in CMOS Integrated Circuits Under System-Level ESD Test

Ming-Dou Ker and Cheng-Cheng Yen
Nanoelectronics & Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

Abstract—**Two different on-chip power-rail electrostatic discharge (ESD) protection circuits, (1) with NMOS and PMOS feedback; and (2) with cascaded PMOS feedback, have been designed and fabricated in a 0.18-μm CMOS technology to investigate their susceptibility to system-level ESD test. The main purpose for adopting the feedback loop into the power-rail ESD clamp circuits is to avoid the false triggering during a fast power-up operation. However, during the system-level ESD test, where the ICs in a microelectronics system have been powered up, the feedback loop used in the power-rail ESD clamp circuit provides the lock function to keep the main ESD device in a "latch-on" state. The latch-on ESD device, which is often designed with a larger device dimension to sustain high ESD level, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD test. The susceptibility of power-rail ESD clamp circuits with the additional board-level noise filter to the system-level ESD test is also investigated. To meet high system-level ESD specifications, the chip-level ESD protection design should be considered with the transient noise during system-level ESD stress.**

Keywords- Electrostatic Discharge (ESD), system-level ESD test, power clamp circuits, board-level noise filter.

I. INTRODUCTION

Electrostatic discharge (ESD) protection has been one of the most important reliability issues in CMOS IC products. In order to obtain high ESD robustness, CMOS ICs must be designed with on-chip ESD protection circuits at the input/output (I/O) pins and across the power lines. With the reduced breakdown voltage of the thinner gate oxide in deep submicron CMOS processes, turn-on-efficient ESD protection circuit is required to clamp the overstress voltage across the gate oxide of internal circuits. Besides the input or output ESD protection circuits around the each input or output pads, the whole chip ESD protection must be designed with an effective power-rail ESD clamp circuit to protect CMOS ICs without suffering the unexpected ESD damage on internal circuits [1]. When the input (or output) pin is zapped under the positive-to-V_{SS} (PS-mode) or negative-to-V_{DD} (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between the V_{DD} and V_{SS} power lines to efficiently discharge ESD current. For a comprehensive component-level ESD verification, two additional pin combinations under ESD test, the pin-to-pin ESD stress and the V_{DD}-to-V_{SS} ESD stress [2], are performed to verify ESD reliability of the whole IC chip. To avoid the unexpected ESD damages located in the internal circuits after ESD stresses, the power-rail ESD clamp circuit must be designed with high turn-on efficiency and fast turn-on speed. Thus, the effective power-rail ESD clamp circuit is necessary in CMOS ICs for protecting the internal circuits against ESD damage. To enhance the triggering efficiency of the power-rail ESD clamp circuit, some advanced designs had been reported in [3]-[5].

Recently, system-level ESD reliability has attracted more attentions than before in microelectronics products. This tendency results from not only the process with more integrated functionality into a single chip, but also the strict requirement of reliability regulation, such as the system-level ESD test for electromagnetic compatibility (EMC) [6]. During the system-level ESD test, the microelectronics products must sustain the ESD stresses of ±8kV (±15kV) under the contact-discharge (air-discharge) test mode to meet the immunity requirement of "level 4". During such a high-energy ESD event, some of ESD-induced overshooting/ undershooting pulses may couple into the microelectronics products to cause damage or malfunction inside the CMOS ICs. Some CMOS ICs are very susceptible to system-level ESD stress, even though they have passed the component-level ESD specifications [2] of human-body-model (HBM) of ±2kV, machine-model (MM) of ±200V, and charged-device- model (CDM) of ±1kV.

In this work, the malfunction or wrong triggering behavior among two different on-chip power-rail ESD clamp circuits under system-level ESD test are investigated. The ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits will continually keep the ESD-clamping NMOS in the latch-on state after system-level ESD test. The latch-on ESD-clamping NMOS between V_{DD} and V_{SS} power lines in the already powered-up microelectronics system causes a serious latchup-like failure in CMOS ICs. The system-level ESD gun [7] is used to evaluate the susceptibility of two different power-rail ESD clamp circuits to the system-level ESD test.

II. POWER-RAIL ESD CLAMP CIRCUITS

To provide effective on-chip ESD protection, two different power-rail ESD clamp circuits with feedback techniques had been reported [4], [5], which are re-drawn in Figs. 1(a) and 1(b) with the names of (1) power-rail ESD clamp with NMOS+PMOS feedback, and (2) power-rail ESD clamp with cascaded PMOS feedback. These two power-rail ESD clamp circuits have been re-designed with their proposed design principles and fabricated stand alone in a 0.18-μm CMOS technology to investigate their susceptibility to system-level ESD test.

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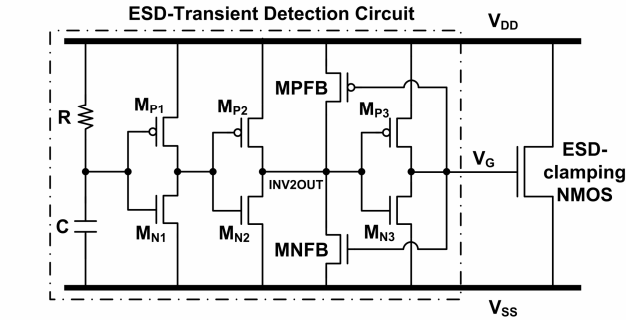

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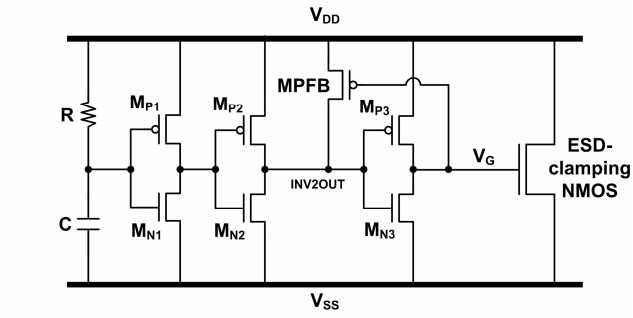


(b)

Figure 1. Two different power-rail ESD clamp circuits designed with (a) NMOS+PMOS feedback and (b) cascaded PMOS feedback.

A. Power-Rail ESD Clamp With NMOS+PMOS Feedback

The typical RC-based power-rail ESD clamp circuit is composed of a three-stage buffer between the RC circuit and the ESD-clamping NMOS [3]. The RC time constant is designed about 0.1~1μs to achieve the desired operations. However, in the advanced CMOS technology with thinner gate oxide, the power-rail ESD clamp circuit with a large MOS capacitance in the RC timer was reported to cause significant stand-by power loss due to gate oxide leakage [8]. Thus, the modified power-rail ESD clamp circuits with small capacitance are needed to combat the gate leakage. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can reduce the RC time constant [4], as illustrated in Fig. 1(a). The ESD-clamping NMOS is used to provide a low impedance path between the V_{DD} and V_{SS} to discharge ESD current. The ESD-transient detection circuit is designed to detect the ESD pulses and sends a control voltage to the gate of ESD-clamping NMOS. The transistors MPFB and MNFB provide a feedback loop, which can latch the ESD-clamping NMOS into a conductive state during ESD-stress condition. When a fast positive going ESD transient across the power rails, the MNFB can further pull the potential of INV2OUT node towards ground to latch the ESD-clamping NMOS in the conducting state until the voltage on V_{DD} drops below the threshold voltage of ESD-clamping NMOS. With this feedback loop in the power-rail ESD clamp circuit, the dynamic currents of M_{P2}, M_{N2}, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. Thus, the device ratios of M_{P2} and MNFB in the power-rail ESD clamp circuit should be suitably selected with consideration of the NMOS and PMOS feedback loop.

B. Power-Rail ESD Clamp With Cascaded PMOS Feedback

Another RC-based power-rail ESD clamp circuit with cascaded PMOS feedback has been proposed to reduce the RC time constant and to solve false trigger issue during fast power-up operation [5], as shown in Fig. 1(b). The PMOS transistor MPFB is connected to form the cascaded feedback loop. During the ESD-stress condition, the transistor MPFB was turned off and the voltage on the INV2OUT node can be remained in a low state. Thus, the turn-on time of the ESD-clamping NMOS can be longer than the time period set by the RC time constant. Another design consideration for power-rail ESD clamp circuit is the circuit immunity to false triggering during power-up condition. The power-rail ESD clamp circuit should be kept off when the IC is under normal power-on condition. If the power-rail ESD clamp circuit with cascaded PMOS feedback is mis-triggered by fast transient, the voltage on the INV2OUT node can be charged up toward V_{DD} by the subthreshold current of MPFB. Therefore, the ESD-clamping NMOS was avoided to stay at latch-on state after fast power-up operation. Compared with the NMOS+PMOS feedback design, the power-rail ESD clamp circuit with cascaded PMOS feedback is a dynamic feedback design and device ratio of transistors is not so critical.

III. SYSTEM-LEVEL ESD TEST

A. Measurement Setup

In the standard of IEC 61000-4-2 [6], two test modes have been specified: air-discharge test mode and contact-discharge test mode. Fig. 2 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode, which consists of a wooden table on the grounded reference plane (GRP). In addition, an isolation plane is used to separate the equipment under test (EUT) from horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470kΩ resistors in series. With such measurement setup, the susceptibility of different power-rail ESD clamp circuits under the system-level ESD stress can be evaluated. After every ESD zapping, the voltage level on V_{DD} node of IC is monitored to watch whether latchup-like failure occurs after the test.

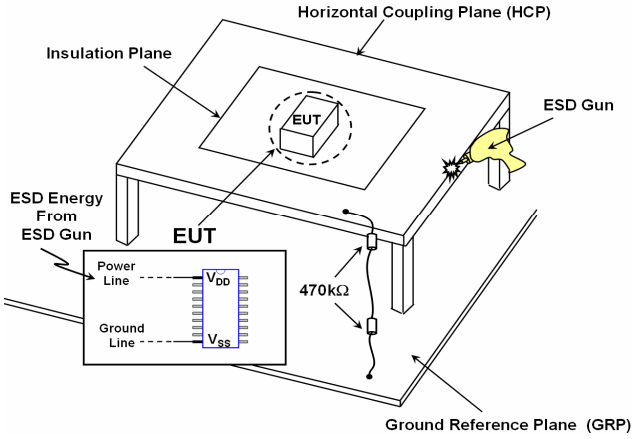
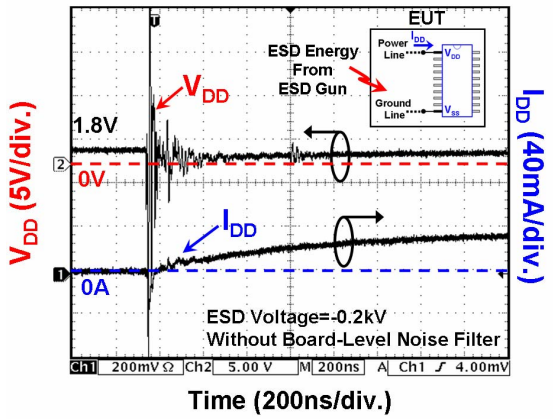


Figure 2. Measurement setup of the system-level ESD test with indirect contact-discharge test mode.

B. Measured Results

With the measurement setup of the system-level ESD test under indirect contact-discharge test mode shown in Fig. 2, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope to clearly indicate whether the latchup-like failure occurs (I_{DD} will significantly increase). Figs. 3(a) and 3(b) show the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback structure under the system-level ESD stress with ESD voltage of -0.2kV and +2.5kV, respectively. After the system-level ESD test with an ESD voltage of -0.2kV, latchup-like failure can be initiated in this power-rail ESD clamp circuit, because I_{DD} significantly increases and V_{DD} is pulled down as the waveforms shown in Fig. 3(a). After the system-level ESD test with an ESD voltage of +2.5kV, latchup-like failure has also been observed in Fig. 3(b). All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part. This implies that the feedback loop in the ESD-transient detection circuit is locking after system-level ESD test and to continually keep the ESD-clamping NMOS in its latch-on state. From the observed voltage and current waveforms, the large I_{DD} current is due to the latch-on state of ESD-clamping NMOS after system-level ESD test under indirect contact-discharge test mode.



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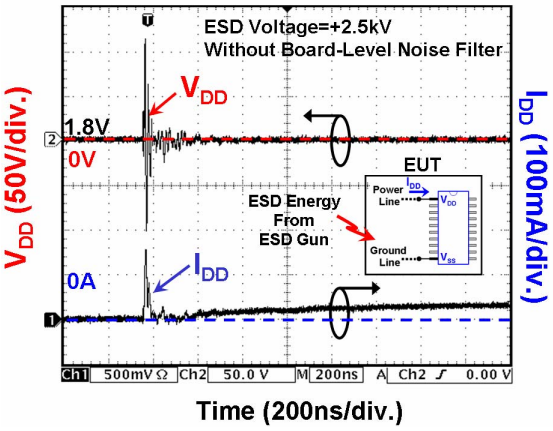


(b)

Figure 3. Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under system-level ESD test with ESD voltage of (a) -0.2kV and (b) +2.5kV.

For the power-rail ESD clamp circuit with cascaded PMOS feedback, the similar latchup-like failure has also been observed during the system-level ESD test with an ESD voltage of -1kV. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of ESD-clamping NMOS after system-level ESD test. The comparison on susceptibility between these two different power-rail ESD clamp circuits under system-level ESD test are listed in Table I.

TABLE I. COMPARISON ON THE SUSCEPTIBILITY BETWEEN TWO DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS UNDER SYSTEM-LEVEL ESD TEST.

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
With NMOS and PMOS Feedback	+2.5kV	-0.2kV
With cascaded PMOS Feedback	over +10kV	-1kV

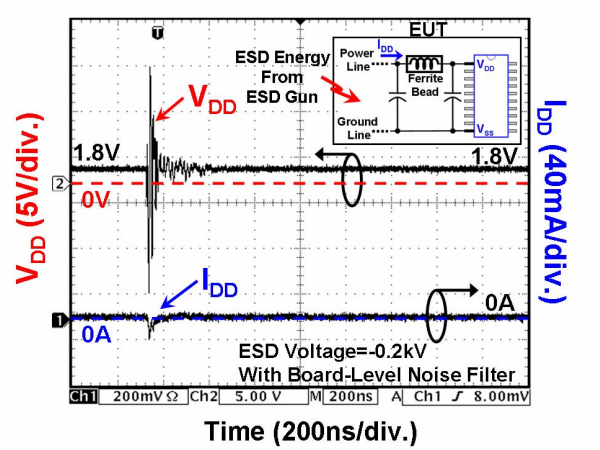
IV. EFFECTS OF BOARD-LEVEL NOISE FILTERS ON POWER-RAIL ESD CLAMP CIRCUITS

The board-level noise filters can enhance system-level ESD immunity of CMOS ICs by decoupling, bypassing, or absorbing ESD-induced noise voltage (energy) during the system-level ESD test [9]. To clarify how the board-level noise filter will affect the susceptibility of the power-rail ESD clamp circuit to the system-level ESD test, a 3rd-order π-section filter is used to investigate the dependency of board-level noise filters on V_{DD}/I_{DD} transient waveforms under system-level ESD test.

The 3rd-order π-section filter consists of a ferrite bead and two decoupling capacitors with equal capacitance. The ceramic disc capacitor has advantages of high rated working voltage (1kV), good thermal stability, and low loss at wide range of frequency. With the aid of the capacitor placed between the V_{DD} and V_{SS}, the noise voltage on power lines can be further reduced. With the equivalent circuit of an inductor and a small series resistor, the ferrite bead can protect CMOS ICs from RF field by absorbing RF energy while the ESD-induced transient current flows through it. Here, a resistor-type ferrite bead (part number: RH 3.5x9x0.8 with minimum impedance of 80Ω (120Ω) at 25MHz (100MHz) is employed.

To evaluate the influence of such a 3rd-order π-section filter, the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback are shown in Figs. 4(a) and 4(b), respectively, with ESD voltages of +2.5kV and -0.2kV zapping on the HCP during the system-level ESD test. When a 3rd-order π-section filter with the decoupling capacitance of 0.1μF is added between V_{DD} and V_{SS} of the power-rail ESD clamp circuit with NMOS+PMOS feedback, the measured V_{DD} and I_{DD} transient waveforms with ESD voltage of -0.2kV zapping on the HCP are shown in Fig. 4(a). Compared with the measured waveforms in Fig. 3(a) where there is no board-level filter network to suppress ESD-induced noise, the transient peak voltage waveform can be reduced to that shown in Fig. 4(a). As a result, latchup-like failure does not occur, and I_{DD} does not increase after the ESD-induced disturbance on V_{DD}. When an 3rd-order π-section filter is added between V_{DD} and V_{SS} of the power-rail ESD clamp circuit with NMOS+PMOS

feedback, the measured V_{DD} and I_{DD} transient waveforms with the ESD voltage of +2.5kV zapping on the HCP are shown in Fig. 4(b). Compared with the measured waveforms in Fig. 3(b), the transient peak voltage of the V_{DD} waveform is greatly reduced. As a result, the board-level 3rd-order π-section noise filter can further enhance the susceptibility of the power-rail ESD clamp circuit with NMOS+PMOS feedback against system-level ESD test.



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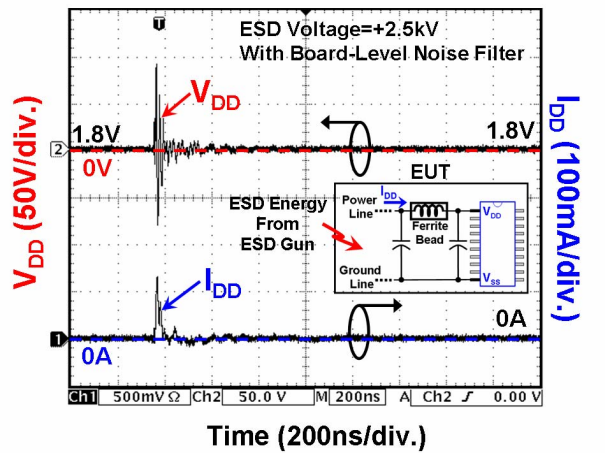

(b)

Figure 4. Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback combined with 3rd-order noise filter under system-level ESD test with ESD voltage of (a) -0.2kV and (b) +2.5kV.

The 3rd-order π-section filters with decoupling capacitances widely ranging from 100pF to 0.1μF are used to investigate their improvements on the susceptibility of the power-rail ESD clamp circuit with NMOS+PMOS feedback to system-level ESD stress. Due to a higher insertion loss, such a π-section filter has greater noise-bypassing ability as compared with the noise filters by only using capacitors or ferrite beads. For the power-rail ESD clamp circuit with NMOS+PMOS feedback combined with a 3rd-order π-section filter, the minimum system-level ESD voltage to cause latch-like failure can be greatly increased. For example, the minimum positive system-level ESD voltage to cause latch-like failure can be significantly increased from +2.5kV (without noise filter) up to +6kV (with 3rd-order π-section filter, decoupling capacitance of 0.1μF), as shown in Fig. 5.

Similarly, the minimum negative system-level ESD voltage to cause latch-like failure can be also significantly increased from -0.2kV (without noise filter) up to -5.5kV (with 3rd-order π-section filter, decoupling capacitance of 0.1μF).

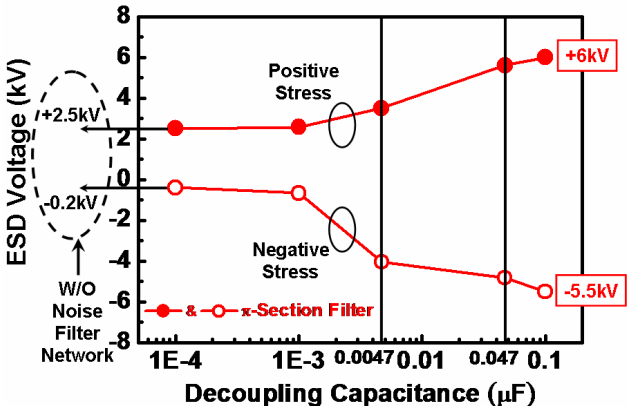

Figure 5. Relations between the decoupling capacitance and the minimum ESD voltage to cause latchup-like failure of the power-rail ESD clamp circuit with NMOS+PMOS feedback during system-level ESD test.

V. Conclusion

The on-chip power-rail ESD clamp circuits designed with feedback loop in their ESD-transient detection circuits have been found to suffer the latchup-like failure after the system-level test. The latch-on state of the ESD-clamping NMOS is kept by the feedback loop in the ESD-transient detection circuit during and after system-level ESD stress. To further improve the system-level ESD immunity of electronic products, chip-level solutions should be co-designed with board-level solutions to meet high system-level ESD specification.

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