# ESD Protection Design for Mixed-Voltage I/O Circuit with Substrate-Triggered Technique in Sub-Quarter-Micron CMOS Process

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## Abstract

*A substrate-triggered technique is proposed to improve ESD protection efficiency of the stacked-NMOS device in the mixed-voltage I/O circuit. The substrate-triggered technique can further lower the trigger voltage of the stacked-NMOS device to ensure effective ESD protection for the mixed-voltage I/O circuit. The proposed ESD protection circuit with the substrate-triggered technique for 2.5V/3.3V tolerant mixed-voltage I/O circuit has been fabricated and verified in a 0.25-µm salicided CMOS process. Experimental results have confirmed that the HBM ESD robustness of the mixed-voltage I/O circuit can be increased ~ 65% by this substrate-triggered design.*

## 1. Introduction

In the mixed-voltage IC with single power supply, only a low VDD power supply is provided for internal circuits. Therefore, the I/O circuits are designed to be tolerant of, and protected from, high-voltage input signals. Typically, a chip, which operates with I/O signals ranging from 0V to 3.3V, may have an internal supply voltage of only 2.5V or 1.8V. The chip-to-chip interface I/O circuits must be designed to avoid electrical overstress on the gate oxide and to prevent undesirable current leakage paths between the chips [1]-[5]. The ESD protection circuit also has to meet these constraints for providing robust ESD protection in such mixed-voltage application. In advanced deep submicron CMOS technology, some fabrication processes provide both high-voltage and low-voltage transistors. In such processes the high-voltage transistors, which have thicker gate oxides, can be used for the protection circuits. However, some processes with only single gate-oxide thickness do not have this capability. Thus, there is a need for an ESD protection circuit designed by using the thin-oxide MOS devices, which have the same oxide thickness as those used in the interior of chip.

To solve the gate-oxide reliability issue without using the addition thick gate-oxide process (or called as dual gate oxide in some CMOS process), the stacked-NMOS structure had been widely used in the mixed-voltage I/O buffer [5]-[6], or even used in the power-rail ESD clamp circuits [7]. The typical 3V/5V-tolerant mixed-voltage I/O circuit is shown in Fig. 1 [5]. The pull-up PMOS, connected from the I/O pad to VDD power line, has the gate tracking circuits for tracking the gate voltage and N-well self-biased circuits for tracking N-well voltage to ensure that pull-up PMOS does not conduct current when the 5-V input signals enter the I/O pad. Due to the limitation of placing a diode from the pad to VDD, such mixed-voltage I/O circuits with stacked-NMOS often have much lower ESD level, as compared to the buffer with single NMOS [8]-[9].

In this paper, a substrate-triggered technique is proposed to reduce the trigger voltage of the lateral n-p-n BJT in the stacked NMOS device, and to enhance the ESD robustness of the mixed-voltage I/O circuits. An NMOS device with higher local substrate potential had been confirmed to provide better ESD robustness [10]-[12]. The substrate-triggered technique, realized by special circuit design, is therefore applied to improve ESD robustness of the stacked NMOS in the mixed-voltage I/O circuits.

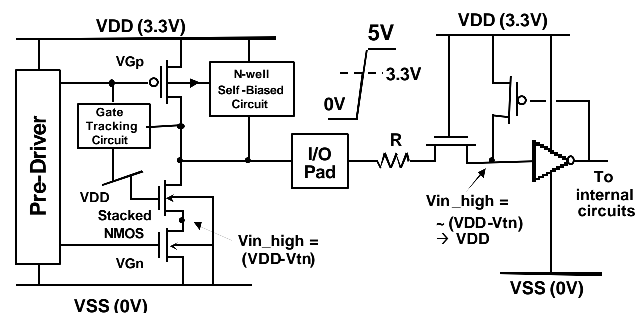


Fig. 1 The typical mixed-voltage I/O circuit with the stacked-NMOS and the self-biased-well PMOS to avoid the leakage current path and the gate oxide reliability issue.

## 2. Substrate-Triggered Stacked NMOS

### *2.1 Stacked-NMOS Device*

Fig. 2 shows the finger-type layout pattern and the corresponding cross-sectional view of the stacked-NMOS structure for mixed-voltage I/O circuit, which includes one

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pair of NMOS transistors connected in a stack configuration. The stacked-NMOS device is used as both of the pull-down stage and the ESD protection device for the I/O circuit. This NMOS transistor pair includes a first transistor (top NMOS transistor), having a drain connected to an I/O pad, and a gate (Vg1) connected to the VDD power supply. A second NMOS transistor (bottom NMOS transistor) of the NMOS transistor pair is merged into the same active area of the first transistor, having a gate (Vg2) connected to the pre-driver of mixed-voltage I/O circuit. The drain of the bottom NMOS and the source of the top NMOS are constructed together by sharing the common N+ diffusion region.

The voltage (Vg1) of the top NMOS is biased at the low VDD voltage (e.g. 2.5V in a 2.5V/3.3V process). The voltage (Vg2) of the bottom NMOS is at VSS provided by the pre-driver to avoid leakage current through the stacked-NMOS structure, when the I/O circuit has an high-voltage input signal. With a high-voltage input signal at the pad (e.g. 3.3V in a 2.5V/3.3V process), the shared common diffusion region has approximately a voltage level of VDD-Vth (~2.7V). The Vth (= 0.6V) is the threshold voltage of NMOS device. Therefore, the stacked-NMOS can be operated within the safe range for both dielectric and hot carrier reliability limitations.

Under the positive-to-VSS ESD-stress condition (with VSS grounded but VDD floating), the stacked-NMOS operates in snapback breakdown, with the bipolar effect taking place between the drain of the top NMOS and the source of the bottom NMOS. Fig. 3 shows a device cross sectional view of a stacked-NMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition. These two diffusions act as bipolar emitter and collector, respectively. Their spacing determines the base width and turn-on efficiency of the lateral bipolar transistor.

The snapback mechanism of stacked-NMOS for conducting large amount of ESD current involves both avalanche breakdown and turn-on of the parasitic lateral npn bipolar transistor. The hole current (Isub) generated from drain avalanche breakdown, drifting through the effective substrate resistance (Rsub) to ground, may elevate the substrate potential local to the emitter-base junction of npn shown in Fig. 3. The voltage level, which the local substrate potential is elevated, depends on the relative proximity to the avalanching junction. When the emitter-base junction of npn begins to weakly forward bias due to the increase of local substrate potential, additional electron current through the bipolar device acts as "seed current" to drive a significant increase in the multiplication rate and avalanche current generation at the collector-base junction of the lateral npn BJT. Therefore, a "snapback" is seen, and the lateral npn BJT enters strong bipolar conduction.

### *2.2 Substrate-Triggered Stacked-NMOS Device*

As shown in Fig. 3, the snapback operation of stacked-NMOS device depends on the substrate current (Isub), which is created at the reversed-biased drain/p-substrate junction, to forward bias the substrate/source junction. Hence, the substrate resistance (Rsub) and substrate current (Isub) are the important design parameters for ESD protection [13]-[14]. The substrate-triggered technique can be used to generate the substrate current. With the substrate-triggered current, the trigger voltage (Vt1) of the stacked-NMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

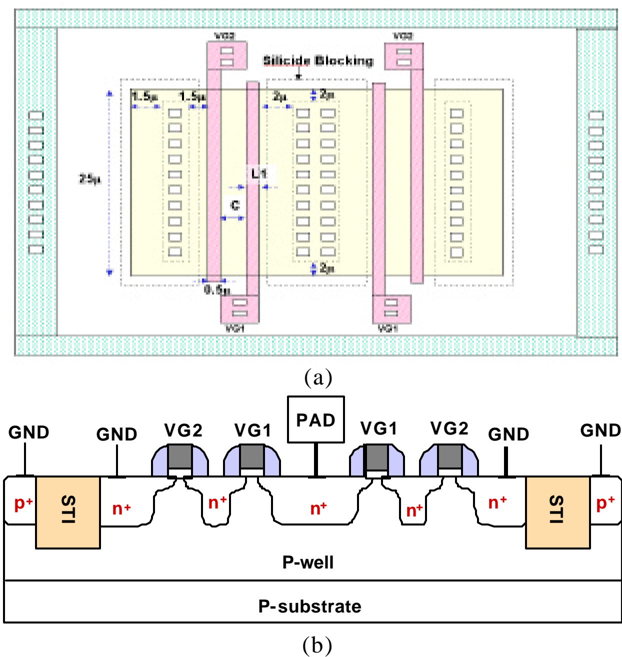


Fig. 2 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-NMOS device in a P-substrate CMOS process.

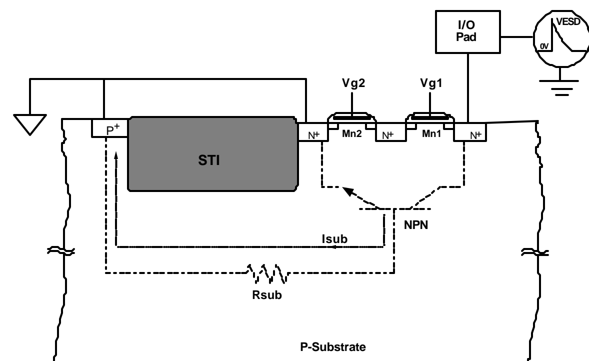


Fig. 3 The cross-sectional view of the stacked-NMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition.

The substrate-triggered technique has an obvious improve on ESD level of the large-dimension NMOS devices [11]-[12]. However, in the literature, the substrate-triggered technique was never reported to improve ESD



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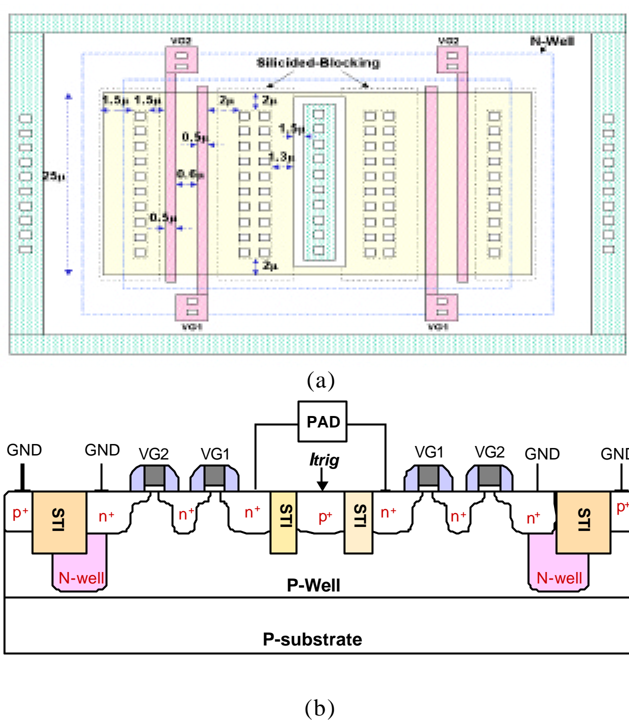
robustness of the stacked-NMOS device in the mixed-voltage I/O circuit. In this work, the substrate-triggered stacked-NMOS device that combines the substrate-triggered technique into the stacked-NOMS device is proposed.

The finger-type layout pattern and the corresponding cross-sectional view of the new proposed substrate-triggered stacked-NMOS device are shown in Fig. 4(a) and Fig. 4(b), respectively. In Fig. 4(b), the P+ diffusion is inserted into the center region of the stacked-NMOS device as the substrate-triggered point. The trigger current (Itrig) is provided by the special ESD detection circuit. An N-well structure is further diffused under the source region of this device to form a higher equivalent substrate resistance to improve turn-on efficiency of the lateral npn BJT in the stacked-NMOS device.




(a)

(b)

Fig. 4 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-NMOS device in a P-substrate CMOS process.

## 3. ESD Protection Design for Mixed-Voltage I/O Circuit

The ESD protection design including the substrate-triggered stacked-NMOS device, the substrate-triggered circuit, and the corresponding cross-sectional view are shown in Fig. 5 and Fig. 6, respectively. The substrate-triggered circuit is composed of the diode string, PMOS (P1) and NMOS (N1), to provide the substrate current for triggering on the parasitic lateral npn bipolar junction transistor contained in the stacked-NMOS device while the ESD voltage is applied on the I/O pad.

The anode of the diode string in the substrate-triggered circuit and the collector of the parasitic npn BJT in the stacked-NMOS device are connected to the I/O pad. The cathode of the diode string is connected to the source of P1. The emitter (the base) of the lateral npn BJT are connected to VSS power line (the drain of P1). The NMOS (N1) is connected between the base of the lateral npn BJT and the VSS power line. The gates of P1 and N1 are connected together to the VDD power line through a resistor, which is an N+ diffusion resistance with a parasitic N+/P-sub diode used as an antenna diode to solve the antenna effect during the fabrication process. The diode string including in the substrate-triggered circuit is composed of individual diodes formed by using P+ diffusion in the separated n-well structure.

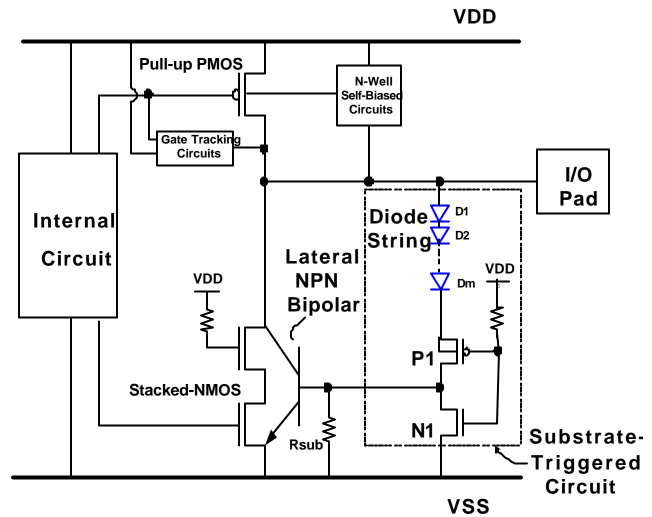



Fig. 5 The proposed on-chip ESD protection design for mixed-voltage I/O circuit with the substrate-triggered stacked-NMOS device.

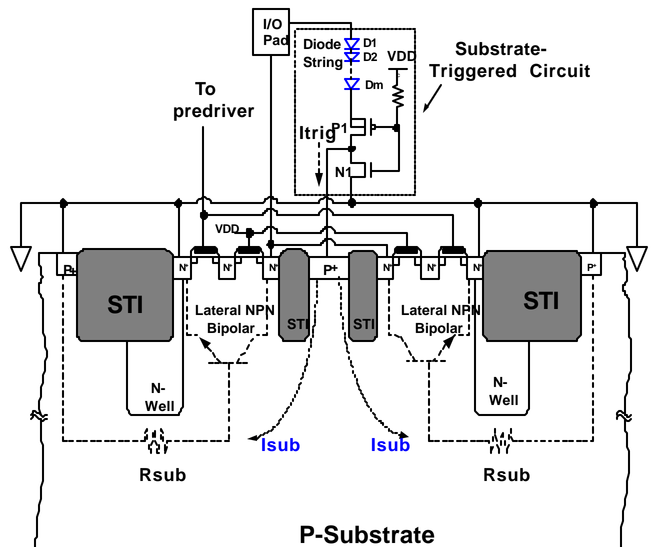



Fig. 6 The cross-sectional view of substrate-triggered stacked-NMOS device with substrate-triggered circuit.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The total voltage drop across the diode string can be expressed as

$$V_{string}(I) = mV_D(I) - nV_T[\frac{m(m-1)}{2}] \times \ell n(\boldsymbol{b}+1), \qquad (1)$$

where

$V_{string}(I)$ = total voltage drop across the m diodes;

m= the number of diodes in the diode string;

n= ideality factor; and

$\boldsymbol{b}$ = the beta gain of the parasitic vertical pnp BJT.

During the ESD stress condition, the PMOS (P1) device is used in conjunction with a diode string to provide the substrate current to trigger the lateral npn BJT. Once the lateral npn BJT has been turned on, the ESD current is discharged from the pad to VSS.

Fig. 6 shows the cross-sectional view of the substrate-triggered stacked-NMOS device with the substrate-triggered circuit for protecting mixed-voltage I/O circuits. In the normal circuit operating condition, the substrate-triggered circuit should remain in a non-conductive state, so that it does not interfere with the voltage levels on the I/O pad. For the 2.5V/3.3V mixed-voltage IC application, 3.3V tolerance was desired for normal circuit operation with a 2.5-V VDD supply in the chip.

The turn-on voltage of the substrate-triggered circuit roughly equals to Vpad ≥ $V_{string}(I)$+|Vtp|+VDD, where the Vtp is the threshold voltage of the PMOS (P1). The turn-on voltage can be adjusted by varying the number of the diodes in the diode string. To satisfy the requirement in the 2.5V/3.3V mixed-voltage application, the number of the diodes in the diode string should be adjusted to let the turn-on voltage greater than 3.3V. When the I/O pad is applied with a high voltage (3.3V), PMOS (P1) is kept off, and the substrate of the stacked-NMOS is biased at VSS.

The choice of a particular diode string is also determined by the specified pin leakage current at a given temperature. If a lower input leakage is desired, the number of the diodes in the diode string should be increased. Since the diode string is not in the main ESD current discharging path, its perimeter can be adjusted with less impact on ESD performance. The leakage problem of the diode string comes from the vertical pnp BJT of each diode formed by P+ in an n-well. The PMOS (P1) in conjunction with a diode string is used to reduce the leakage current at the I/O pad in the normal circuit operating condition. Moreover, the NMOS (N1) with its gate biased at VDD is always turned on to bypass any leakage current, which may trigger on the lateral npn BJT in the normal circuit operating condition.

Under the positive-to-VSS ESD-stress condition, the gate of PMOS (P1) has an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the PMOS (P1) into the p-substrate, when Vpad ≥ $V_{string}(I)$+|Vtp|. For a given Rsub, the substrate-triggered circuit must supply an enough trigger current (Itrig) to raise up the substrate potential, so that VBE (= Isub x Rsub) > 0.6v for triggering on the parasitic lateral npn BJT in the stacked-NMOS device. Once the parasitic lateral npn BJT is turned on, the ESD current is discharged from the I/O pad through the npn BJT to the grounded VSS. The trigger current (Itrig) provided by the substrate-triggered circuit is determined by the diode string and the size of PMOS (P1). With an appropriate Itrig, the substrate potential is raised up high enough to trigger on the lateral npn BJT and to reduce the trigger voltage of the ESD clamp circuit. Therefore, ESD robustness of the mixed-voltage I/O circuits with the stacked-NMOS devices can be effectively improved.

## 4. Experimental Results

The stacked NMOS and substrate-triggered design for mixed-voltage I/O circuit have been verified in a 0.25-μm CMOS process. The I-V characteristics of the substrate-triggered stacked-NMOS devices are measured by the Tek370A curve tracer. The ZapMaster ESD simulator is used to evaluate the ESD robustness of the devices with a failure criterion of 1-μA current leakage under a 3.3-V bias.

### *4.1 Characteristics of the Stacked-NMOS Device*

To understand the dependence of ESD robustness on the layout spacing in the stacked-NMOS device, some layout parameters are practically investigated on the fabricated testchips. The main layout parameters to affect ESD robustness of ESD protection devices are the channel width and the poly-to-poly spacing (C) across the common N+ region between the top gate and the bottom gate of stacked-NMOS device. The relations between the device channel width and HBM ESD level of stacked-NMOS are shown in Fig. 7. The HBM ESD level of the stacked-NMOS device is increased while the device channel width is increased. Moreover, the stacked-NMOS device with silicided-blocking process can sustain higher ESD level than that with the silicided diffusion. For example, the ESD level of the silicided stacked-NMOS with a channel width of 240μm is 3kV, but that of the silcided-blocking stacked-NMOS with the same device dimension and layout style is 4.5kV.

The relation between the poly-to-poly spacing (C) and the HBM ESD level of stacked-NMOS device is shown in Fig. 8. The layout style and spacing are all kept the same, but only the poly-to-poly spacing (C) is different under this investigation. From the experimental results, by decreasing the poly-to-poly spacing (C), the HBM ESD level is increased because the turn-on efficiency and performance of parasitic lateral bipolar transistors in the stacked-NMOS are significantly improved. Moreover, the stacked-NMOS device with silicide-blocking process can sustain higher ESD level than that with the silicided diffusion.


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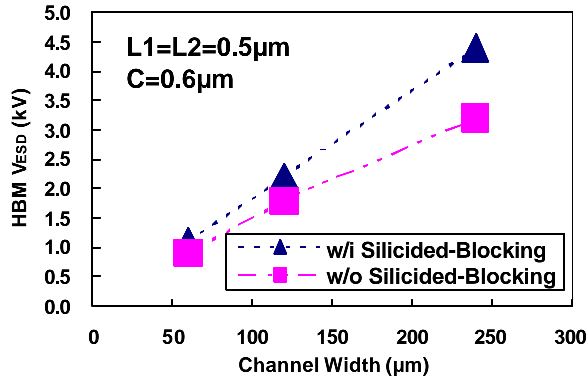


Fig. 7 Dependence of the HBM ESD level on channel width of the stacked-NMOS device. Failure criterion : Ileakage > 1µA @ Vbias=3.3V.

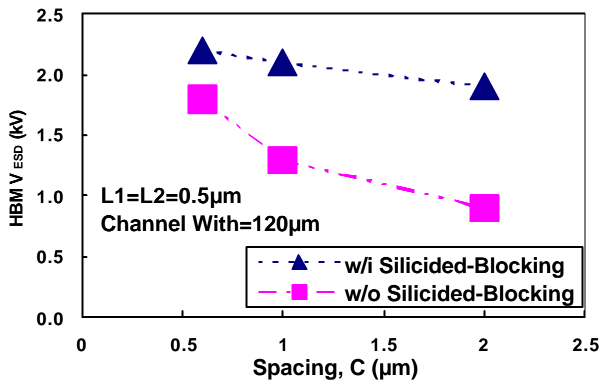


Fig. 8 Dependence of the HBM ESD level on the layout parameter C of the stacked-NMOS device. Failure criterion : Ileakage > 1µA @ Vbias=3.3V.

### *4.2 Characteristics of the Substrate-Triggered Stacked-NMOS Device*

The measured I-V characteristics of the substrate-triggered stacked-NMOS are shown in Fig. 9. The trigger voltage of the NMOS transistor decreases when the substrate-triggered current increases. The trigger voltage reduces to only 5.3V when the Itrig is 8mA. The dependence of It2 on the Itrig current under the different channel widths of substrate-triggered stacked-NMOS is shown in Fig. 10. The It2 (secondary breakdown current) is measured by the TLPG (transmission line pulse generator) with a pulse width of 100 ns. The It2 of the substrate-triggered stacked-NMOS can be increased, when the Itrig is increased. For example, the It2 is increased from 2.5A to 3.4A for the stacked-NMOS device with a channel width of 240 µm, when the Itrig increases from 0mA to 2mA.

Based on above experimental results, the ESD protection circuit can be designed with the special substrate-triggered circuit to generate the substrate current to further increase ESD robustness of the stacked-NMOS device in the mixed-voltage I/O buffer.

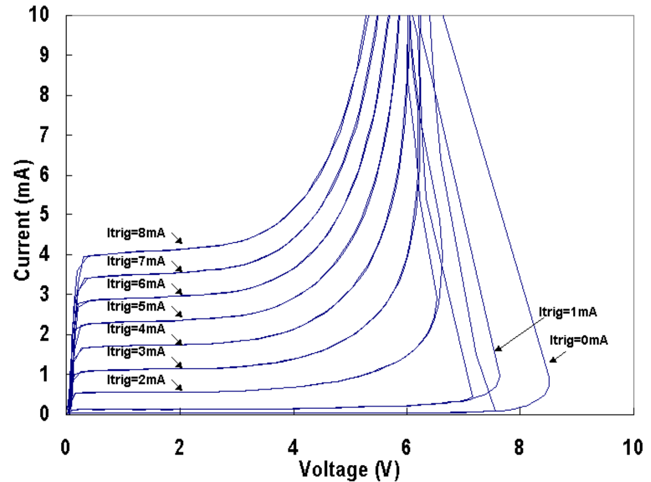


Fig. 9 The measured I-V characteristics of the substrate-triggered stacked-NMOS device with different substrate-triggered currents.

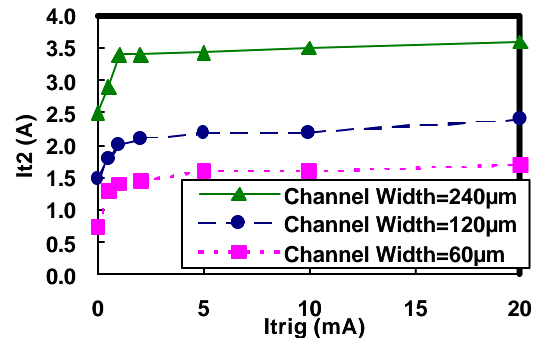


Fig. 10 The dependence of It2 on the trigger current (Itrig) of the stacked-NMOS under different channel widths.

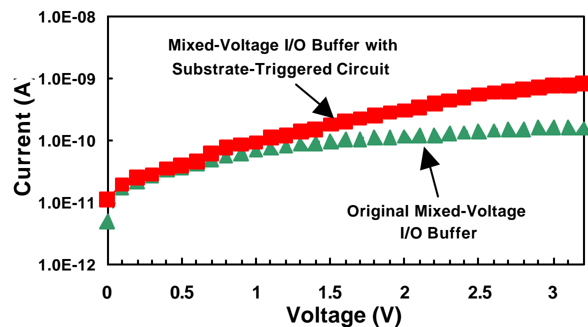


Fig. 11 The dependence of leakage current on the pad voltage (Vpad) of the mixed-voltage I/O circuits with or without substrate-triggered circuit under the temperature of 25 ° C.

### *4.3 Leakage Current*

Fig. 11 shows the dependence of leakage current on the pad voltage (Vpad) of the mixed-voltage I/O circuits with or without the proposed substrate-triggered design in Fig. 5. Here, the VDD was held at 2.5V, and the I/O pad voltage swept from 0 to 3.3V at a room temperature of 25 ºC. An input leakage current in the mixed-voltage I/O buffer with


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(without) the substrate-triggered circuit is only 1nA (0.2nA) when 3.3V is applied on the I/O pad, which is acceptable for general application. The leakage current shown in Fig.11 is measured from a mixed-voltage I/O circuit with the stacked NMOS of 240-μm channel width (for both top and bottom NMOS's) and a 480-μm pull-up PMOS. The diode string in the substrate-triggered circuit has 6 diodes. More diodes can be added into the diode string to further reduce the leakage current.

### *4.4 ESD Robustness*

The four-modes HBM (human-body-model) ESD test results of the mixed-voltage I/O buffers with or without the proposed ESD protection design are summarized in Table I. The positive-to-VSS HBM ESD levels of the proposed ESD protection circuits with different channel widths are shown in Fig. 12. The original mixed-voltage I/O buffers with different stacked-NMOS channel widths are also tested as a reference. Stacked-NMOS devices with different channel widths have the same L1=L2=0.5μm and C=1μm layout spacings. From the experimental results, HBM ESD level of the proposed ESD protection design by using stacked-NMOS with substrate-triggered technique can be improved up to ~65%. This has verified the effectiveness of the substrate-triggered design to improve ESD level of mixed-voltage I/O circuits.

**Table I**

The HBM ESD test results of the mixed-voltage I/O buffers with or without the substrate-triggered circuit under a fixed device dimension.

| I/O Circuits \ HBM ESD Stress | PS-Mode (Postive-to -VSS) | NS-Mode (Negative-to -VSS) | PD-Mode (Positive-to -VDD) | ND-Mode (Negative-to -VDD) |
|---|---|---|---|---|
| Original Mixed-Voltage I/O Buffer | 2.1kV | 6.4kV | 3.1kV | 3.9kV |
| Mixed-Voltage I/O Buffer + Substrate-Triggered Circuit | 3kV | 6.4kV | 3.3kV | 4kV |

Pull-up PMOS : W/L=240/0.5um; Stacked-NMOS : W/L=120/0.5um w/i Silicided-Blocking

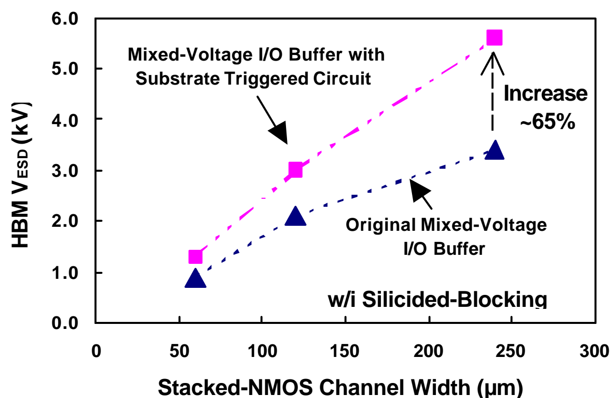


Fig. 12 The positive-to-VSS (PS-mode) HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit realized in a 0.25-μm CMOS process with silicided-blocking mask.

## 5. Conclusion

To improve ESD robustness of the stacked-NMOS devices in mixed-voltage I/O circuits, a new ESD protection circuit has been designed and successfully verified in a 0.25-μm CMOS process. From the experimental results, the positive-to-VSS HBM ESD level of the mixed-voltage I/O circuit with a stacked-NMOS of 240-μm channel width can be improved from the original 3.4 kV up to 5.6 kV (increase of ~65%) by using the substrate-triggered design. The trigger voltage of stacked-NMOS device can be reduced from the original 8.5V to become 5.3V to ensure effective protection for the mixed-voltage I/O circuit. This design is very useful in the sub-quarter-micron CMOS processes.

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