# Study of Board-Level Noise Filters to Prevent Transient-Induced Latchup in CMOS Integrated Circuits during EMC/ESD Test

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Abstract—Different types of board-level noise filters are evaluated for their effectiveness to improve the immunity of CMOS ICs against transient-induced latchup (TLU) under system-level electrostatic discharge (ESD) test. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs can be greatly improved. All the experimental evaluations have been verified in test chips with the silicon controlled rectifier (SCR) fabricated in a 0.25- $\mu$ m CMOS technology. Some of such board-level solutions can be further integrated into the chip design to effectively improve TLU immunity of CMOS IC products.

### I. INTRODUCTION

Transient-induced latchup (TLU) is an increasingly significant reliability issue in CMOS technology [1]. This tendency results from not only the progress of the functionality of CMOS ICs such as RF, system on chip (SOC), mixed-signal, etc, but also the strict requirements of reliability test standards such as system-level ESD test [2] for electromagnetic compatibility (EMC) regulation. The inset figure of Fig. 1 shows the measurement setup of the system-level ESD test with indirect contactdischarge test mode [2]. When the ESD gun zaps to the horizontal coupling plane (HCP), all CMOS ICs inside the equipment under test (EUT) will be disturbed due to the high ESD-coupled energy. The measured  $V_{DD}$ transient waveform on one of CMOS ICs inside the EUT during ESD zapping with ESD voltage of -1000V is shown in Fig. 1. Clearly, the power line of the CMOS IC no longer maintain its normal DC voltage level (+2.5V), but acts as an underdamped sinusoidal voltage. Such underdamped sinusoidal voltage on power or ground lines of CMOS ICs can easily induce TLU [3], even if such TLU-sensitive CMOS ICs have already met the requirements of the quasi-static latchup test standard [4].

To improve the TLU immunity of CMOS ICs, an intuitional solution is the usage of the noise filter network between the noise sources and CMOS ICs to decouple, bypass, or absorb noise voltage (energy) which may initiate TLU. The purpose of this work is to develop a high efficiency board-level noise filter network for TLU prevention. Different types of noise filter networks, including capacitor filter, ferrite bead, transient voltage suppressor (TVS), and several high-order noise filters such as LC-like and  $\pi$ -section filters, are evaluated to see their improvements on TLU immunity. All the experimental results have been verified with the SCR test chips fabricated in a 0.25- $\mu$ m CMOS technology.

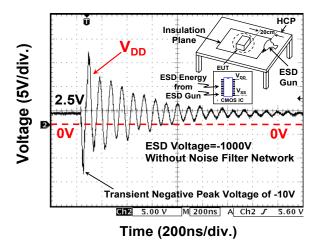


Fig. 1. The measured  $V_{DD}$  transient waveform on one of CMOS ICs inside the EUT during ESD zapping on the HCP with ESD voltage of -1000V. The inset figure shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode.

## II. TEST STRUCTURE

An SCR structure is used as the test structure for TLU measurements because the occurrence of latchup results from the parasitic SCR in CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 2(a) and 2(b), respectively. The geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. All the SCR structures are fabricated in a 0.25-µm salicided CMOS technology.

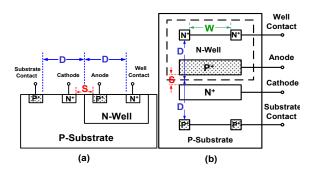


Fig. 2. (a) Device cross-sectional view, and (b) layout top view, of the SCR structure for TLU measurements.

### III. MEASUREMENT SETUP

During the system-level ESD test, we can only judge whether the EUT passes the required criterion through the abnormal function of EUT (e.g. EUT shuts down). Nevertheless, it is difficult to directly evaluate the TLU immunity of single IC inside the EUT. To solve this issue, a component-level TLU measurement setup with bipolar trigger waveform [5] is used in this work, as shown in Fig. 3. It has the advantage of easily evaluating the TLU immunity of single IC by monitoring the measured voltage/current waveforms oscilloscope. More importantly, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how a CMOS IC inside the EUT will be disturbed by the ESD-coupled noises during the system-level ESD test. In this measurement setup, an ESD simulator is used to generate the underdamped sinusoidal trigger source, V<sub>Charge</sub>. A capacitor of 200pF used in the machine model (MM) ESD test [6] is employed as the charged capacitor. Noise filter network located between TLU-triggering source (V<sub>Charge</sub>) and the device under test (DUT) is used to decouple, bypass, or absorb noise voltage (energy) produced by TLUtriggering source. The DUT is the SCR structure shown in Fig. 2. The P<sup>+</sup> anode and the N<sup>+</sup> well contact of SCR are connected together to  $V_{DD}$ , whereas the  $N^+$  cathode and the P<sup>+</sup> substrate contact are connected together to V<sub>SS</sub> (ground). I<sub>DD</sub> is the total current flowing into the P<sup>+</sup> anode and the N<sup>+</sup> well contact of SCR. Furthermore, a small current-limiting resistance of  $5\Omega$  is used to avoid the possible electrical over-stress (EOS) damage under a high-current latchup state [7].

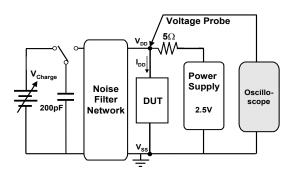


Fig. 3. A component-level TLU measurement setup with bipolar trigger waveform.

With the component-level TLU measurement setup in Fig. 3, the measured  $V_{DD}$  and  $I_{DD}$  transient responses with  $V_{Charge}$  of -2V and -7V are shown in Figs. 4(a) and 4(b), respectively. Both cases have no noise filter network between the TLU-triggering source and DUT (i.e. SCR with the specified device layout parameters of D=16.6µm, S=20µm, and W=22.5µm). With a smaller  $V_{Charge}$  of -2V, TLU doesn't occur because  $I_{DD}$  doesn't significantly increase after applying the underdamped sinusoidal noise on  $V_{DD}$ , as shown in Fig. 4(a). However, with a larger  $V_{Charge}$  of -7V, TLU can be initiated, because  $I_{DD}$  significantly increases (up to 60mA) and  $V_{DD}$  is pulled down to the latchup holding voltage (1.8V)

after triggering, as shown in Fig. 4(b). In Fig. 4(a),  $V_{\rm DD}$  acts as the underdamped sinusoidal voltage just as that under the system-level ESD test in Fig. 1. Thus, this component-level TLU measurement setup can be used to evaluate different types of board-level noise filter networks for their effectiveness to improve TLU immunity of CMOS ICs under system-level ESD test.

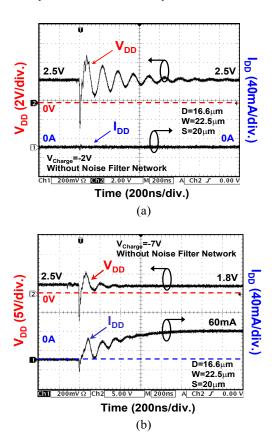


Fig. 4. The measured  $V_{DD}$  and  $I_{DD}$  transient responses of the SCR with  $V_{\text{Charge}}$  of (a) -2V and (b) -7V. Both cases have no noise filter network between TLU-triggering source and the SCR.

### IV. EXPERIMENTAL EVALUATIONS

Different types of noise filter networks are investigated for their effectiveness to improve the TLU immunity of the SCR structure, including: (1) capacitor filter, (2) LC-like filter, (3)  $\pi\text{-section filter,}$  (4) ferrite bead, (5) TVS, and (6) hybrid type filters based on the combinations with TVS and ferrite bead. The SCR structure for all cases has the specified layout parameters of D=16.6 $\mu m$ , S=20 $\mu m$ , and W=22.5 $\mu m$ .

## A. TLU Level of the SCR Structure without Noise Filter Network

Without the noise filter network, the component-level TLU measurement setup in Fig. 3 can be used to evaluate the TLU level of the SCR with various geometrical parameters. The TLU level is defined as the minimum positive (negative)  $V_{\text{Charge}}$  which can trigger on TLU. Thus, higher TLU level is better for DUT, because

it means that the DUT is less sensitive to TLU under the system-level ESD test. The specified SCR structure (with D=16.6µm, S=20µm, and W=22.5µm) used in this work has a very low positive (negative) TLU level of +15V (-7V). Actually, it was found that all the SCR structures are rather susceptible to TLU (the magnitudes of both positive and negative TLU levels are all smaller than 20V) unless the SCR is initially latchup-free (i.e. latchup holding voltage > normal operating voltage of +2.5V). Thus, due to such weak immunity to TLU, the noise filter network is indeed necessary to improve TLU immunity of DUT through bypassing, decoupling, or absorbing noise voltage (energy) between the TLU-triggering source and DUT.

### B. TLU Level of the SCR Structure with Noise Filter Network

Capacitor Filter, LC-Like Filter, and π-Section Filter
 Three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter are depicted in Figs.

5(a), 5(b), and 5(c), respectively. Fig. 6 shows their improvements on both positive and negative TLU levels of the SCR structure.

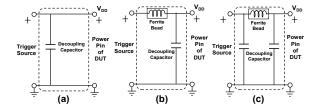


Fig. 5. Three types of noise filter networks: (a) capacitor filter, (b) LC-like filter, and (c)  $\pi$ -section filter.

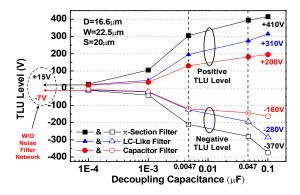


Fig. 6. The relations between the decoupling capacitance and the TLU level of SCR under three types of noise filter networks: capacitor filter, LC-like filter, and  $\pi$ -section filter.

The ceramic disc capacitor with advantages of high working voltage (1kV), good thermal stability, and low loss at wide range of frequency is employed as the decoupling capacitor in the noise filter of Fig. 5. Decoupling capacitances widely ranging from 100pF to  $0.1\mu F$  are used to investigate their improvements on TLU level of the SCR structure. With the aid of the capacitor filter, the positive TLU level can be significantly enhanced from +15V (without decoupling

capacitor) to +200V (with decoupling capacitance of 0.1  $\mu F$ ), as shown in Fig. 6. Similarly, the negative TLU level can be also significantly enhanced from -7V (without decoupling capacitor) to -160V (with decoupling capacitance of 0.1  $\mu F$ ). Thus, by choosing a proper capacitance value, a simple 1st-order decoupling capacitor placed between  $V_{DD}$  and  $V_{SS}$  (ground) of CMOS ICs can be used to improve the TLU immunity of DUT under the system-level ESD test, no matter for the positive or the negative ESD voltage.

The ferrite bead, which is commonly used for absorbing RF energy, substitutes inductor as a secondorder LC-like filter component in Fig. 5(b). Here, a resistor-type ferrite bead (part number: RH 3.5x9x0.8 with minimum impedance of  $80\Omega$  (120 $\Omega$ ) at 25MHz (100MHz)) is employed. Due to a higher insertion loss (2nd-order filter), such LC-like filter has better TLU level enhancements than that with the capacitor filter (1st-order filter). For example, the positive TLU level can be significantly enhanced from +15V (without decoupling capacitor) to +310V (with decoupling capacitance of 0.1µF), as shown in Fig. 6. Similarly, the negative TLU level can be also significantly enhanced from -7V (without decoupling capacitor) to -280V (with decoupling capacitance of 0.1µF). Thus, in order to achieve a higher TLU level, the LC-like filter can be used to avoid the usage of an excessively or unreasonably large decoupling capacitance in a simple 1st-order capacitor filter.

A 3rd-order  $\pi$ -section filter is used to further enhance the TLU level of the SCR, as shown in Fig. 5(c). This  $\pi$ -section filter consists of a ferrite bead (the same one in Fig. 5(b)) and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filter networks in Figs. 5(a), 5(b), and 5(c), the TLU level of SCR can be most greatly improved. For example, with the decoupling capacitance of  $0.1\mu\text{F}$ , the positive (negative) TLU level can be significantly enhanced up to +410V (-370V), which is much higher than those with capacitor filter or LC-like filter, as shown in Fig. 6.

## (2). Ferrite Bead, TVS, and Hybrid Type Filters

Four other types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II are depicted in Figs. 7(a), 7(b), 7(c), and 7(d), respectively. Fig. 8 shows their improvements on both positive and negative TLU levels of the SCR structure.

The ferrite bead can absorb RF energy while the noise-induced time-varied current flows through it. The resistor-type ferrite beads with three different minimum impedances at 25MHz are employed in this work:  $35\Omega$ ,  $50\Omega$ , and  $80\Omega$ . However, a noise filter network with only ferrite bead alone doesn't perform well enhancement on TLU level because of a worse energy-absorbing ability at frequency lower than 10MHz [8]. As a result, TLU level of the SCR structure will not be efficiently improved (the magnitudes of both positive and negative TLU levels are all lower than 25V), even though the minimum impedance of the ferrite bead at 25MHz is as high as  $80\Omega$ .

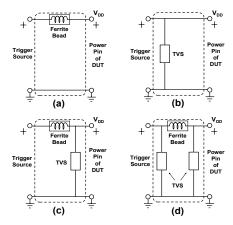


Fig. 7. Four other types of noise filter networks: (a) ferrite bead, (b) TVS, (c) hybrid type I, and (d) hybrid type II.

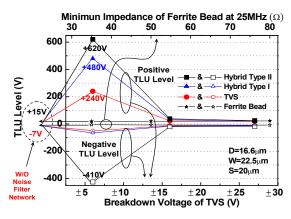


Fig. 8. The relations among the TLU level of SCR, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

TVS, which is commonly used to bypass/decouple the high-frequency noises, is also considered for improving TLU immunity of the SCR. The bidirectional-type TVS (part number: P6KE series) with three different breakdown voltages,  $V_{BR},\,(\pm 6.8V,\,\pm 16V,$  and  $\pm 27V)$  are employed in this work. As shown in Fig. 8, the TVS with breakdown voltage of ±16V or ±27V fail to improve TLU level of the SCR (the magnitudes of both positive and negative TLU levels are all lower than 25V), because TLU occurs prior to the breakdown of such high-V<sub>BR</sub> TVS. That is, the intrinsic (without noise filter network) TLU level of SCR (positive and negative TLU level of +15V and -7V) is smaller than the  $V_{BR}$  (±16V and  $\pm 27V$ ) of such high-V<sub>BR</sub> TVS. Thus, only the TVS with  $V_{\text{BR}}$  lower than the intrinsic TLU level of DUT can effectively enhance the TLU level. For example, the positive (negative) TLU level can be enhanced up to +240V (-50V) with a low- $V_{BR}$  ( $\pm 6.8V$ ) TVS.

Hybrid type filters consisting of both ferrite bead (minimum impedance of  $80\Omega$  at 25MHz) and TVS (with different  $V_{BR}$ ) are also evaluated for their improvements on TLU level of the SCR, as shown in Figs. 7(c) and 7(d). Hybrid types I and II are the counterparts of the LC-like and  $\pi$ -section filters where the TVS substitutes

the decoupling capacitor as a noise-bypassing component. As shown in Fig. 8, only the hybrid type filters with a low- $V_{BR}$  ( $\pm 6.8V$ ) TVS can efficiently improve the TLU level. In addition, because such higher-order hybrid type filters provide the higher insertion loss, they can enhance the TLU level of SCR more greatly than ferrite bead or TVS alone. For example, for hybrid type filters with a low- $V_{BR}$  ( $\pm 6.8V$ ) TVS, hybrid type I (II) can greatly enhance the positive TLU level up to +480V (+620V), and enhance the negative TLU levels up to -65V (-410).

Through investigating different types of noise filter networks for their improvements on TLU levels in Figs. 6 and 8, it can be found that TVS (hybrid type I) doesn't improve the negative TLU level as greatly as the 1st-order capacitor filter (LC-like filter) does. For example, the negative TLU level can be greatly enhanced up to -160V (-280V) for 1st-order capacitor filter (LC-like filter) with decoupling capacitance of  $0.1\mu\text{F}$ , but only up to -50V (-65V) for TVS (hybrid type I) with a low  $V_{BR}$  of  $\pm 6.8\text{V}$ . Thus, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance negative TLU level more efficiently but also is compatible to CMOS technology for integrating the noise filter into chips.

#### V. CONCLUSION

By choosing proper components in each board-level noise filter network, the TLU immunity of CMOS ICs under the system-level ESD stresses can be greatly improved. From the experimental results, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance the negative TLU level more efficiently but also is compatible to CMOS technology for integrating the noise filter into chips. To further improve the TLU immunity of electronic products, proper board-level solutions can be combined with chiplevel solutions to meet the applications with strict system-level ESD specification.

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