System-Level ESD Protection Design with On-Chip Transient Detection Circuit

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***Abstract*—A new on-chip transient detection circuit for system-level electrostatic discharge (ESD) protection is proposed. By including this new proposed on-chip transient detection circuit, a hardware/firmware solution cooperated with power-on reset circuit has been analyzed to fix the system-level ESD issues. The circuit performance to detect different positive and negative fast electrical transients has been investigated by HSPICE simulator and verified in silicon chip. The experimental results in a 0.13-μm CMOS process have confirmed that the proposed on-chip transient detection circuit can detect fast electrical transients during system-level ESD zapping.**

I. Introduction

System-level ESD issue is an increasingly significant reliability issue in CMOS IC products [1]. This tendency results from the strict requirements of reliability test standards, such as system-level ESD test for electromagnetic compatibility (EMC) regulation [2]. In the system-level ESD test standard of IEC 61000-4-2, the electrical/electronic product must sustain the ESD level of +8kV (+15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4." Such high-energy ESD-induced noises often cause damage or malfunction of CMOS ICs inside the equipment under test (EUT). It has been found that some CMOS ICs are very susceptible to system-level ESD stress, even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2kV, machine-model (MM) of ±200V, and charged-device-model (CDM) of ±1kV.

In the test standard of IEC 61000-4-2, two test modes have been specified: air-discharge test mode and contact-discharge test mode. Fig. 1 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode, which consists of a wooden table on the grounded reference plane (GRP). In addition, an isolation plane is used to isolate the EUT from horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470kΩ resistors in series. When the ESD gun zaps to the HCP, all CMOS ICs inside the EUT will be disturbed due to the high ESD-coupled energy. Fig. 2 shows the measured V_{DD} transient waveform on one of the CMOS ICs inside the EUT when an ESD voltage of -1000V is directly zapping on the HCP plane. Clearly, the power lines (pins) of the CMOS IC no longer maintain their normal voltage levels, but acts as an underdamped sinusoidal voltage instead (with transient negative peak voltage of -13V).

When such a fast transient occurs on the power pins of CMOS ICs, it has been investigated that the logic states stored in the microcontroller of microelectronic products can be easily destroyed to cause the CMOS ICs upset or frozen after the system-level ESD zapping. In order to meet the system-level ESD specifications, some discrete noise-decoupling components or board-level noise filters are added into the printed circuit board (PCB) to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test, such as capacitor filters, ferrite bead, transient voltage suppressor (TVS), or low-pass noise filters [3]. However, the additional discrete noise-bypassing components increase the total cost of microelectronics system. Therefore, an on-chip solution integrated with the CMOS ICs, but without adding additional cost on the PCB, is strongly requested by IC industry.

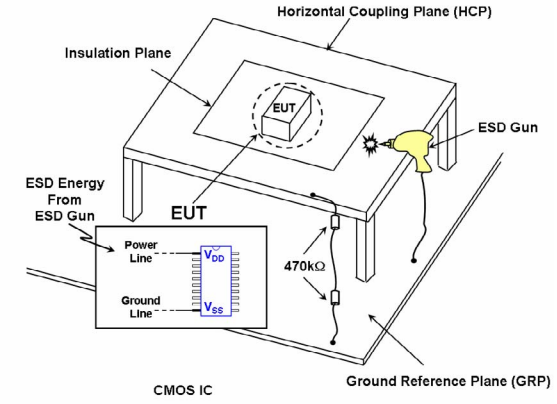

Fig. 1. Measurement setup of the system-level ESD test with indirect contact-discharge test mode. The ESD gun zapping on the horizontal coupling plane (HCP) could cause underdamped sinusoidal voltage waveform on power lines of CMOS ICs insude the EUT.

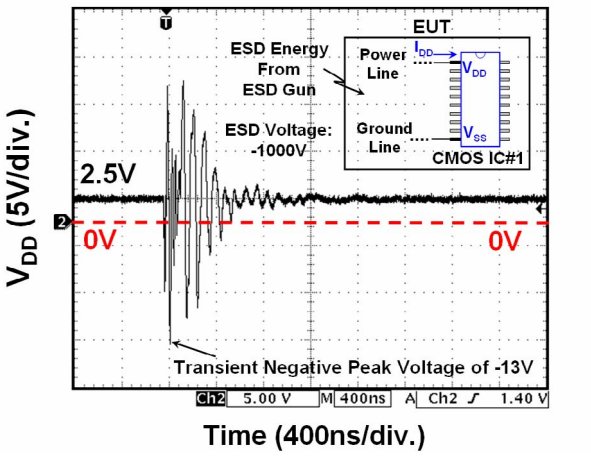

Fig. 2. Measured VDD transient waveform on the CMOS ICs inside EUT with the abn ESD voltage of -1000V zapping on the HCP. VDD waveform acts as a underdamped sinusoidal voltage due to the distance of the high ESD-coupled energy.

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In this paper, an on-chip transient detection circuit is proposed to detect the fast electrical transient under the system-level ESD test. The new proposed transient detection circuit can be combined with the power-on reset circuit to provide a hardware/firmware system co-design for system-level ESD solution. The performance of new proposed transient detection circuit to sense different fast electrical transients has been investigated by HSPICE and verified in silicon chip. The experimental results in a 0.13-μm CMOS process have confirmed that the proposed on-chip transient detection circuit can successfully detect fast electrical transients during system-level ESD zapping.

II. System Design for ESD Protection

The hardware/firmware co-design can effectively improve the system-level ESD susceptibility of the CMOS IC products. As shown in the flowchart in the Fig. 3, the detection results (V_{OUT}) from the on-chip ESD sensors can be temporarily stored as an ESD flag for firmware check. The states in the transient detection circuit and the ESD flag are initially cleared to logic "0" by the power-on reset. The reset procedure is executed through the normal firmware reset procedure when the ESD flag has a state of logic "0". When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient to change the output states V_{OUT} to logic "1". At this time, the ESD flag is re-stored at logic "1", as well as the firmware executes the recover procedure to recover all system functions to a stable state as soon as possible. After the reset and recover procedures, the states in the transient detection circuit and the ESD flag are re-set to logic "0" again for detecting the next ESD events.

To realize system-level hardware/firmware co-design ESD protection function, a hardware/firmware system co-design combined the transient detection circuit and the power-on reset circuit has been analyzed. Under the normal power-on condition, the VDD power-on voltage waveform has a rise time in the order of millisecond (ms). As there is no input signal except VDD power-on voltage waveform, the power on reset circuit should be designed with the same internal delay as the order of millisecond. Thus, the output signal of power-on reset circuit can set the ESD flag into logic "0", as shown in Fig. 4. However, there are some mis-triggered conditions for power-on reset circuit. For example, a sudden surge can result in a very short interval between the power-down and power-up. Such short interval of power-off creates difficult situations for the power-on reset circuit to work properly. Therefore, a transient detection circuit is designed to sense fast electrical transients on power lines and combined with the power-on reset circuit in order to provide hardware/firmware co-design solution for system-level ESD issues.

Due to the difference in the rise times between the ESD voltage and the VDD power-on voltage, the on–chip transient detection circuit is designed to sense fast electrical transients and make the flag signal into logic "1", as shown in Fig. 5. Then, the firmware can execute the recover procedure to recover all the electrical functions to a stable state as soon as possible. After the reset and recover procedures, the ESD flag is reset to logic 0 again for detecting the transient ESD events.

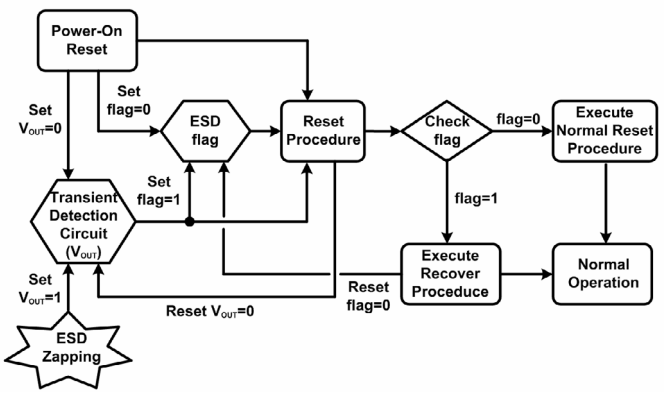


Fig. 3. Firmware flowchart to reset or recover the system if the on-chip ESD sensor detects the electrical transient during the system-level ESD stress.

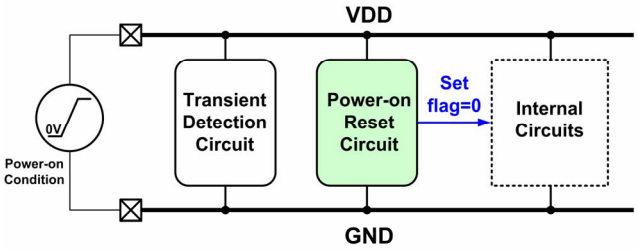


Fig. 4. Hardware/firmware operation during power-on reset condition.

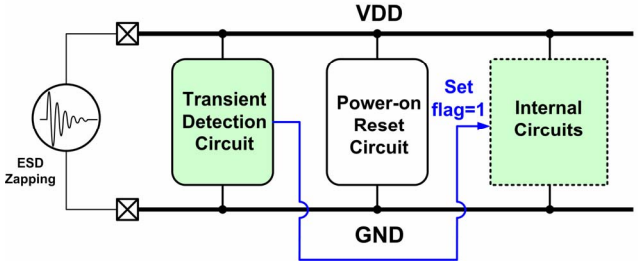


Fig. 5. Hardware/firmware operation during the system-level ESD stress.

By including the on-chip transient detection circuit and an additional ESD flag into the chip, the firmware flowchart shown in Fig. 3 can be used to improve the susceptibility of microelectronic products. Such hardware/firmware co-design method can provide an effective system solution to solve the system-level ESD issues in microelectronics system with CMOS ICs.

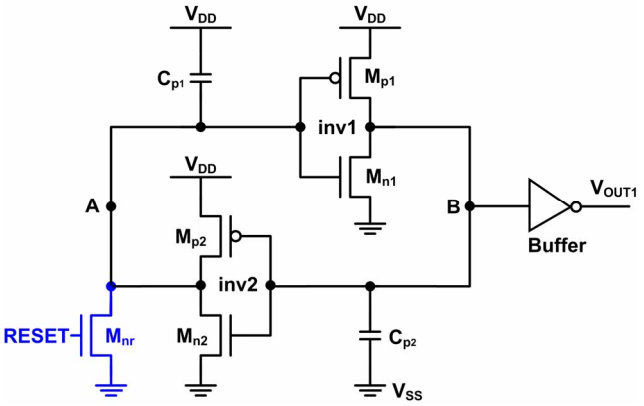
III. Transient Detection Circuit

A. Circuit Structure

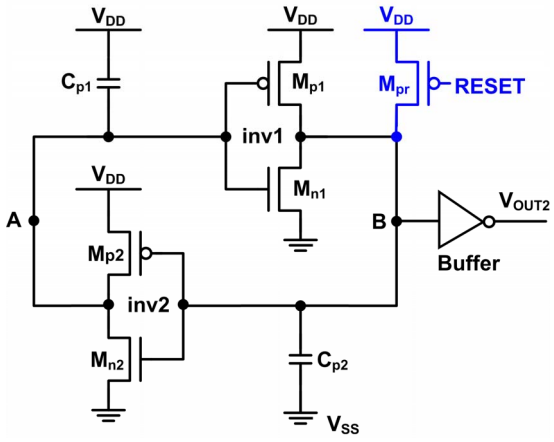
The proposed transient detection circuits realized with NMOS-reset and PMOS-reset functions are shown in Figs. 6(a) and 6(b), respectively. The detection circuits, composed of one latch and two coupling capacitances, are designed to memorize the occurrence of system-level ESD events and to sense the fast electrical transient on the power and ground lines. The detection circuits shown in Figs. 6(a) and 6(b) are realized with 3.3V devices in a standard 0.13-μm CMOS process for 3.3-V circuit applications. The output signal of proposed on-chip transient detection circuit with NMOS-reset function is V_{OUT1}, and the output signal of proposed on-chip transient detection circuit with PMOS-reset function is V_{OUT2}.

In order to increase the operation speed of detection circuit in Figs. 6(a) and 6(b) during fast electrical transient under the system-level ESD zapping, the device ratios (W/L) of latch should be adjusted. In order to pull down the voltage level of node B easily, the NMOS (M_{n1}) in the inverter1 (inv1) is designed with a larger W/L than that of PMOS (M_{p1}). On the contrary, to pull up the voltage level of node A easily, the PMOS (M_{p2}) in the inverter2 (inv2) is designed with a larger W/L ratio than that of NMOS (M_{n2}).

In order to enhance the sensitivity of the detection circuit to electrical transient, two capacitances (C_{P1} and C_{P2}) are added between the node A (B) and V_{DD} (V_{SS}). The capacitance C_{P1} (C_{P2}) is placed between the V_{DD} (V_{SS}) and the input of inv1 (inv2) in order to sense fast electrical transient on V_{DD} (V_{SS}). The NMOS (M_{nr}) in Fig. 6(a) and the PMOS (M_{pr}) in Fig. 6(b) are used to provide the reset function in order to avoid the metastable operation of the latch circuit. With the reset signal of 3.3V (0V), the node A (B) of the detection circuit shown in Figs. 6(a) (Fig. 6(b)) can be initially set up to 0V (3.3V). In normal condition, the outputs (V_{OUT1} and V_{OUT2}) of the proposed transient detection circuits will be kept at logic "0". When a system-level ESD event occurs, the fast transient noises injecting to the power lines (V_{DD} and V_{SS}) will change the output state from logic "0" to become logic "1". Therefore, the system-level ESD event can be detected by the proposed detection circuits.



(a)



(b)

Fig. 6. The proposed on-chip transient detection circuits realized with (a) NMOS-reset, and (b) PMOS-reset, functions.

B. Simulation

A simulation tool (HSPICE) is used to investigate the on-chip detection circuit performance under the system-level ESD test. In this simulation tool, an underdamped sinusoidal waveform is used to simulate fast electrical transients on the power lines of the proposed transient detection circuits.

The simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with a positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} are shown in Fig. 7. The positive-going underdamped sinusoidal voltage with amplitude of +20V is used to simulate the positive ESD stress under the system-level ESD test. Under ESD stress, V_{DD}/V_{SS} begins to increase rapidly from 3.3V/0V. V_{OUT1} and V_{OUT2} are disturbed simultaneously during V_{DD}/V_{SS} disturbance. During this period, the transient detection circuit can detect the occurrence of disturbance on V_{DD}/V_{SS}. As a result, after V_{DD} finally returns to its normal voltage level of 3.3V, V_{OUT1} and V_{OUT2} will be changed from 0V to 3.3V.

The simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with a negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} are shown in Fig. 8. The negative-going underdamped sinusoidal voltage with amplitude of -20V is used to simulate the negative ESD stress under the system-level ESD test. The V_{OUT1} and V_{OUT2} are influenced by the V_{DD}/V_{SS} disturbance through coupling paths. Finally, the outputs (V_{OUT1} and V_{OUT2}) of the transient detection circuits are changed from 0V to 3.3V.

By using HSPICE, the circuit performance of proposed transient detection circuit to sense fast electrical transients has been analyzed. From these simulations, the output states of detection circuits can be changed and kept at logic "1", after the system-level ESD events. The sensitivity of the ESD detection circuits on the electrical transient stress can be analyzed by changing the coupling capacitances between the nodes A (B) and V_{DD} (V_{SS}) or by changing the device ratios (W/L) in the latch. The HSPICE simulation can be used to fine tune the device sizes in the proposed transient detection circuits to detect different transient levels.

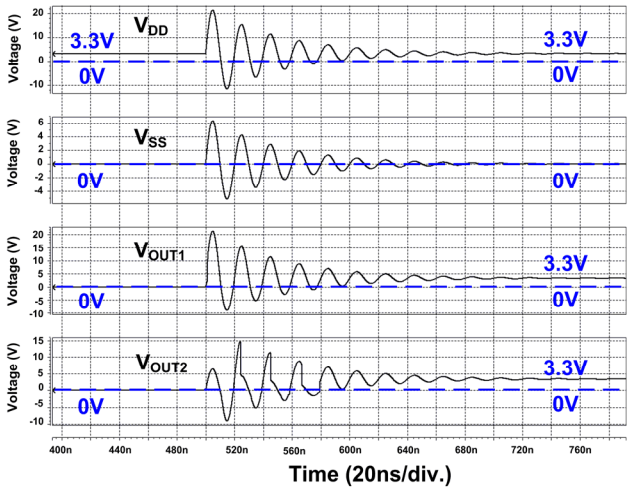


Fig. 7. Simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuits with positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}.

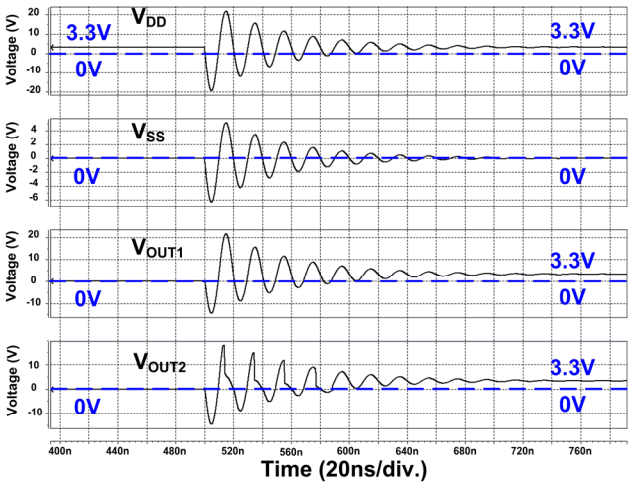


Fig. 8. Simulated V_{DD}, V_{SS}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}.

IV. Experimental Results

The proposed on-chip transient detection circuits have been fabricated in a 0.13-μm 1.2/3.3-V 1P8M CMOS process. The system-level ESD test with indirect contact-discharge test mode is used to experimentally verify the proposed transient detection circuit. With both positive and negative fast electrical transient, the measured V_{DD} transient response can be recorded by the oscilloscope. This can clearly indicate whether the detection circuit works correctly during the system-level test.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed transient detection circuit with ESD voltage of +1500V zapping on the HCP under system-level ESD test are shown in Fig. 9. V_{DD} begins to increase rapidly from the normal voltage (+3.3V). Meanwhile, V_{OUT1} and V_{OUT2} begin to greatly increase with such high-energy ESD stress. During the period with disturbance on V_{DD}, V_{OUT1} and V_{OUT2} are disturbed simultaneously. Finally, the output voltage of the transient detection circuit is changed from 0V to 3.3V. As a result, the transient detection circuit can memorize the occurrence of the system-level ESD stress. The experimental results in Fig. 9 are consistent with the HSPICE simulation results in Fig. 7.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} transient waveforms of the proposed transient detection circuits with ESD voltage of -1500V zapping on the HCP under system-level ESD test are shown in Fig. 10. During V_{DD} disturbance, V_{OUT1} and V_{OUT2} are disturbed simultaneously. Obviously, V_{OUT1} and V_{OUT2} are finally pulled up to the 3.3V after the fast electrical noise. The experimental results in Fig. 10 are consistent with the HSPICE simulation results in Fig. 8.

The circuit performance of the transient detection circuit under the system-level ESD test has been proved by both the experimental results in silicon chip and the HSPICE simulation. From the experimental results, the proposed transient detection circuit can indeed memorize the occurrence of system-level ESD stress.

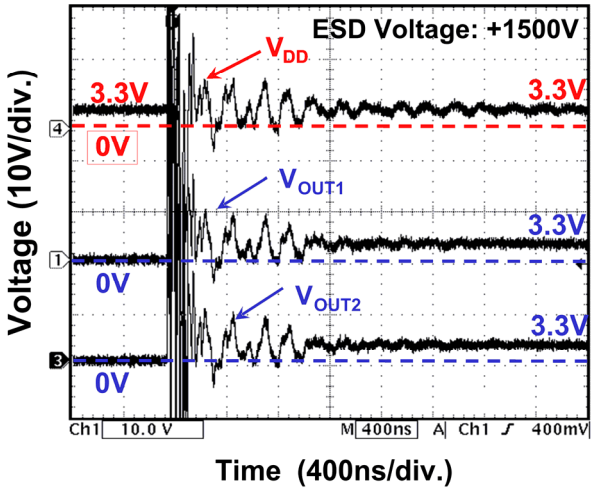


Fig. 9. Measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses with ESD voltage of +1500V zapping on the HCP under system-level ESD test.

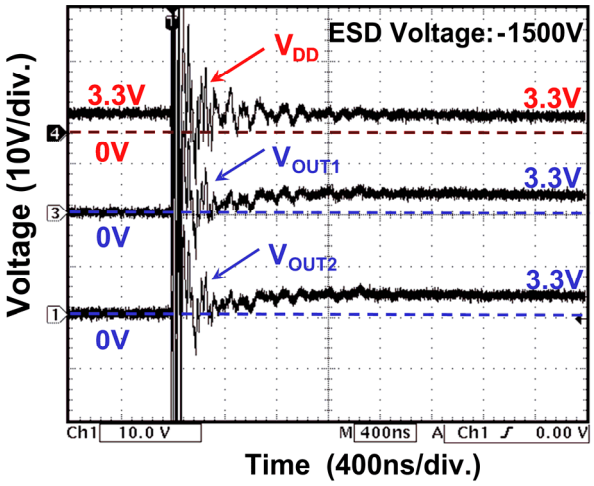


Fig. 10. Measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses with ESD voltage of -1500V zapping on the HCP under system-level ESD test.

V. Conclusion

A new transient detection circuit for system-level ESD protection has been implemented in a 0.13-μm CMOS process. The proposed transient detection circuit can be combined with power-on reset circuit and firmware design to provide an effective solution to solve the system-level ESD issue in microelectronics system with CMOS ICs. The experimental results in silicon chip have confirmed that the proposed on-chip transient detection circuit can detect fast electrical transients during system-level ESD zapping.

References

[1] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821–1831, Aug. 2005.

[2] IEC 61000-4-2 Standard, "*EMC – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*," IEC, 2001.

[3] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. on Electromagnetic Compatibility*, vol. 48, no. 1, pp. 161–171, Feb. 2006.