# Low-Power Wordline Voltage Generator for Low-Voltage Flash Memory

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*Abstract*—**Wordline voltage generating circuit with high speed active mode and low power standby mode is proposed. In the active mode, two different ring oscillators with high clock frequency ($f_{CLK}$) 170MHz, and low clock frequency ($f_{CLK}$) 25MHz which is also the operating frequency of the entire circuit, are employed. The proposed circuit has a short response time of 3μs typically in active mode, and very low standby current about 3μA in standby mode.**

## I. INTRODUCTION

Recently, flash memories are in widespread applications especially in many portable products, such as cellular phones, palm-top computers, and so on. For most of portable products, power consumption is an important issue needed to be concerned because a long battery life is an extreme merit. To reduce the power consumption, the simplest and most efficient way is to reduce its power supply voltage [1]. However, too low power supply voltage degrades circuit performance. For example, speed, dynamic range, and noise margin are affected. For flash memory applications, the high voltage operation in programming, erasing, or reading is also difficult to achieve with low power supply voltage. So, the voltage boosting circuit is used to boost power supply voltage to higher voltage level as required.

Two ways used mostly in voltage boosting circuits are Dickson charge pump [2] and capacitor-switched booster circuit [3]. The Dickson charge pump takes advantage of lower power, smaller chip area, and fast access time while suffering from the standby current compared with capacitor-switched booster circuit [3]. To reduce the average current in the standby mode is a crucial issue when Dickson charge pump is used as voltage boosting circuit. In [4], the wordline voltage generating circuit for low-power and low-voltage flash memories had been proposed to provide a good architecture and solution to reduce the standby current of Dickson charge pump in the standby mode. In case of the resistive load is connected to the output in active mode, the response time increases on account of the finite load current. The response time is defined by the time when output voltage varies from 0V to its specified steady state voltage.
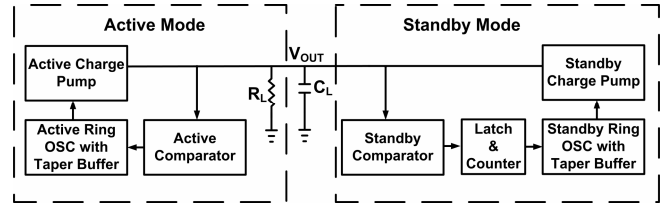


Fig. 1. Block diagram of the conventional wordline generating circuit [4].
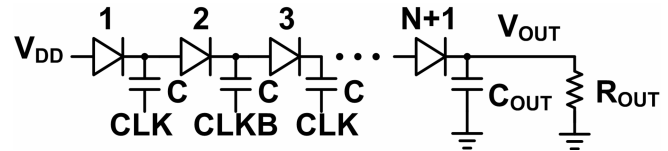


Fig. 2. Dickson charge pump circuit with a resistive load [6].

Since the active mode with resistive load needs longer response time to achieve steady state of the entire system, there are many analyses to discuss this issue [5]-[7]. In this paper, the wordline voltage generating circuit with low power in standby mode and short response time in active mode is proposed.

## II. CONVENTIONAL WORDLINE GENERATING CIRCUIT

Fig. 1 illustrates the block diagram of the conventional wordline generating circuit [4]. The resistive load ($R_L$) is only connected to the output in the active mode. Ideally, the active charge pump is designed to boost supply voltage to the specified output voltage ($V_{OUT}$), which may be above or below the limited range in real implementation due to process variation. Consequently, the charge pump regulator scheme is needed. In [4], it utilizes the comparator and the resistor divider to compare the divided $V_{OUT}$ with constant reference voltage. If the divided $V_{OUT}$ is greater than the constant reference voltage, the comparator stops the ring OSC (Oscillator). When the ring oscillator stops, the charge pump stops boosting too. Therefore, the $V_{OUT}$ is decreased and vice versa.

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To perform the low standby current, the voltage divider requires large resistors in standby mode. With the aforementioned charge pump regulator scheme, if the time that the ring oscillator stops is longer, the circuit has a lower standby current. The larger capacitor used in the standby charge pump results in the longer time ring oscillator takes to stop. Comparatively, the large capacitor also needs large taper buffer size to charge it. In [4], a latch and a counter are used in the standby mode. Variation of power supply voltage and temperature has great influence on the average standby current consumption. The taper buffer consumes the major portion of the average standby current, and it has the correlation with the counting number of the standby ring oscillator. Therefore, the conventional wordline generating circuit utilizes a latch and a counter to control the counting number to reach optimized standby current consumption.

To decrease the response time is an important issue in a power-up state. When the circuit has a short response time, short recovery time appears after the output voltage drops suddenly [5]. Fig. 2 shows the standard Dickson charge pump with a capacitive and a resistive load connected to the output. Two out-of-phase clock signals, CLK and CLKB, boost the capacitors (C) to raise the output voltage ($V_{OUT}$) to the specified high voltage. In [6] and [7], rise time $T_r$ can be derived as

1) *Without a resistive load:*

$$T_r = \frac{\ln\left(1-\dfrac{V_{OUT}-V_g}{V_g}\right)}{\ln\beta}\times T_{CLK} \tag{1}$$

$$\beta = \frac{1}{1+\dfrac{C}{NC_{Load}}} \tag{2}$$

where $V_g = V_{DD}-V_t$, $V_t$ is the threshold voltage, and $T_{CLK}$ is the cycle time of driving clock.

2) *With a resistive load:*

$$T_r = \frac{\ln\left(\dfrac{V_M-V_{OUT}}{V_M-V_{OUT}(0)}\right)}{\ln\beta}\times T_{CLK} \tag{3}$$

$$\beta = \frac{1-\dfrac{T_{CLK}}{R_L\times C_{Load}}}{1+\dfrac{C}{N\times C_{Load}}} \tag{4}$$

where $C_p = \left(C^{-1}+C_{OUT}^{-1}\right)^{-1}$,

$V_M = \dfrac{(N+1)\times V_g}{1+\dfrac{N}{C}\dfrac{T}{R_L}}$ and $R_L = \dfrac{R_{OUT}}{\left\{1-\dfrac{T_{CLK}}{8\times R_{OUT}}\left[C^{-1}-(C+C_{OUT})^{-1}\right]\right\}}$.

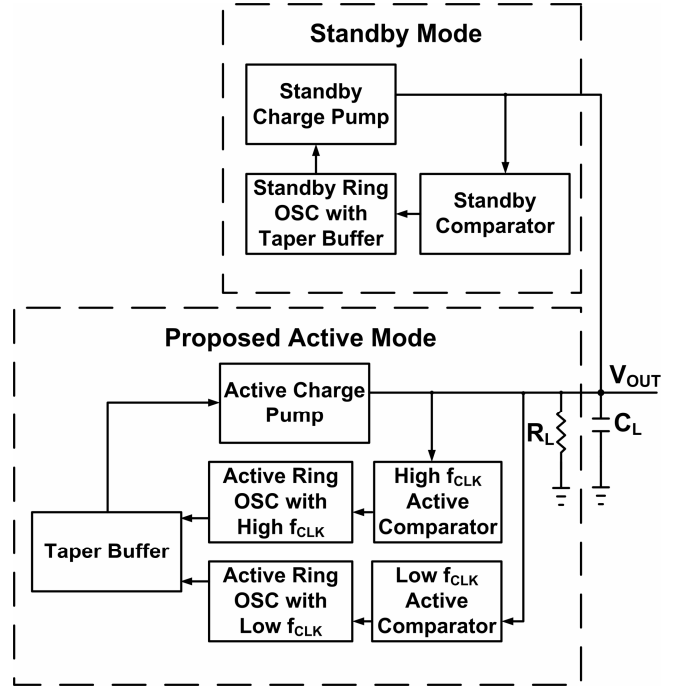In (2) and (4), $C_{Load} = C_{OUT} + C_{pump}$ and $C_{pump}$ is about NC/3.



Fig. 3. New proposed wrodline generating circuit.

## III. NEW PROPOSED WORDLINE GENERATING CIRCUIT

Fig. 3 shows the new proposed wordline generating circuit. In the active mode, the output has an additional resistive load ($R_L$), and it results in the finite load current. The increasing response time results from the finite load current. According to (1) and (3), a new active mode is proposed to reduce the response time. In the standby mode, a latch and a counter are left out.

In the active mode, two different ring oscillators with high clock frequency ($f_{CLK}$) 170MHz, and low clock frequency ($f_{CLK}$) 25MHz which is also the operating frequency of the entire circuit, are employed. Each of the two ring oscillators is controlled by different comparators. In the power-up state, the active ring oscillator with high $f_{CLK}$ is used to boost active charge pump first, so the output voltage would rise more quickly than conventional wordling generating circuit with a resistive load. Before the output voltage just reaches its steady state, the high $f_{CLK}$ active comparator stops high $f_{CLK}$ ring oscillator, but the low $f_{CLK}$ active comparator starts the low $f_{CLK}$ ring oscillator. After the transition between two ring oscillators, the active mode works in steady state with proper operating clock frequency 25MHz, thus it would not cause extra average current consumption. The higher clock frequency also means the smaller pumping period, and the larger current of the taper buffer is needed to boost charge pump to the specified high voltage. In other words, a large taper buffer size is inevitable. Under considerations of chip size and current consumption, the high clock frequency should not be chosen too high.
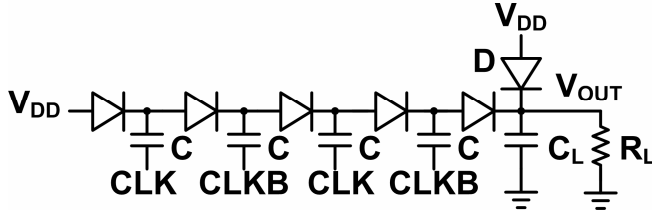
Fig. 4. Active charge pump with a diode (D) connected between $V_{DD}$ to $V_{OUT}$.

Fig. 4 shows the active charge pump with a diode (D) connected between $V_{DD}$ and $V_{OUT}$. When the power-up state begins, $V_{OUT}$ varies from 0V to the specified output voltage. At the beginning of operation, the diode (D) makes $V_{OUT}$ reach to $V_{DD}$-$V_t$ in advance ($V_t$ is about 0.5V), so it leaves out the time taking for $V_{OUT}$ from 0V to $V_{DD}$-$V_t$. When $V_{OUT}$ reaches to steady state output voltage (4.5V to 4.7V), the diode (D) is off without breakdown.

In the standby mode, the regulation is controlled by only the standby comparator. As mentioned before, Dickson charge pump has a finite standby current. The standby comparator decides the boosted voltage value, whether the standby ring oscillator works or not. The entire system takes the average current into account, thence the standby period which is composed of pumping and blocking period [5] should be as long as possible. Consequently, not only the capacitors used in standby charge pump should be suitable, but also the boosted voltage in the pumping period should be high enough to increase the standby period.

## IV. SIMULATION RESULTS

In order to evaluate and analyze the new proposed wrodline generating circuit compared with the conventional one, the circuit with four stage charge pump, a 100kΩ resistive load and a 2nF capacitive load is performed. The output voltage should be limited from 4.5V to 4.7V. A supply voltage ($V_{DD}$) is from 1.6V to 2V, the operating frequency works at 25MHz, the high clock frequency in the active mode is 170MHz, and the temperature varies from -40$^o$C to 85$^o$C. The simulation uses SPICE Model in a 0.18μm 1.8V/5V 1P4M Logic Process with Embedded Flash.

Fig. 5 shows the simulation results between the new proposed and conventional wordline generating circuit (WGC). The simulation conditions are $V_{DD}$ = 1.6V, $R_L$ = 100kΩ, operation clock frequency = 25MHz, temperature = 25$^o$C, and $V_{OUT}$ is not out of the specified range in steady state (4.5V to 4.7V). In this work, $R_L$ is large enough to bring relatively small load current, thus the response time between conventional WGC with or without $R_L$ is similar. Nonetheless, the response time is still too long for conventional WGC. In the new proposed WGC, the response time improves obviously, as shown in Fig. 5. The response time in the new proposed WGC with $R_L$ is about 1.86μs, and the response time is 4.34μs in the conventional WGC with the same $R_L$. The improvement is about 57.14%.
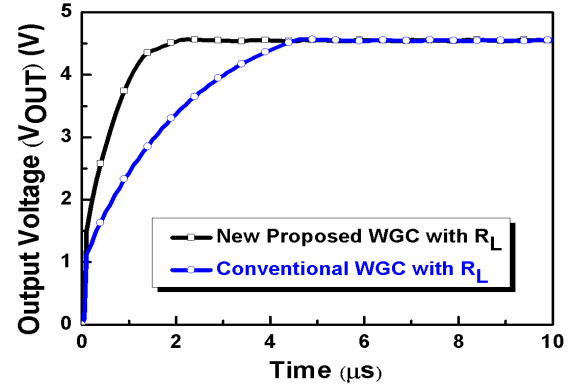


Fig. 5. Comparisons between the new proposed and conventional wordline generating circuit (WGC) in active mode with a resistive load ($R_L$).
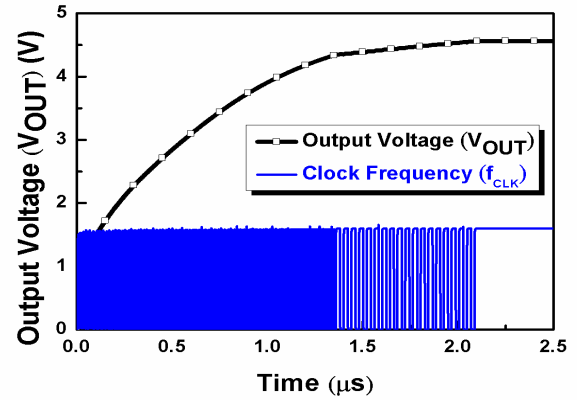


Fig. 6. Two different clock frequencies ($f_{CLK}$) in the active mode.

Fig.6 has the same condition with the new proposed WGC with $R_L$ in Fig. 5, but it illustrates two different clock frequencies in the active mode. The dense waveform in clock frequency ($f_{CLK}$) is high $f_{CLK}$ with 170MHz, and the rare waveform is low $f_{CLK}$ with operation clock frequency of 25MHz. At the beginning of the active mode, high $f_{CLK}$ executes. With high $f_{CLK}$ and the additional diode (D), the output voltage rises rapidly. After the high $f_{CLK}$ stops at the time of 1.4μs, the low $f_{CLK}$ starts to boost charge pump and the output voltage ($V_{OUT}$) rises smoothly. After the time of 2.2μs, $f_{CLK}$ holds with constant voltage level of $V_{DD}$, that is, both ring oscillators stop boosting output voltage because $V_{OUT}$ reaches to its steady state (4.5V to 4.7V).

In real applications, variation of supply voltage and temperature should be cogitated. Fig.7 shows the response time with difference supply voltage and temperature. At $V_{DD}$ = 1.6V, temperature of -40$^o$C, 25$^o$C, and 85$^o$C are simulated. Each of them compared with conventional WGC with $R_L$ has improvement of 57.14%, 40.45%, and 65.53%, respectively. At $V_{DD}$ = 2V, the new proposed WGC with $R_L$ has improvement of 62.3%, 59.86%, and 65.9% under the corresponding temperatures.
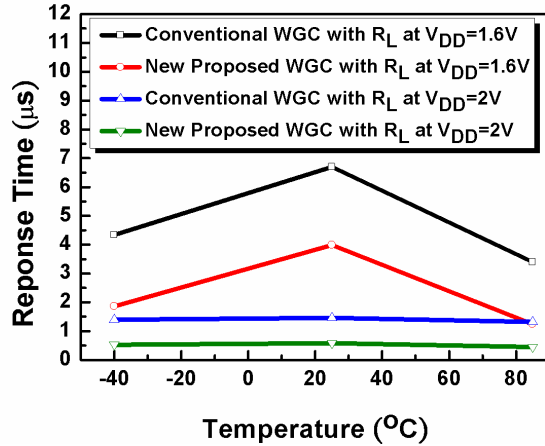
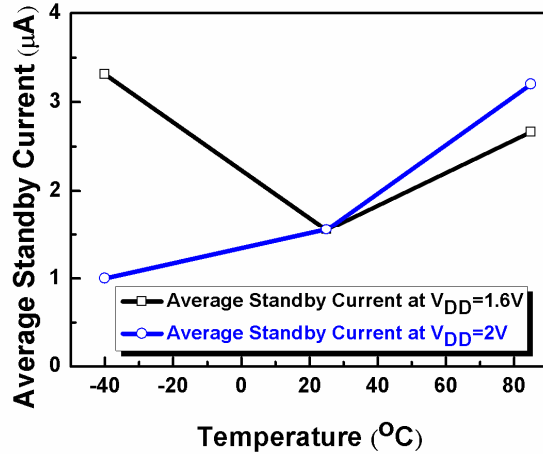Fig. 7. The response time between conventional and the new proposed WGC with $R_L$ at $V_{DD}$=1.6V and 2V.



Fig. 8. The average standby current at $V_{DD}$=1.6V and $V_{DD}$=2V.

The response time between $V_{DD}$ = 1.6V and 2V are quite different in Fig. 7. In the new proposed WGC, the ring oscillator is utilized to boost the charge pump, but the frequency of ring oscillator is excessively related with supply voltage. The higher supply voltage leads to higher clock frequency. In (1) and (3), the frequency has extreme influence on the response time.

In the new proposed WGC, only a comparator is used to regulate the standby mode. The standby comparator only consumes about 100 nA, and the standby charge pump consumes about few hundred nano amp. The current consumption of the standby charge pump is decided by the resistors used in the voltage divider. The current goes through the standby comparator, and the voltage divider is very small, thus the response time of standby comparator is longer than that of active comparator. It may result in the output voltage larger than 4.7V in the pumping period of the standby mode. For this reason, the resistor value of the voltage divider and the current consumption of comparator in standby mode are required to modify.

Fig. 8 shows the simulation results of average standby current consumption. Under considerations of variation of supply voltage and temperature, output voltage is successfully controlled in the range of 4.5V to 4.7V, and current consumption is below 3.3μA. At temperature of -40°C, the circuit operation with $V_{DD}$ of 1.6V and 2V have excessive different current consumption compared with others. The standby regulator is only composed of a comparator, hence the temperature variation has more influences than conventional WGC. As mentioned before, the standby period is as long as possible if the standby current demands to be smaller. The higher output voltage level in the pumping period brings about the longer blocking period. At $V_{DD}$ = 1.6V and temperature = -40°C, the standby comparator has worse performance, so the boosted voltage in the pumping period is lower than others. Therefore, the standby period is also smaller to increase the average standby current consumption.

## V. CONCLUSION

A new wordline voltage generating circuit with high speed active mode and low power standby mode is proposed. The circuit has been simulated in a 0.18μm 1.8V/5V 1P4M Logic Process with Embedded Flash. In active mode, the response time has been improved from 40.45% to 65.9% in different supply voltages and temperatures. In standby mode, average standby current is from 1.56μA to 3.3μA under variations of supply voltages and temperatures. The experimental chip to verify this design is now under wafer fabrication. The measured results will be shown in the presentation.

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