# CMOS Power Amplifier with ESD Protection Design Merged in Matching Network

Yu-Da Shiu[1], Bo-Shih Huang[1], and Ming-Dou Ker[2]
[1]SoC Technology Center, Industrial Technology Research Institute, Hsinchu, Taiwan.
[2]Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
Email: {ydshiu, huangboshi}@itri.org.tw and mdker@ieee.org

***Abstract*—A power amplifier (PA) with combination of ESD protection circuit and matching network into single block was proposed and implemented in a 0.18-μm CMOS process. By comprising ESD protection function into the matching network, this design omits individual I/O ESD clamps to alleviate loading that degrades RF performances. According to the experimental results, the ESD protection circuit with LC configuration contributes a 3.0-kV human body model (HBM) ESD robustness without significant degradation on RF performances of the PA for 2.4-GHz RF applications.**

## I. Introduction

Wireless communication turns out to be one of the most rapidly emerging technologies in recent decades of years. There have been numerous wireless applications in many fields such as transportation, medicine, and amusement. Power amplifier (PA) plays an important position in wireless transceiver to transmit RF signal with adequate power. Delivering large power via air to another receiver, PA ranks the most power-hungry block in transceiver.

The developed IC products tend toward final targets of high integration, low cost, and high reliability in commercial markets. RF ICs are approaching the final targets as well. CMOS processes provide important supports to implement a CMOS PA into system on chip (SoC). Electrostatic discharge (ESD) issues have come out with down scaled transistor size in advanced CMOS processes. Thus, ESD robustness has been taken into a main reliability consideration for high production yield. In RF IC, ESD protection continues to be a challenge because RF performances are sensitive to parasitic effects of ESD protection devices. ESD protection designs for RF ICs are in two classifications, ESD devices with low parasitic effect or new circuit techniques. One of suitable devices widely applied in RF ICs is diode [1]. Diode induces low parasitic capacitance and has low cut-in voltage, which are advantages for RF performance and ESD protection, respectively. Silicon-controlled rectifier (SCR) can sustain high ESD current with low parasitic capacitance, too [2]. In addition, I/O ESD clamps with π-match, broadband-architecture, and inductance-resonance techniques have been proposed as ESD protection for RF ICs [3]-[5]. With proper I/O ESD clamps of low parasitic effects, the challenge of ESD protection for RF ICs could be solved.

However, ESD protection design for CMOS PA still lacks further study. Published ESD protection designs were almost for RF receiver such as low-noise amplifier (LNA). There could be more challenge in ESD protection for PA compared to LNA. Diode is no longer suitable as in I/O ESD clamp for PA because the low cut-in voltage could cause improper turn-on by large-power signal of PA. SCR could result in latch-up danger due to unexpected trigger by PA signal. Most of ESD protection designs for LNA cannot work if applied in PA. Therefore, a CMOS PA with ESD protection was designed in this work.

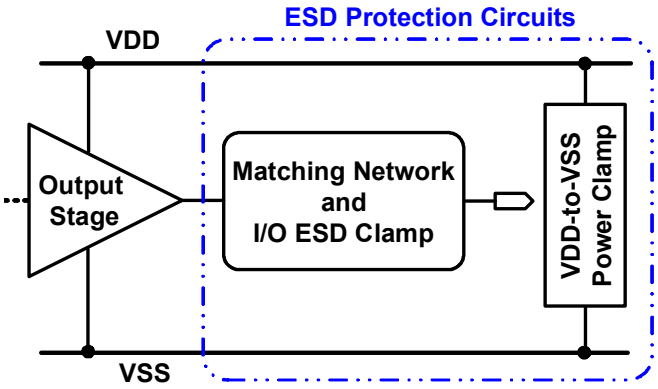


Figure 1. Block diagram of PA with ESD protection.

Figure 1 shows a brief block diagram of PA. The matching network is well-known for delivery of RF power. In order to merge ESD protection and impedance matching, the matching network is implemented as a specified LC configuration that can also be utilized as an I/O ESD clamp. This circuit technique omits traditional ESD devices, such as diodes and SCRs, in the I/O ESD clamp. This design is

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particularly suitable for RF front-end circuits including PA. Improper turn-on or latch-up events never happen in this I/O ESD clamp.

## II. ESD Protection Design Merged in Matching Network

To implement proper ESD protection circuit for PA, ESD weakness on PAs was investigated. An example of PA stage is illustrated in Figure 2. The drain and gate of transistor M1 are most likely failure points caused by ESD stresses because of low breakdown voltages below 10 V. While there are ESD stresses between the drain and VSS, the p-n junction between p substrate and n diffusion is damaged due to reverse breakdown with large discharge current. The gate is damaged as well due to oxide breakdown while there are ESD stresses between Vin and VSS. To avoid ESD failure on the drain, an on-chip shunt inductor can be placed between node Vout and VSS. The metal of inductor must be wide enough to conduct large current. While ESD events happen, the inductor works like short circuit and draw out ESD current. Besides, there exists a parasitic resistance in the inductor. When the inductor conducts ESD current, the equivalent series resistor of inductor causes a overshooting voltage $V_{ESD}$ at the pad. Even if the resistance is small, a large ESD current could cause a $V_{ESD}$ that is higher than the drain or gate breakdown voltage. The breakdown issue can be alleviated with MIM capacitors. MIM capacitor has high dielectric strength indicating high breakdown voltage, over 30 V in a given 0.18-µm CMOS process. A series MIM capacitor that blocks direct connection between the drain and inductor can prevent the drain from breakdown while a higher $V_{ESD}$ is induced by ESD current conducting via the inductor.

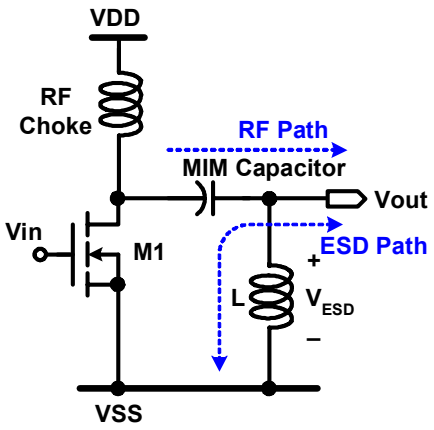



Figure 2. PA stage with a series capacitor and an on-chip inductor for ESD protection.

Matching networks can be realized with capacitors or inductors in series or shunt configurations. The configuration of a series capacitor and a shunt inductor is preferred with ESD protection consideration. Input and output matching networks of PA should be well designed with proper capacitances and inductances for impedance transformation, respectively.

## III. Implementation of PA with ESD Protection

A 2.4-GHz PA with ESD protection design was implemented in a 0.18-µm CMOS process. The circuit realization is shown in Figure 3. Transistor M1 operates as a class-A amplifier with a proper gate bias for higher linearity. The dimension of M1 was designed with main considerations of output power, power added efficiency (PAE), and process limitation on power consumption. An off-chip inductor RFC works as an RF choke of the gain stage. The matching networks comprise C1, L1, C2, and L2 for the input and output of PA, respectively. MIM capacitors were employed to realize C1 and C2 for higher breakdown voltage, higher capacitance precision, and lower parasitic effect. L1 and L2 were implemented with on-chip spiral inductors. The matching-network design combines both functions of impedance matching and ESD protection. Impedance matching requires proper capacitances and inductances. ESD protection requires sufficiently high breakdown voltage of the capacitors to protect M1 drain/gate and wide metal of the spiral inductors to draw out large ESD current. VDD-to-VSS power clamp, as shown in Figure 4, provides a path that can sustain ESD current up to amperes. The power clamp consists of an ESD detection circuit and a current-conducting transistor Mn2 [6]. Detecting an ESD stress, the ESD-detection circuit immediately outputs a trigger signal to the gate of Mn2, and then Mn2 turns on to conduct ESD current. A well-designed power clamp must turn on in time to protect PA circuit against ESD stresses.

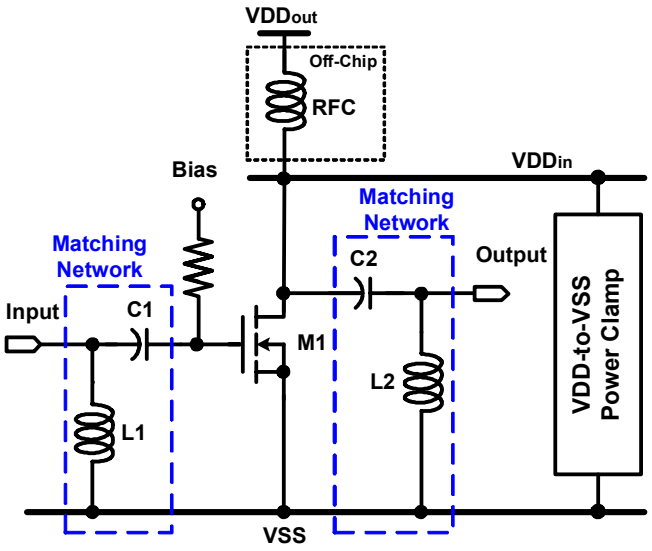



Figure 3. Realization of PA with ESD protection .

In this PA design, the matching networks contribute ESD protection functions without additional I/O ESD clamps, leading to less performance degradation of the PA circuit.

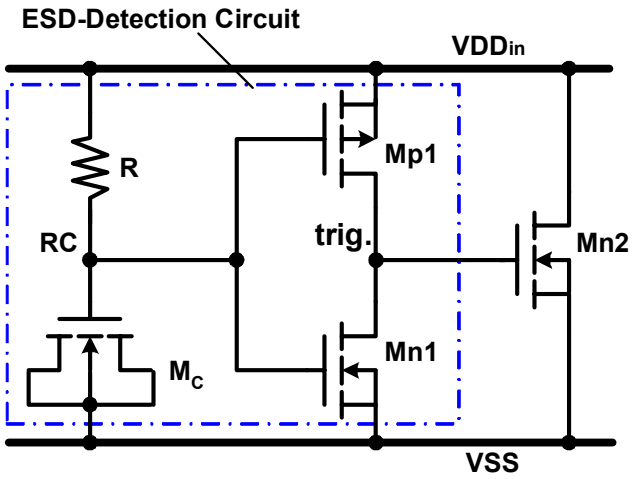
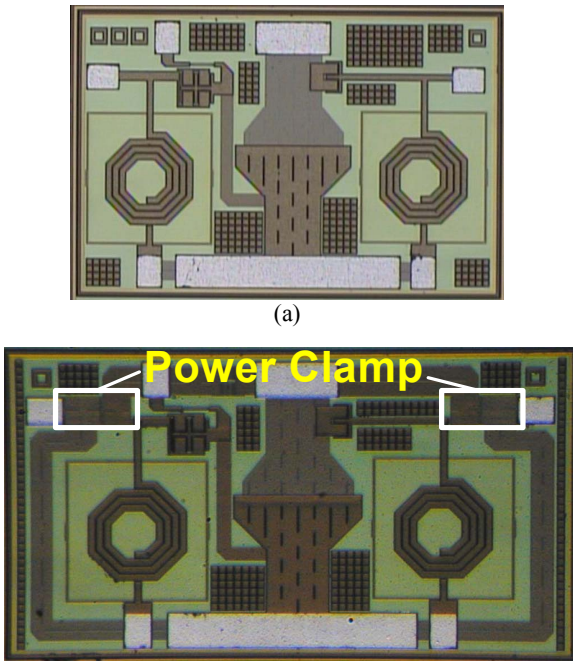



Figure 4. VDD-to-VSS power clamp.

## IV. Experiental Results

Two kinds of PA chips, without and with ESD protection, were fabricated in a standard 0.18-μm 1P6M CMOS process. The photographs of fabricated chips are shown in Figure 5.



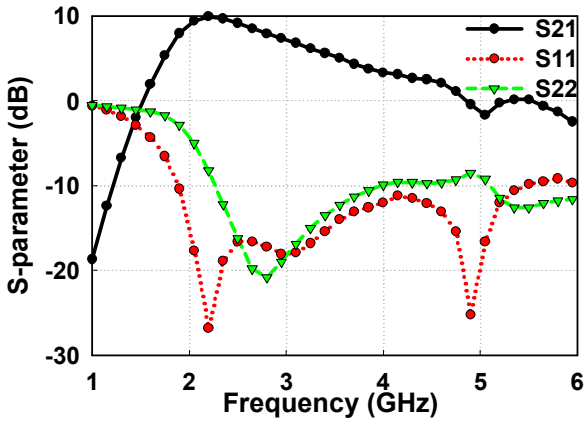

(a)

(b)

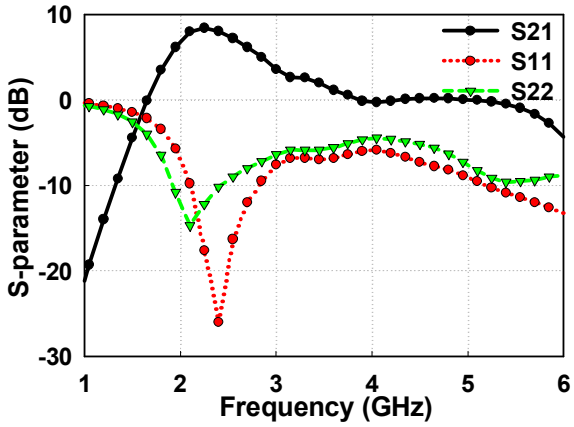
Figure 5. Chip photographs of the PAs (a) without, and (b) with, ESD protection circuits.

In RF measurement, the chips were measured on board with bond-wire connection. Network Analyzer, Signal Generator, and Spectrum Analyzer were utilized to verify the PA performances. The PAs without and with ESD protection both operate under 1.8-V power supply and consume 106-mA DC current. As two S21 curves shown in Figure 6, the gains of PAs without and with ESD protection are 9.3 dB and 8 dB, respectively. The input and output return losses, S11 and S22, of PAs without and with ESD protection are less than −10 dB in 2.4-GHz ISM band. The relations of output power and PAE to input power are shown in Figure 7. The output powers at 1-dB compression points of PA with/without ESD protection are 17.3 dBm with 34% PAE and 15.6 dBm with 20% PAE, respectively. A comparison of measured results between the PAs without and with ESD protection is summarized in TABLE I.

To verify ESD robustness of PA with the proposed ESD protection, the chips were zapped by an ESD simulator that generates standard human-body-model (HBM) pulses [7]. ESD voltage was applied to I/O pin with test combinations of positive-to-VSS (PS-mode), positive-to-VDD (PD-mode), negative-to-VSS (NS-mode), and negative-to-VDD (ND-mode) ESD stresses. The chips were also tested by positive and negative VDD-to-VSS ESD stresses. As shown in TABLE II, the HBM level of PA with the proposed ESD protection achieves at least 3.0 kV that satisfies general ESD specifications (2.0 kV) for commercial ICs.

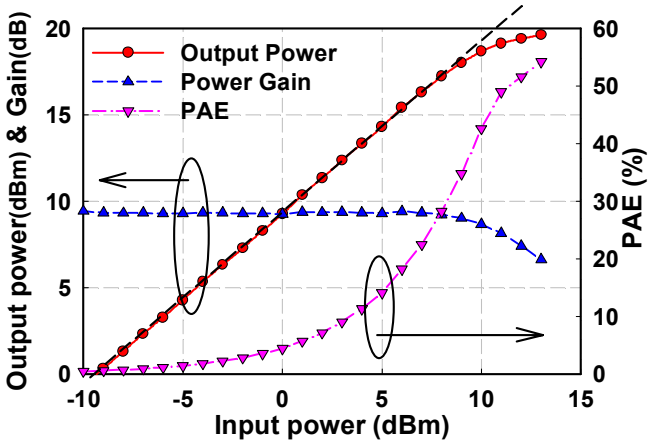



(a)

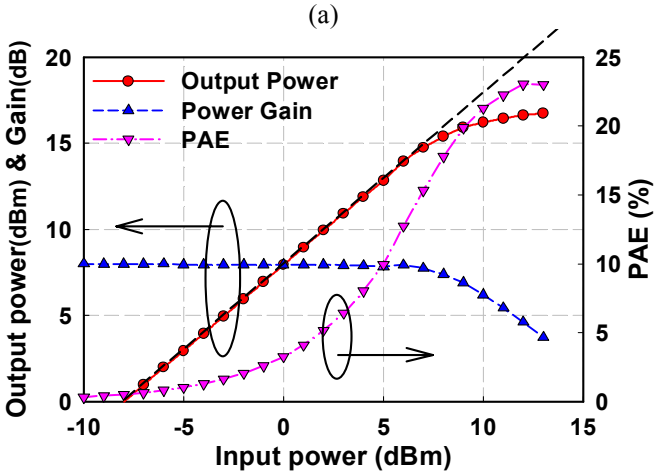



(b)

Figure 6. Measured S-parameters of the PAs (a) without, and (b) with, ESD protection circuits.




(a)




(b)

Figure 7. Measured output power, power gain, and PAE of the PAs (a) without, and (b) with, ESD protection circuits.

TABLE I. COMPARISON OF RF PERFORMANCES BETWEEN THE PAS WITHOUT OR WITH ESD PROTECTION CIRCUIT

| PA Features | Without ESD Protection | With ESD Protection |
|---|---|---|
| Operating Freq. (GHz) | 2.4 | 2.4 |
| Supply Voltage (V) | 1.8 | 1.8 |
| DC Current (mA) | 106 | 106 |
| Gain (dB) | 9.3 | 8.0 |
| Input Return Loss (dB) | 17.1 | 19.5 |
| Output Return Loss (dB) | 14.9 | 10.6 |
| Output Power (dBm @P1dB) | 17.3 | 15.6 |
| PAE (%) | 34 | 20 |
| Die Size ($\mu m^2$) | 1000 x 750 | 1200 x 750 |

TABLE II. HBM ESD ROBUSTNESS OF THE PA WITH ESD PROTECTION CIRCUIT

| HBM (kV) | PS | PD | NS | ND | VDD-to-VSS(+) | VDD-to-VSS(–) |
|---|---|---|---|---|---|---|
| Input Pin | >8.0 | >8.0 | >8.0 | 3.0 | 3.0 | >8.0 |
| Output Pin | >8.0 | >8.0 | >8.0 | 3.0 | | |

## V. CONCLUSIONS

A PA with ESD protection circuit in a 0.18-µm CMOS process has been designed, fabricated, and successfully verified. The combination of matching networks with ESD protection solution benefits not only RF performance but also ESD robustness. From the experimental results, the proposed ESD protection design on the PA provides high HBM ESD robustness of over 3.0 kV without significant degradation on RF performance. The ESD protection design merged into the matching network is a simple and effective solution of ESD protection for RF PA.

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