ESD Protection Structure with Embedded High-Voltage P-Type SCR for Automotive Vacuum-Fluorescent-Display (VFD) Applications

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Abstract –A new ESD protection structure of HVPSCR embedded into the high-voltage PMOS device is proposed to greatly improve ESD robustness of the vacuum-fluorescent-display (VFD) driver IC for automotive electronics applications. By only adding the additional N+ diffusion into the drain region of HVPMOS, the It2 of output cell has been greatly improved form 0.07A to be greater than 6A within the almost same layout area. Such an ESD-enhanced VFD driver IC has been in mass production for automotive applications in car to sustain HBM ESD stress of up to 8kV.

1. Introduction

High-voltage transistors in smart-power technology are widely used for display driver ICs, power supplies, power management, and automotive electronics. In smart-power technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, and bipolar junction transistors have been used as ESD protection devices [1]-[7]. For these applications, the high-voltage MOSFET was often used as the common ESD device in the high-voltage CMOS ICs, because it can work as both of output driver and ESD protection device simultaneously. However, the ESD robustness of such high-voltage MOSFET is quite weaker than that of the low-voltage MOSFET in CMOS technologies. Hence, ESD reliability has been an important issue for such high-voltage IC products.

In some specific application, such as the driver IC for vacuum fluorescent display (VFD) [8] in automotive instrumentation [9], only high-voltage PMOS (HVPMOS) is provided in a specific CMOS process which is modified from the low-cost low-voltage CMOS process. By adding few additional masks and process steps, only high-voltage PMOS is provided with the low-voltage NMOS and PMOS to design the VFD driver IC. To reduce the fabrication cost, no high-voltage NMOS is used in such specific VFD driver IC. For safety concerns in automotive electronics, the ESD robustness was often requested much higher than that of consumer electronics products. Thus, an additional protection device is necessary in the high-voltage I/O pin to sustain a high enough ESD robustness of the VFD driver IC for safe automotive applications.

In this work, a new ESD protection structure with the embedded high-voltage p-type SCR (HVPSCR) into the high-voltage PMOS device is proposed. Only an additional N+ diffusion is added into the HVPMOS to form the HVPSCR for ESD protection. The HVPSCR device structure can greatly improve HBM ESD robustness up to 8kV of the VFD driver IC in the specific 0.5-μm high-voltage CMOS process for automotive electronics applications.

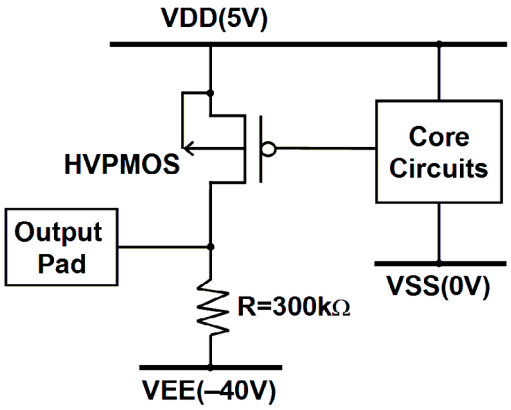


Fig. 1. The original output cell of the automotive VFD driver IC realized with the high-voltage PMOS (HVPMOS) and the pull-down resistor.

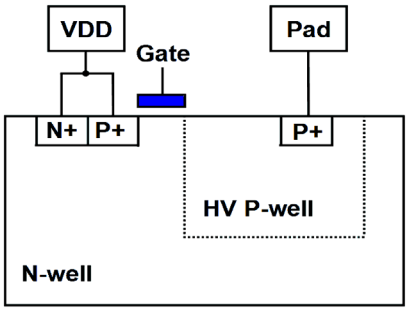
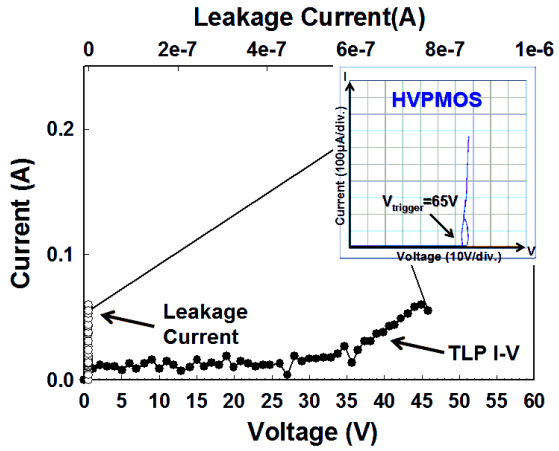


Fig. 2. The device structure of HVPMOS in the specific CMOS process. A HV P-well is used to surround the drain of HVPMOS to meet the HV application.

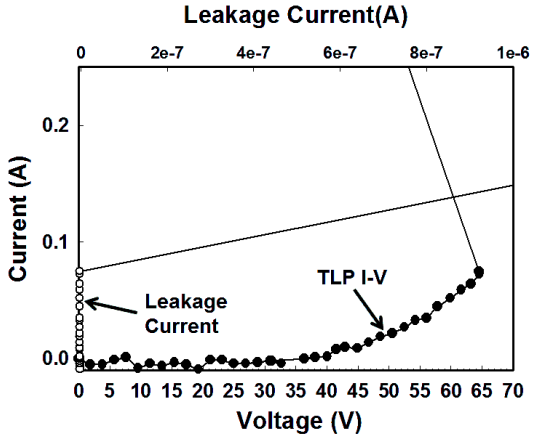
2. Original Design of VFD I/O

The high-voltage output cell of the automotive VFD driver IC fabricated in a 0.5-µm high-voltage CMOS process is shown in Fig. 1. In this VFD driver IC, the output pull-up function is realized by the high-voltage PMOS (HVPMOS), whereas the pull-down function is realized by the on-chip resistor of 300 kohm for vacuum fluorescent display. The resistor is connected from the output pad to VEE of -40V for VFD applications.

The device structure of the HVPMOS is drawn in Fig. 2, where the high-voltage region is surrounded by the high-voltage (HV) P-well of lightly doped concentration with a specified clearance from the HV P-well edge to the drain P+ diffusion of the HVPMOS. Such a HV P-well with lightly doped concentration will provide the drain of HVPMOS with high enough breakdown voltage for VFD application. The breakdown voltage of the HVPMOS is specified to be higher than 45V for this VFD application.



(a)



(b)

Fig. 3. (a) The TLP-measured I-V curve of HVPMOS with 600µm in width and 2µm in length. The DC I-V curve of HVPMOS in low-current region is also shown in the inset figure, which has a DC breakdown voltage of 65V. (b) The TLP-measured I-V curve of HVPMOS with 800µm in width and 2µm in length.

The TLP-measured I-V curve of the HVPMOS with 600µm in width and 2µm in length is shown in Fig. 3(a), whereas the DC I-V curve in low-current region is shown in the inset figure of Fig. 3(a). The DC breakdown voltage of this HVPMOS is ~ 65V. But, the trigger voltage (Vt1) in the TLP-measured I-V curve of HVPMOS is ~35V. Due to the inefficient parasitic p-n-p bipolar action in the HVPMOS, no obvious snapback characteristic is found. Therefore, the holding voltage of HVPMOS is larger than the trigger voltage of 35V, and the secondary breakdown current (It2) of the HVPMOS with 600µm in width and 2µm in length is only 0.07A. Moreover, the TLP-measured I-V curve of the HVPMOS with 800µm in width and 2µm in length is shown in Fig. 3(b), where the It2 is only 0.08A. The difference on the trigger voltages of HVPMOS measured by DC and TLP is caused by transient-coupling effect. The TLP is designed with a rise time of 10ns to simulate the HBM ESD event. The zapping dV/dt transient voltage at the drain could be coupled into the device through the parasitic capacitance in the drain/bulk junction to lower the trigger voltage.

The HBM ESD levels and It2 among the HVPMOS with the different device widths (but keeping the same length) are listed in Table I. With such a lower It2, the HBM ESD levels of such output cell with the HVPMOS are about ~500V under the negative-to-VDD (ND-mode) ESD stress. The failure analysis (FA) picture of this output cell on the HVPMOS with 600µm in width after HBM 1-kV ESD stress is shown in Fig. 4, where serious contact spiking from drain to source of the HVPMOS is found.

Table I. HBM ESD level and TLP_It2 of HVPMOS with different device widths.

HVPMOS Device Widths	500µm	600µm	800µm
HBM ESD Level Under ND-mode ESD Stress	500V	500V	500V
TLP_It2	0.04A	0.07A	0.08A

Fig. 4. The SEM failure picture on the output HVPMOS with device width of 600µm in the VFD driver IC after 1-kV negative-to-VDD HBM ESD stress.

3. New ESD Design for VFD I/O

A new ESD protection structure with the high-voltage p-type SCR (HVPSCR) embedded into the output HVPMOS is proposed to greatly improve ESD robustness of the automotive VFD driver IC. The output cell with the embedded HVPSCR for automotive VFD drive IC is shown in Fig. 5. With the help of power-rail ESD clamp circuit [10], the positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses [11], [12] on the output pin can be discharged through HVPSCR to VSS or VDD with the cooperation of power-rail ESD clamp circuit.

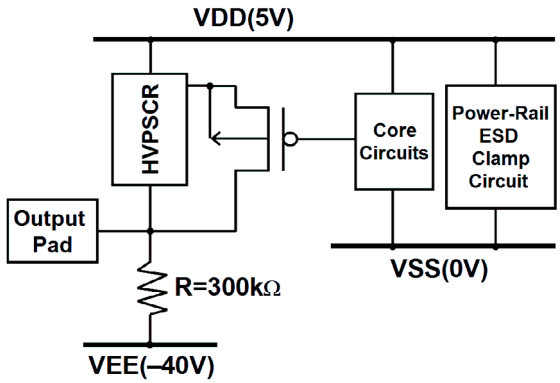


Fig. 5. The proposed ESD protection design with the high-voltage p-type SCR (HVPSCR) embedded into the output HVPMOS to improve ESD robustness of output cell of the automotive VFD driver IC.

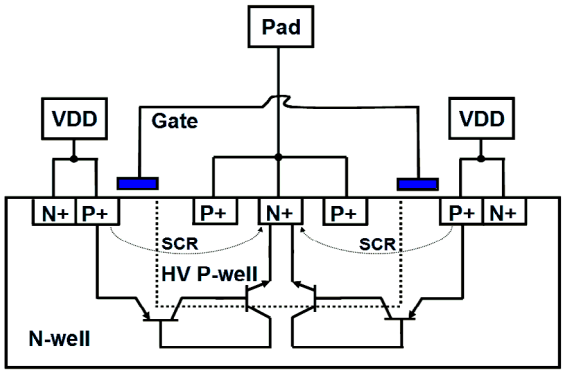


Fig. 6. The device structure of the HVPSCR embedded into the output HVPMOS.

The device structure of the HVPSCR embedded into the output HVPMOS is drawn in Fig. 6, where an additional N+ diffusion is inserted into the drain region of the HVPMOS. The SCR path of the HVPSCR from VDD to the output pad is composed by P+ diffusion (source of HVPMOS), N-well, HV P-well (drain of HVPMOS), and N+ diffusion in HV P-well in Fig. 6. The trigger voltage of the HVPSCR is determined by the doping concentration of the N-well and HV P-well. Hence, the trigger voltage will be higher than that of the typical SCR in the 0.5-μm CMOS process. On the other hand, the path from the output pad to VDD is through the parasitic diode in the HVPMOS. The parasitic diode is composed of HV P-well and N-well. Hence, for both ND-mode and PD-mode ESD-stress conditions, the automotive VFD output cell will have a good ESD robustness due to the low holding voltage of the HVPSCR and the forward-biased parasitic diode in the HVPMOS, respectively.

Here, only an additional N+ diffusion is added into the HVPMOS to form the HVPSCR for ESD protection. So, only a little increase of occupied silicon area is used to realize this HVPSCR. The final die size of the VFD driver IC with the proposed HVPSCR for ESD protection is still kept the same.

The TLP-measured I-V curve of the HVPSCR with 600μm in width and 2μm in length is shown in Fig. 7, whereas the DC I-V curve of the HVPSCR is shown in the inset figure of Fig. 7. The DC trigger voltage of HVPSCR is ~ 65V, which is the same as that of the HVPMOS. Before the SCR path is triggered on, the I-V curve behavior of HVPSCR is the same as that of the HVPMOS. When the current is larger than ~ 5mA, the embedded HVPSCR will be triggered on with a holding voltage of 5V. Moreover, for VFD output driver IC, the maximum operation current flow across the pull-down resistor between the output pad and the VEE power pad is 0.15mA. This current is obtained from the maximum voltage drop which is 45V (between VDD and VEE) divided by 300kohm when the pull-up HVPMOS is turned on. The current of 0.15mA is less than the trigger voltage of the HVPSCR. Hence, under normal operation condition, the HVPSCR in the VFD output driver IC is free to the latchup or latchup-like problem.

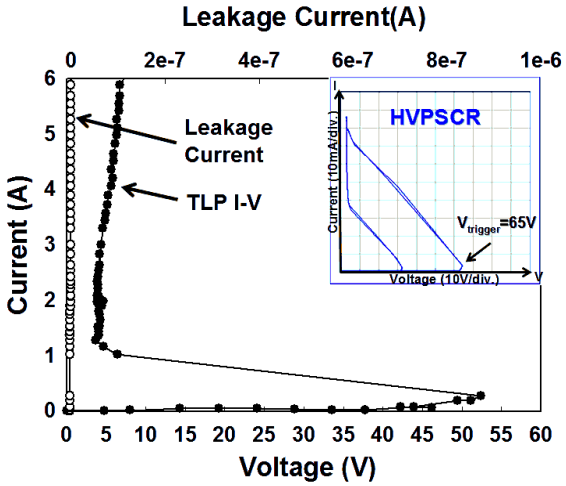


Fig. 7. The TLP-measured I-V curve of the HVPSCR. The DC I-V curve of the HVPSCR is shown in the inset figure, which has a DC breakdown voltage of 65V and a holding voltage of 5V.

The trigger voltage of the HVPSCR in the TLP-measured I-V curve is about ~53V, and the trigger current is about

0.3A, as shown in Fig. 7.The HVPMOS will be triggered on in the TLP measurement while the applied voltage is higher than 35V. As the TLP current is higher than 0.3A, the HVPSCR is triggered on. Moreover, the holding voltage of the HVPSCR is around 5V, which is much lower than that of the HVPMOS. According to the power dissipation of P=I×V, where I indicates the ESD discharge current and V indicates the holding voltage of the device, the device with the lower holding voltage during ESD stress can sustain a higher ESD level. The TLP-measured It2 of HVPSCR is greater than 6A which is much higher than that of HVPMOS. So, the HVPSCR can indeed sustain a much higher ESD level than the HVPMOS in the output cell of VFD driver IC.

The HBM ESD levels and It2 of the HVPSCR with different device widths (but keeping the same length) are shown in Table II. The It2 of the HVPSCR with different device widths are over 6A, and the HBM ESD levels can pass over 8kV under ND-mode ESD stress.

Table II. HBM ESD level and TLP_It2 of HVPSCR with different device widths.

Device Width (HVPSCR+HVPMOS)	500μm	600μm	800μm
HBM ESD Level Under ND-mode ESD Stress	>8kV	>8kV	>8kV
TLP_It2	>6A*	>6A*	>6A*

*Limitation due to the maximum output current of TLP equipment.

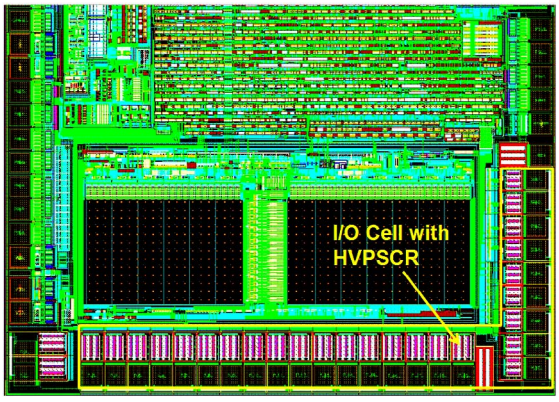


Fig. 8. The partial layout view of the VFD driver IC with the HVPSCR in I/O cell, which can sustain HBM ESD stress of up to 8kV.

With both the new proposed HVPSCR embedded into the HVPMOS and the power-rail ESD clamp circuit, the HBM ESD robustness of the output cell in automotive VFD driver IC has been successfully improved from 500V up to 8kV within almost the same layout area. The partial layout view of this VFD driver IC with HVPSCR in I/O cell is shown in Fig. 8, which can fully meet the ESD specification of automotive applications. Such an ESD-enhanced driver IC has been in mass production for the VFD applications in car.

4. Conclusion

The HVPMOS is not suitable for ESD protection in VFD driver IC for automotive electronics applications due to very poor ESD level. To greatly improve ESD robustness, a new ESD protection structure of the HVPSCR embedded into the HVPMOS is proposed by only adding an additional N+ diffusion into the drain region of HVPMOS. Within almost the same layout area, the It2 of the output cell has been improved to be over 6A. Moreover, the HBM ESD level of such VDF driver IC with HVPSCR can sustain up to 8kV.

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