Correlation between Transmission-Line-Pulsing I-V Curve and Human-Body-Model ESD Level on Low Temperature Poly-Si TFT Devices

Ming-Dou Ker[1], Chun-Lin Hou[2], Chih-Yih Chang[2], and Fang-Tsun Chu[3]

[1] Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics
National Chiao-Tung University, Hsinchu, Taiwan. Email: *mdker@ieee.org*

[2] ESD and Product Engineering Department, System-on-Chip Technology Center
Industrial Technology Research Institute, Hsinchu, Taiwan.

[3] Electronics Research and Service Organization, Industrial Technology Research Institute, Hsinchu, Taiwan.

Abstract -- The relations between human-body-model (HBM) electrostatic discharge (ESD) waveform and transmission line pulsing (TLP) I-V curve on low temperature poly-Si (LTPS) thin film transistor (TFT) have been investigated in this paper. By using ESD zapper and TLP system, the ESD waveforms and TLP I-V curves on the LPTS TFT devices under different device dimensions have been measured. From the experimental results, the turn-on resistances of TFT devices during HBM zapping and TLP stress are almost the same. Such experimental results have shown a good correction between HBM ESD level and TLP measurement on LTPS TFT devices.

1. Introduction

Low temperature poly-Si (LTPS) thin film transistor (TFT) employing excimer laser annealing (ELA) has been a promising technology for integrating driver circuits of active matrix liquid crystal display (AMLCD) due to the high mobility and low thermal budget. Moreover, due to the presence of a glass insulating layer, electrostatic discharge (ESD) becomes a critical issue in LTPS TFTs more than in CMOS devices. The related standards of human body model (HBM) testing has been defined by electrostatic discharge association (ESDA) and electronic industries alliance/joint electron device engineering council (EIA/JEDEC) [1], [2].

In the silicon-based CMOS and amorphous silicon thin film transistor technologies, the relations between the human-body-model (HBM) ESD testing and the transmission-line-pulsing (TLP) measurement had been investigated [3], [4]. However, the related research about the ESD current waveform on a LTPS TFT device is seldom proposed. The purpose of this work is to analyze the characteristics of ESD current waveform on LTPS TFT device under HBM zapping. Furthermore, in order to gain more information about the ESD behaviours of LTPS TFTs from the TLP characterizations, the correction between HBM ESD testing and TLP measurement is first built up in this paper.

2. Device Fabrication and Measurement Setup

Top-gate, n-channel LTPS TFTs were fabricated on the glass substrate, as shown in Fig. 1. Firstly, TEOS buffer oxide and a 500Å thick amorphous Si film were deposited on the glass substrate by PECVD. The laser crystallization was carried out by the XeCl excimer laser. The 1000Å PE-TEOS oxide was deposited after the active islands were patterned. Subsequently, the source/drain region was formed by the ion shower technology, followed the activation and gate electrode was patterned. After interlayer was deposited, contact opening and metallization were performed to complete the fabrication of the LTPS TFTs.

The HBM ESD robustness of LTPS TFT was evaluated by using a manual ESD tester ETS-910. The equipment setup for measuring the ESD current waveform on TFT devices is shown in Fig. 2. The ESD current waveform would be affected by the parasitic effect of measurement system [5]. In order to get a correct current waveform on LTPS TFT device, it was performed by minimizing the parasitic effects from device under test (DUT) to current probe CT-1 [6]. It has been certified that the current waveform of this measurement system meets the waveform specification of JESD22-A114-B standard.

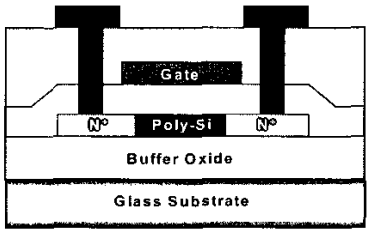


Fig. 1 The schematic structure of the investigated top-gate LTPS TFT device.

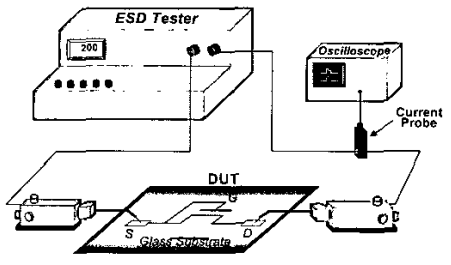


Fig. 2 The equipment setup for measuring the ESD current waveforms on TFT devices.

3. HBM ESD Waveform on LTPS TFT

In order to analyze the characteristics of ESD current waveform on LTPS TFT device, the HBM discharging waveform from the manual ESD tester ETS-910 was recored and studied. The ESD current waveform of a 100-V HBM ESD stress on a LTPS TFT device is shown in Fig. 3. The rise time was defined as the time between 10% and 90% of the leading edge of the current waveform. The decay time was defined as the time between the peak current and 36.8% of peak current along the trailing edge of the pulse. The dependence of HBM ESD peak current on the channel width of TFT device under 100-V HBM ESD stress is shown in Fig. 4, where the channel length of LTPS TFT device is kept at 8 μm. The peak current of HBM ESD waveform is increased while the device channel width is increased, because the turn-on resistance is reduced with the increase of device channel width.

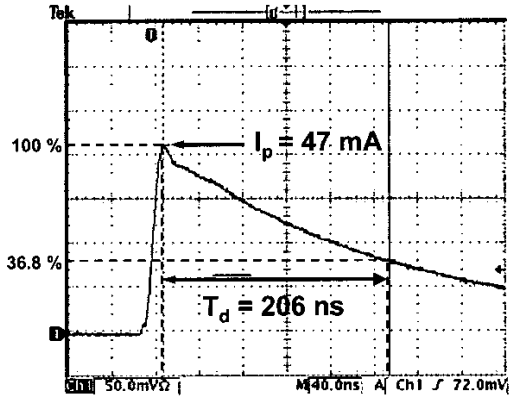


Fig. 3 The HBM ESD current waveform through a TFT device (W/L = 50μm/8μm) under HBM 100-V zapping.

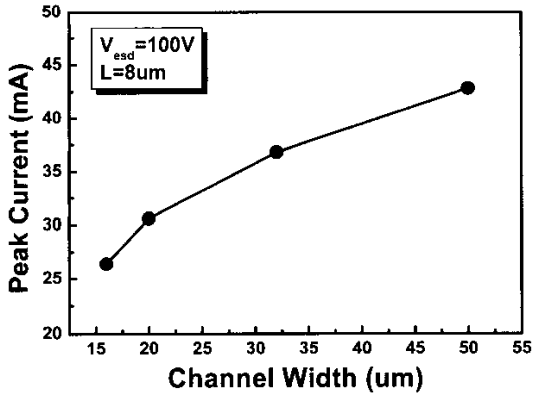


Fig. 4 The dependence of HBM ESD peak current on the channel width of TFT device under 100-V HBM ESD stress.

The dependence of ESD peak current on the HBM ESD voltage of TFT device with a fixed device dimension (W/L = 50μm/8μm) is shown in Fig. 5. It is found that the peak current is increased linearly with the increase of HBM ESD zapping voltage. Therefore, the device turn-on resistance (R_{HBM}) under HBM ESD stress can be calculated by

$$V_{ESD} \approx I_{ESD} \times (1.5k\Omega + R_{HBM}), \quad (1)$$

where V_{ESD} is defined as the ESD zapping voltage. I_{ESD} is the peak current through a TFT device under HBM ESD zapping. R_{HBM} is defined as the device turn-on resistance of the LTPS TFT under HBM ESD zapping. The equivalent resistance of human body is 1.5 kΩ. In Fig. 5, the turn-on resistances of the LTPS TFT (W/L=50μm/8μm) under different HBM ESD zapping voltages are almost kept as a constant.

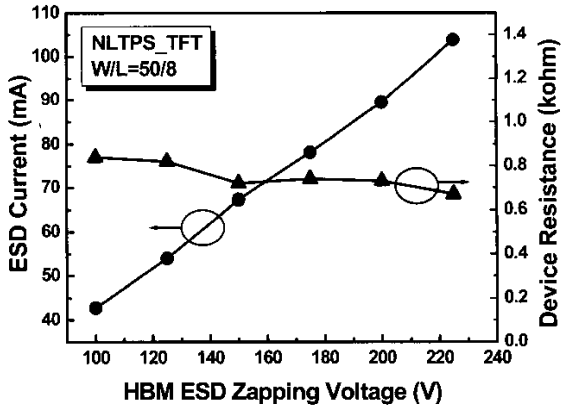


Fig. 5 The dependence of ESD peak current on the HBM ESD zapping voltage of a TFT device with a fixed device dimension (W/L = 50μm/8μm).

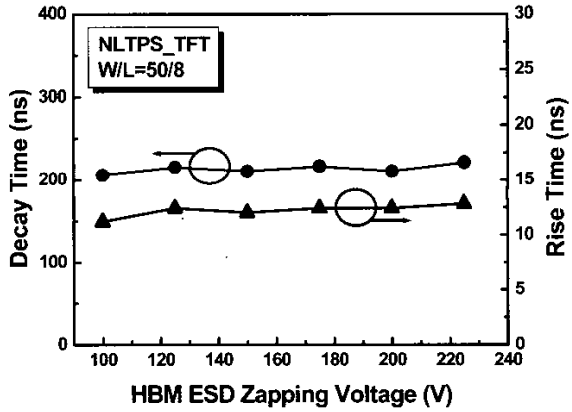


Fig. 6 The rise time and decay time of the HBM current waveform through a TFT device under different HBM ESD zapping voltages.

The rise and decay time of HBM current waveform under different HBM ESD zapping voltages are shown in Fig. 6. The rise time and decay time are independent of the zapping voltage. The reason is that the rise and decay time are mainly affected by the resistor load [7]. However, the resistance of a device with fixed dimension is not varied under different HBM ESD zapping voltages, as shown in Fig. 5.

The measured HBM ESD levels of LTPS TFTs with different channel widths are shown in Fig. 7. It is found that the LTPS TFT device with wider channel width can sustain higher HBM ESD level. The larger junction area and lower

turn-on resistance of LTPS TFT can sustain higher ESD discharging current and heat.

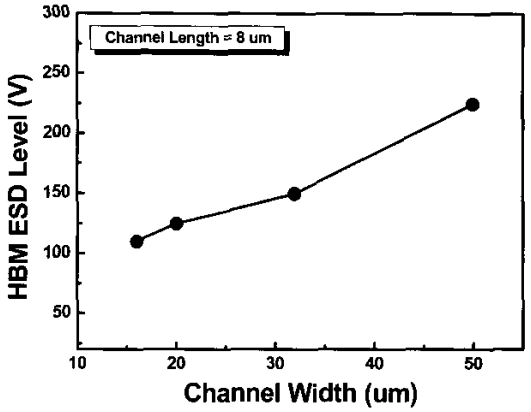


Fig. 7 The relations between HBM ESD level and channel width of N-type LTPS TFTs with different channel widths.

4. TLP Measurement

The TLP-measured I-V curve of an ESD protection element gives not only a failure current, but also the holding voltage and the device turn-on resistance in high current regime. In order to analyze the TLP characteristic of LTPS TFT, the TLP-measured I-V curves on LTPS TFTs with different channel widths are shown in Fig. 8. The pulse width generated by TLP system is 100ns with a rise time of 10ns [8]. Moreover, the failure criteria for device under test is defined as TLP measured I-V curve showing obviously secondary breakdown with negative resistance. The It2 is defined as the current at the beginning of the second breakdown point with negative resistance [9]. As shown in Fig. 8, the N-type LTPS TFT with a device dimension of W/L = 50 μm /8 μm has a It2 of 104 mA. When the channel width is decreased to 16 μm, the It2 decreases to 29.6 mA. The result shows that the top-gate LTPS TFT with larger channel width will has higher ESD robustness.

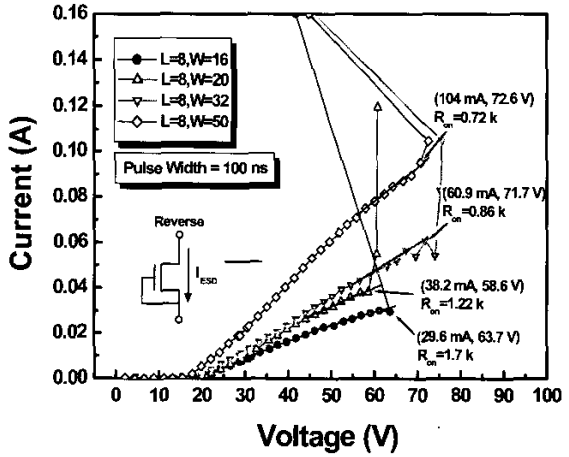


Fig. 8 The TLP-measured I-V curves of the N-type LTPS TFTs with different channel widths.

The relations between It2 and channel width of LTPS TFTs under TLP measurement are shown in Fig. 9, where the It2 value increases linearly with the increase of device channel width. The device turn-on resistance (R_{TLP}) can be also calculated from the slope of TLP-measured I-V curves. Fig. 9 also shows that the turn-on resistance of LTPS TFT decreases when the device channel width is increasing.

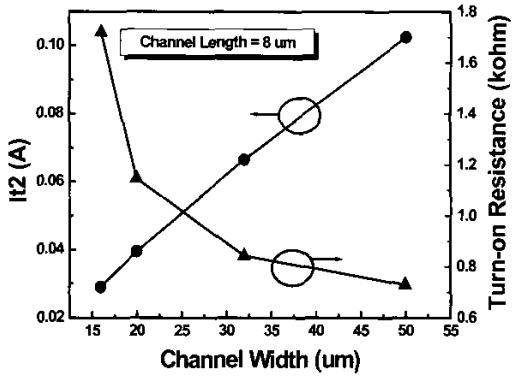


Fig. 9 The relations between It2 and channel width of LTPS TFTs.

5. Correction between HBM ESD and TLP Stresses

The ratio of turn-on resistances between HBM ESD-zapping condition (R_{HBM}) and the TLP-measured condition (R_{TLP}) on different channel widths of LTPS TFTs is shown in Fig. 10. R_{TLP} is the device turn-on resistance calculated from the slope of TLP-measured I-V curves. R_{HBM} is the device turn-on resistance calculated from the measured time-domain ESD waveforms on the LTPS TFT device. The results calculated from HBM ESD stress and TLP measurement show an almost perfect agreement. Therefore, the ESD robustness of LTPS TFT panel can be estimated by measuring the on-glass TFT devices with TLP system.

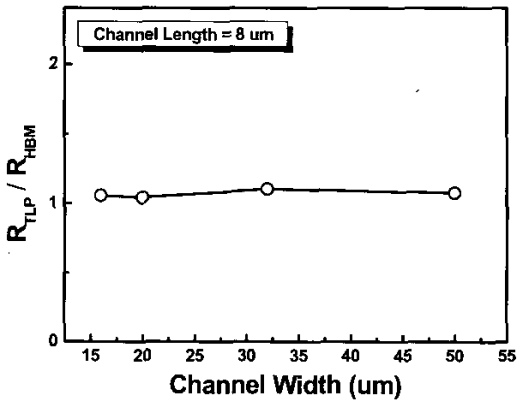


Fig. 10 The ratio of turn-on resistances between HBM ESD-zapping condition (R_{HBM}) and the TLP-measured condition (R_{TLP}) on different channel widths of LTPS TFTs.

6. Failure Behaviour

When the silicon-based CMOS device is damaged by ESD stress, it was burned out to short with an abruptly increasing leakage. Due to the thin poly film and unstable grain boundary traps in the LTPS TFT technology, the failure behavior of LTPS TFT device is quite different from that of CMOS devices. From the TLP-measured I-V curve, the LTPS TFT device would perform short-circuit failure at first and then open-circuit failure after the second breakdown point, but there is no obvious increase of leakage current. Therefore, it is hard to judge whether the LTPS TFT device is damaged, or not, only from the leakage measurement.

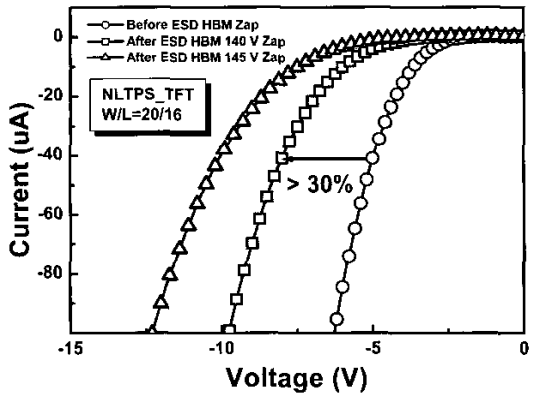
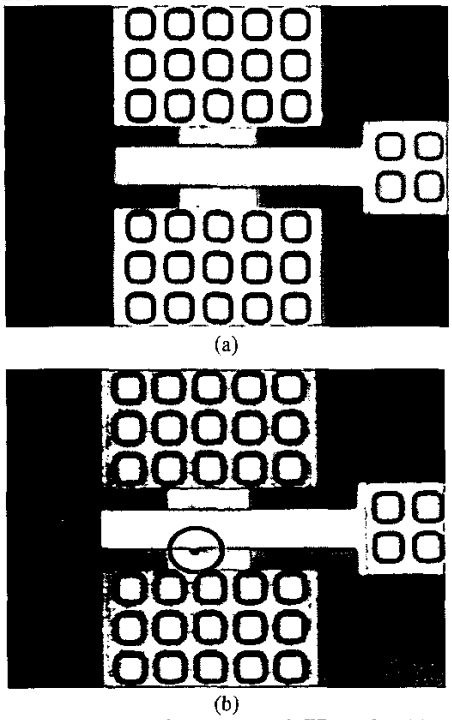


Fig. 11 The measured I-V curve shift of N-type LTPS TFTs under HBM ESD stress.



(a)

(b)

Fig. 12 The top view of N-type LTPS TFTs after (a) 140-V HBM ESD zapping, and (b) 145-V HBM ESD zapping.

The definition of failure criteria in this work is that the voltage shifts greater than 30% under 40 μA after ESD stress [10]. As shown in Fig. 11, the measured I-V curve shift is above 30% after 140-V HBM ESD zapping, but there is no failure spot at the top view of the TFT device in Fig. 12(a). However, the obviously failure spots occurs after 145-V HBM ESD zapping, as shown in Fig. 12(b). Therefore, the failure of LTPS TFT device will occur due to the latent damage before the crash at the top view of device.

7. Conclusion

The characteristics of HBM ESD current waveform on LTPS TFT have been analysed by using a manual ESD tester. The correction between HBM ESD-stress time-domain waveform and TLP-measured I-V curves on the LTPS TFTs with different device dimensions has been investigated. The turn-on resistances of TFT devices under HBM ESD-zapping condition and the TLP-measured condition have been calculated for comparison. The results calculated from HBM ESD stress and TLP measurement show a good agreement. Thus, the TLP system with a pulse width of 100ns and 10 ns rise time can be effectively used to estimate HBM ESD robustness of LTPS TFT panel.

References

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