Gate-Oxide Reliability on CMOS Analog Amplifiers in a 130-nm Low-Voltage CMOS Processes

Jung-Sheng Chen and Ming-Dou Ker

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

***Abstract*—** The effect of gate-oxide reliability in MOSFET on common-source amplifiers is investigated with the non-stacked and stacked structures in a 130-nm low-voltage CMOS process. The supply voltage of 2.5 V is applied on the amplifiers to accelerate and observe the impact of gate-oxide reliability on circuit performances including small-signal gain, unity-gain frequency, and output DC voltage level under DC stress and AC stress with DC offset, respectively. The small-signal parameters of amplifier with non-stacked structure strongly degrade under such overstress conditions. The gate-oxide reliability in analog circuit can be improved by stacked structure for small-signal input and output applications.

1. Introduction

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time-to-breakdown at operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem in the old CMOS technologies, because it had thick gate oxide.

The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown had been investigated on the thin gate oxide [1]. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits had been reported [2]-[10]. In [2], it was demonstrated that the digital circuits would remain functional beyond the first gate-oxide hard breakdown. The gate-oxide breakdown on RF circuit was also studied [4], [5]. Some designs of analog circuits [7] and the mixed-voltage I/O interface [8] indicate that gate-oxide reliability is a very important design consideration in CMOS circuits. The impact of the MOSFET gate-oxide reliability on the CMOS operational amplifiers had been studied [9]. The gate-oxide reliability of MOS switch on switched-capacitor circuit had been also investigated and analyzed [10]. Therefore, gate-oxide reliability is expected to have severe impact to the circuit performances.

In this work, the effect of gate-oxide reliability in MOSFET on common-source amplifiers is investigated with the non-stacked and stacked structures in a 130-nm low-voltage CMOS process. The test chip has been fabricated in a 130-nm low-voltage CMOS process. The small-signal gain, unity-gain frequency, and output DC voltage level of the amplifiers after stresses under supply voltages of 2.5 V are measured and analyzed.

2. Analog Amplifiers

The common-source amplifier is a basic unit in many typical analog circuitry cells, such as level converter and output stage. The common-source amplifiers with the non-stacked and stacked structures are used to verify the impact of MOSFET gate-oxide reliability on CMOS analog amplifier. The complete circuits of the common-source amplifiers with the non-stacked and stacked structures are shown in Figs. 1(a) and 1(b). The common-source amplifiers have been fabricated in a 130-nm low-voltage CMOS process. The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in these two common-source amplifiers are 1-V and 2.5-nm, respectively, in a 130-nm low-voltage CMOS process. The channel width of the MOS transistors in these two common-source amplifiers is set to W_{M1} = 8 μm, W_{M2} = 1 μm, W_{M3} = 1.8 μm, W_{M4} = 2 μm, W_{M5} = 1 μm, and W_{M6} = 1 μm, respectively. The channel length of the M_2 transistor, L_{M2}, is set to 1.5 μm, and that of the other transistors is set to 1 μm, respectively. The body terminals of all NMOS and PMOS transistors are connected to ground and power supply voltage, respectively.

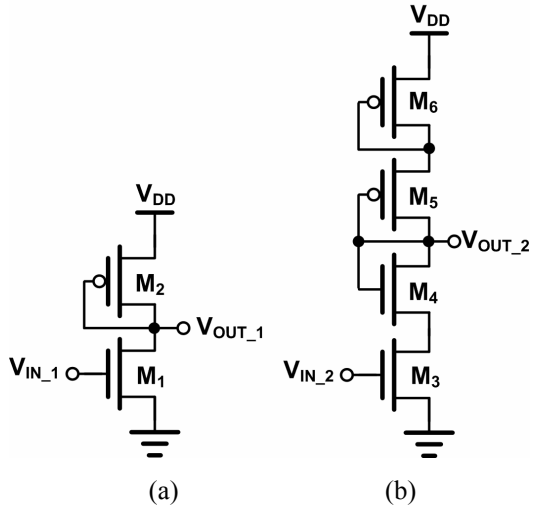

Fig. 1. Complete circuits of the common-source amplifiers with the (a) non-stacked and (b) stacked structures.

The small-signal gain, $A_{V\_Non\text{-}Stacked}$, of the common-source amplifier with the non-stacked structure is given by

$$A_{V\_Non-Stacked} = -\frac{g_{m1} - SC_{GD1}}{g_{o1} + g_{o2} + g_{m2} + S\left(C_{GD1} + C_{GS2} + C_L\right)}, \quad (1)$$

where the g_o and g_m are the output conductance and transconductance of MOS transistor, respectively. In the MOSFET device, the C_{GS} is the parasitic capacitance between the gate and source nodes, and the C_{GD} is the parasitic capacitance between the gate and drain nodes. The C_L is the output capacitive load. The small-signal gain, $A_{V\_Stacked}$, of the common-source amplifier with the stacked structure can be written as

$$A_{V\_Stacked} = -\frac{g_{o3}(g_{m3} - SC_{GD3})}{(SC_{GD3} + g_{o3} + g_{oz})\left[(SC_L + g_{ox} // g_{oy}) - g_{oz}g_{o3}\right]}, \quad (2)$$

where the g_{ox}, g_{oy}, and g_{oz} equal to $g_{m5}+g_{o5}+SC_{GS5}$, $g_{m6}+g_{o6}+SC_{GS6}$, and $g_{m4}+g_{o4}+SC_{GS4}$, respectively. Before overstress, the small-signal gains of the common-source amplifiers with the non-stacked and stacked structures are 17.5-dB and 13.2-dB, respectively. The body effect of the NMOS and PMOS transistors in the common-source amplifiers with the non-stacked and stacked structures is not considered in equations (1) and (2). The phase margins of these two common-source amplifiers are more than 60 degree under output capacitive load of 10 pF.

3. Overstress Test

The impact of gate-oxide reliability on common-source amplifier needs a long-term operation, which may need many years, to measure the performance degradation under the gate-oxide degradation of MOSFET device. In order to accelerate the gate-oxide degradation and observe the impact of gate-oxide reliability on common-source amplifiers with the non-stacked and stacked structures, the common-source amplifiers with the non-stacked and stacked structures are statically stressed by supply voltage V_{DD} of 2.5 V. Because the MOS transistors in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur in conventional time-dependent dielectric breakdown (TDDB). High V_{GS}, V_{GD}, and V_{DS} of the MOSFET are set to get a fast and easy-to-observe breakdown occurrence for investigating the impact of gate-oxide reliability on the common-source amplifier. The advantages of using static stress are the well-defined distributions of the voltages in the common-source amplifiers and the better understanding of the consequences of this stress.

3.1. DC Stress

The power supply voltage, V_{DD}, and output capacitive load, C_L, of the common-source amplifiers with non-stacked and stacked structures are set to 2.5 V and 10 pF, respectively. The input nodes, V_{IN_1} and V_{IN_2}, are biased to 0.5 V in order to set the output DC voltage level at 1.25 V under the power supply voltage of 2.5 V. During this DC overstress, the small-signal gain and unity-gain frequency of the common-source amplifiers with the non-stacked and stacked structures are measured. When those parameters are measured, the input signal of DC 0.5 V at input nodes, V_{IN_1} and V_{IN_2}, is replaced by the AC small-signal of 200 mV sinusoidal signal (peak-to-peak amplitude) with DC offset of 0.5 V.

The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress is shown in Fig. 2. The small-signal gain of the common-source amplifier with the non-stacked structure is degraded by gate-oxide breakdown. Moreover, the common-source amplifier with the non-stacked structure can not maintain its circuit function with continuous stress condition under the DC stress, when the stress time is increased. The small-signal gain of the common-source amplifier with the stacked structure is not changed under the same stress condition even through the stress time up to 2000 minutes. Fig. 3 shows the dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress. The bandwidth of the common-source amplifier with the non-stacked structure on the stress time is decreased, but that of the common-source amplifier with the stacked structure is almost not changed after the stress.

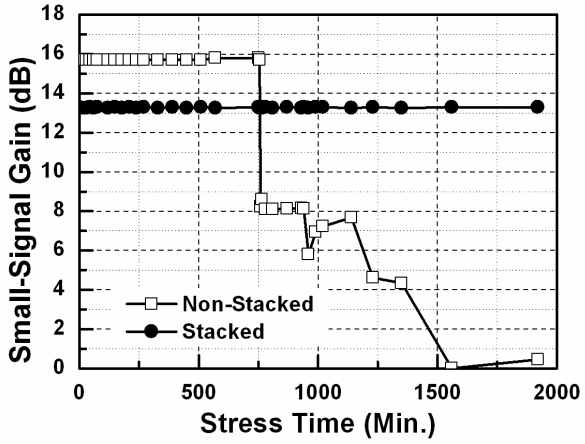

Fig. 2. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress.

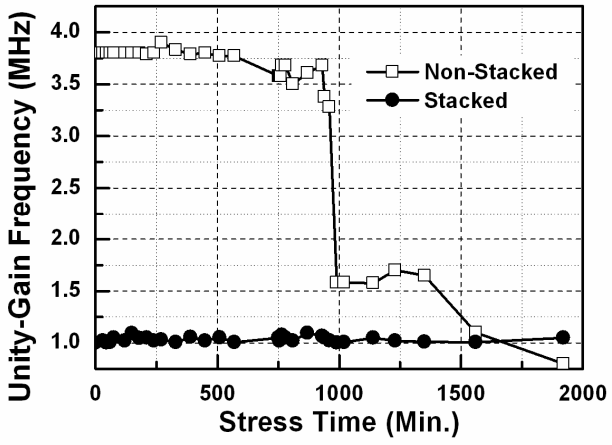

Fig. 3. The dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress.

The dependence of output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress is shown in Fig. 4. The output DC voltage level of the common-source amplifier with the non-stacked structure after stress is approached to the power supply voltage of 2.5 V, but that of the common-source amplifier with the stacked structure is not changed after the stress.

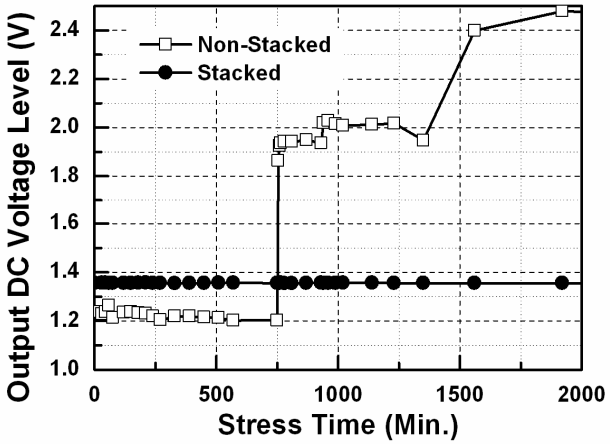

Fig. 4. The dependence of the output DC voltage level on the stress time of the common-source amplifiers with the non-stacked and stacked structures under DC stress.

The reason, why the circuit performances of the common-source amplifier with the non-stacked structure, such as small-signal gain, unity-gain frequency, and output DC voltage level, is degraded by the overstress, is summed up to that the gate-oxide breakdown will degrade the trans-conductance (g_m), threshold voltage (V_{TH}), and output conductance (g_o) of the MOS transistor. In equation (1), if the small-signal parameters g_m, V_{TH}, and g_o of the MOS transistor are degraded with gate-oxide breakdown, the small-signal gain will be changed. From the equation (1), the dominant pole of the common-source amplifier with the non-stacked structure can be written as

$$\omega_{p\_Non-Stacked} = \frac{g_{m2} + g_{o1} + g_{o2}}{C_{GS2} + C_{GD1} + C_L}, \quad (3)$$

which is dominated by transconductance, g_{m2}, and output capacitive load, C_L. Therefore, the unity-gain frequency of the common-source amplifier with the non-stacked structure will be degraded by gate-oxide breakdown. In this test condition, if the transistors, M_1 and M_2, of the common-source amplifier with the non-stacked structure are designed to be operated in saturation region, the output DC voltage level of the common-source amplifier with the non-stacked structure can be expressed as

$$V_{OUT\_1(DC)} = V_{DD} - V_{TH(M_2)} - \sqrt{\frac{\left(\frac{W}{L}\right)_{M_1}}{\left(\frac{W}{L}\right)_{M_2}}}\left(V_{IN\_1} - V_{TH(M1)}\right). \quad (4)$$

In the equation (4), the output DC voltage level, $V_{OUT\_1(DC)}$, is a function of the $V_{TH(M1)}$ and $V_{TH(M2)}$. Therefore, the output DC voltage level of the common-source amplifier with the non-stacked structure should be changed by gate-oxide breakdown after the stress.

3.2. AC Stress with DC Offset

The common-source amplifiers with the non-stacked and stacked structures are continuously tested by the stress of AC small-signal input with DC offset. The input nodes, V_{IN_1} and V_{IN_2}, of the common-source amplifiers with the non-stacked and stacked structures are biased to the AC small-signal input of 200-mV sinusoidal signal (peak-to-peak amplitude) with DC offset voltage of 0.5 V under the different input frequencies of 100 Hz, 500 kHz, and 1 MHz. The power supply voltage, V_{DD}, and output capacitive load, C_L, of the common-source amplifiers with the non-stacked and stacked structures are set to 2.5 V and 10 pF, respectively. The measurement setup is used to investigate the relationship between gate-oxide breakdown and different frequencies of input signals in the CMOS analog circuits.

The dependence of the small-signal gain in the common-source amplifiers with the non-stacked and stacked structures on the stress time under the stress of AC small-signal input with DC offset is shown in Fig. 5. The circuit performances of the common-source amplifier with the stacked structure are not degraded by the stress of the AC small-signal input with DC offset.

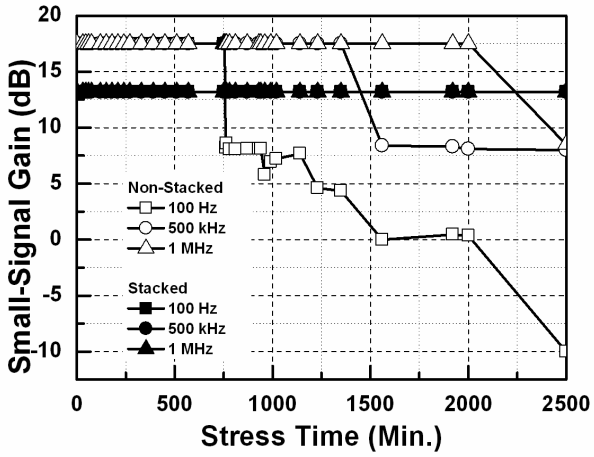

Fig. 5. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the non-stacked and stacked structures under the stress of AC small-signal input with DC offset.

In the common-source amplifier with the non-stacked structure, the high-frequency input signal causes a slow degradation on the small-signal gain, but the low-frequency input signal causes a fast degradation on the small-signal gain under the stress of AC small-signal input with DC offset. The other small-signal performances in the common-source amplifier with the non-stacked structure under the stress of AC small-signal input with DC offset have the similar change

trend as that under DC stress, but the different frequencies of the input stress signal cause the different degradation times. Because the different frequencies of the input stress signal have different periods, the period of the high frequency input signal has shorter time than that of the low frequency input signal. The MOS transistors in analog circuits usually work in the saturation region, so that the gate-oxide breakdown is more likely to occur in conventional time-dependent dielectric breakdown (TDDB). Therefore, the small-signal performance of the non-stacked common-source amplifier with different frequencies of the input signal should cause different degradation times under the stress of AC small-signal input with DC offset.

4. Results and Discussion

The small-signal performance of the common-source amplifier is very sensitivity to the DC operation point. The gate-oxide breakdown will degrade the g_m V_{TH}, and g_o of the MOS transistor to induce the change of DC operation point in the common-source amplifier. Considering the common-source amplifier with the non-stacked structure, if the parameters, g_{m1} and g_{m2}, are variable factors in the equation (1), the sensitivities of the equation (1) to the parameters, g_{m1} and g_{m2}, are expressed as

$$S_{g_{m1}}^{A_{V\_Non-Stacked}} = \frac{g_{m1}}{g_{m1} - SC_{GD1}} \text{ and} \quad (5)$$

$$S_{g_{m2}}^{A_{V\_Non-Stacked}} = \frac{g_{m2}}{g_{o1} + g_{o2} + g_{m2} + S\left(C_{GD1} + C_{GS2} + C_L\right)}. \quad (6)$$

In the equations (5) and (6), the parameters g_{o1} and g_{o2} can be ignored, because they are smaller than 1. The parasitic capacitances C_{GD1} and C_{GS2} of the MOS transistors are not considered. Therefore, the sensitivities of the equations (1) and (2) to the parameters g_{m1} and g_{m2}, respectively, are approached 1. Therefore, the gate-oxide breakdown of the MOS transistors has serious impact on the circuit performances of analog circuits.

The gate-oxide breakdown can degrade the trans-conductance (g_m), output conductance (g_o), and threshold voltage (V_{TH}) of MOSFET devices. After the overstress, the performances of the common-source amplifier with the non-stacked structure under the DC stress and AC stress with DC offset are seriously degraded by stress-induced gate-oxide breakdown, but those of the common-source amplifier with the stacked structure are not changed under the same stresses. Therefore, the gate-oxide reliability is a very important design issue to analog circuits in the nano-meter CMOS process. The gate-oxide reliability can be improved by the stacked structure in the common-source amplifier for small-signal input and output applications. The common-source amplifier with the stacked structure can be worked in high supply voltage depended on the stacked number of transistors used to control the voltages (V_{GS}, V_{GD}, and V_{DS}) across the transistors and to avoid the gate-oxide breakdown in the circuit.

5. Conclusion

The impact of gate-oxide reliability on CMOS common-source amplifiers with the non-stacked and stacked structures has been investigated and analyzed under the DC stress and AC stress with DC offset. The small-signal parameters of the common-source amplifier with the non-stacked structure are seriously degraded by gate-oxide breakdown under analog applications. The analog integrated circuit with the stacked structure, depended on itself bias point of MOSFET device, can be used to improve circuit reliability under the operations with small-signal input and output. The more exact device breakdown model and circuit design solution should be developed to improve the circuit reliability of analog circuits in low-voltage CMOS process.

References

[1] K. Eriguchi and M. Niwa, "Stress polarity dependence of the activation energy in time-dependent dielectric breakdown of thin gate oxides" *IEEE Electron Device Lett.*, vol. 19, pp. 339-401, Dec. 1998.

[2] B. Kaczer, R. Degraeve, M. Rasras, K. V. D. Mieroop, P. J. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, vol. 49, pp. 500-506, Mar. 2002.

[3] B. Kaczer and G. Groesenken, "Potential vulnerability of dynamic CMOS logic to soft gate oxide breakdown," *IEEE Electron Device Lett.*, vol. 24, pp. 742-744, Dec. 2003.

[4] H. Yang, J. S. Yuan, T. Liu, and E. Xiao, "Effect of gate-oxide breakdown on RF performance," *IEEE Trans. Device Materials Reliabil.*, vol. 3, pp. 93-97, Sept. 2003.

[5] E. Xiao, J. S. Yuan, T. Liu, and H. Yang, "CMOS RF and DC reliability subject to hot carrier stress and oxide soft breakdown," *IEEE Trans. Device Materials Reliabil.*, vol. 4, pp. 92-98, Mar. 2004.

[6] A. Aevllan and W. H. Kraustschneider, "Impact of soft and hard breakdown on analog and digital circuits," *IEEE Trans. Device Materials Reliabil.*, vol. 4, pp. 676-680, Dec. 2004.

[7] A. M. Abo and P. R. Gray, "A 1.5 V, 10 bits, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599-606, May 1999.

[8] M.-D. Ker and S.-L. Chen, "Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve 3xVDD input tolerance by using 1xVDD devices and single VDD power supply," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 524-525.

[9] J.-S. Chen and M.-D. Ker, "Impact of MOSFET gate-oxide reliability in CMOS operational amplifiers in a 130-nm low-voltage CMOS process," in *Proc. IEEE Int. Reliability Physics Symp.*, 2005, pp. 423-430.

[10] J.-S. Chen and M.-D. Ker, "Circuit performance degradation of sample-and-hold amplifier due to gate-oxide overstress in a 130-nm CMOS process," in *Proc. IEEE Int. Reliability Physics Symp.*, 2006, pp. 705-706.