

# Abnormal ESD Damages Occur in Interface Circuits between Different Power Domains in ND-Mode MM ESD Stress

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## Abstract

Complex ESD failure mechanisms have been found in the interface circuits of an IC product with multiple separated power domains. The MM ESD robustness can not achieve 150 V in this IC product with separated power domains, although it has the 2-kV HBM ESD robustness. The ND-mode MM ESD currents were discharged by circuitous current paths through interface circuits to cause the gate oxide damage, junction filament, and contact destroy of the internal transistors. The detailed discharging paths of each ND-mode ESD failure were analysed in this paper.

## 1. Introduction

As the ultra-large-scale-integrated (ULSI) circuits being continually developed toward system-on-chip (SoC) designs, more and more multiple separated power domains are used in SoC IC for special circuit applications, such as digital/analog circuit blocks, mixed-voltage circuit blocks, and power management considerations. However, the IC products with multiple separated power domains often have more unexpected current paths during ESD stresses and easily cause damage on interface circuits between different power domains beyond the ESD protection circuits of I/O cells [1]. Such ESD failures in interface circuits between different power domains are often difficult to be clearly examined and modified, even with a lot of failure analysis procedures and extra cost. Therefore, the ESD protection solutions had been studied and proposed to avoid ESD damage on the interface circuits of two separated power domains [2]-[7]. However, the proposed ESD protection solutions could cause the circuit performance degradation in some special applications.

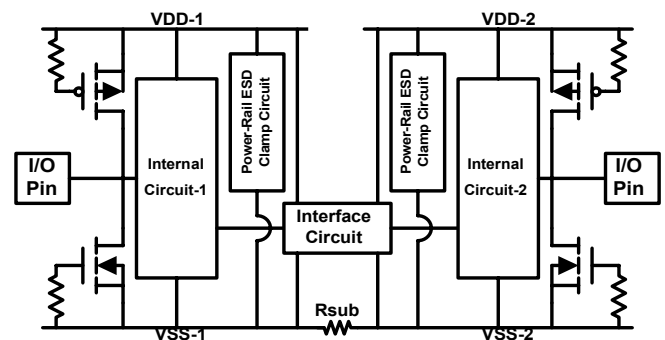
In this paper, a failure study of the internal ESD damages on the interface circuits of a 0.35- $\mu\text{m}$  3.3 V/5 V mixed-mode CMOS IC product with two separated power domains is presented. The ESD failure spots were specially observed at the interface circuits of the separated power domains after negative-to-VDD mode (ND-mode) machine-model (MM) ESD stress of 100 V. However, this IC product has a 2-kV human-body-model (HBM) ESD robustness in each ESD test combination of I/O pin to power/ground pins.

## 2. ESD Protection and Robustness

### 2.1 ESD Protection for an IC with Separated Power Pins

The ESD protection schemes for input, output, and power-rail ESD clamp circuits in this IC product are shown in Fig. 1. The gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) with a channel length/width of 0.8  $\mu\text{m}$ /300  $\mu\text{m}$

are used for pad-to-VSS and pad-to-VDD ESD protection of I/O pins, respectively. The efficient power-rail ESD clamp circuit, which is the substrate-triggered field-oxide-device (STFOD) [8] of 216  $\mu\text{m}$  with RC-based ESD transient detection circuit, is individually installed in each power domain, as illustrated in Fig. 1. The internal circuit-1 is the digital circuit block and the internal circuit-2 is the analog circuit block. Due to power noise considerations, the VDD-1 was separated from the VDD-2. Then, the VSS-1 and VSS-2 only connected by the parasitic p-substrate resistance ( $R_{\text{sub}}$ ).



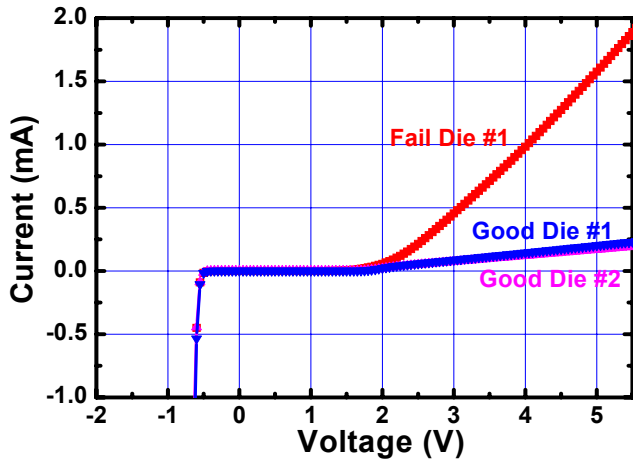
**Fig. 1: The ESD protection schemes in an IC product with separated power lines. The protection circuits include input, output, and power-rail ESD clamp circuits.**

### 2.2 Internal ESD Damages on the Interface

After HBM ESD tests of all I/O pins to each power/ground pin and power-to-ground ESD test, the HBM ESD robustness achieved 2 kV. However, the MM ESD robustness can not achieve 200 V in positive-to-VSS mode (PS-mode), positive-to-VDD mode (PD-mode), negative-to-VSS mode (NS-mode), and ND-mode MM ESD stresses. Even the ND-mode MM ESD robustness of Pin-A and Pin-B can not achieve 200 V by VDD-1 and VDD-2 shorting together in test board under ND-mode ESD stress condition. The ESD test results for this IC product are shown in Table I.

**Table I: ESD Robustness**

ESD Test	I/O Pin	PS-Mode	NS-Mode	PD-Mode	ND-Mode
HBM	Pin-A	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
	Pin-B	> 2.0 kV	> 2.0 kV	> 2.0 kV	> 2.0 kV
MM	Pin-A	< 200 V	< 200 V	< 200 V	< 200 V
	Pin-B	< 200 V	< 200 V	< 200 V	< 150 V



**Fig. 2:** The I-V characteristics of VDD-2-to-VSS-2 showed higher leakage current compared with good dies reference after ND-mode MM ESD stress on I/O pins.

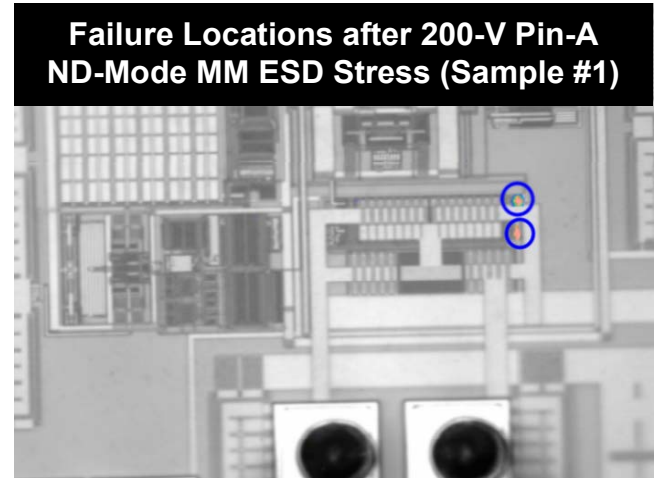
When ESD tests are finished, a monitor of the leakage current is used to judge whether the I/O pin under ESD test is passed or failed. The traced I-V characteristics of investigated IC before and after ESD stress are shown in Fig. 2. Obviously, after the 200-V MM ESD stress, the leakage current at 3.3 V between VDD-2 and VSS-2 showed higher leakage current about 10 times as compared with good dies reference. From the measured I-V characteristics, there are some internal damages in the internal circuits between VDD-2 and VSS-2 after ESD stress.

### 3. Failure Mechanism and Protection Solutions

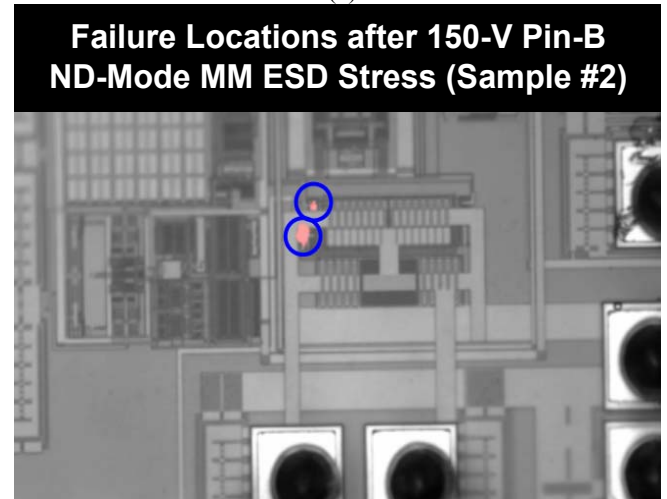
In order to indicate the failure locations caused by ESD stress, the emission microscope (EMMI) was used to find abnormal ESD failure spots in this IC. The measured EMMI photos are shown in Fig. 3 with the corresponding IC layout patterns of the ND-mode failure sample. All the circled areas in Fig. 3 are the damage locations indicated by EMMI found around the interface circuits after ND-mode MM ESD stress.

The ND-mode MM ESD damages are recognized at the interface circuits by comparison with circuits and layout patterns to the SEM photos of ESD damaged failure spots. After Pin-A ND-mode MM ESD stress, the SEM photos of failure spots are shown in Figs. 4(a) and 4(b). The clear failure spots were found in two PMOS transistors (M1 and M2) of the interface circuits. However, the Pin-A are connected to the internal circuit-1 through a 20-k $\Omega$  poly-resistor, which can effectively block the ESD currents to damage internal circuits. Therefore, the ESD current could be discharged by the circuitous path to cause damages on the M1 and M2 after Pin-A ND-mode MM ESD stress, as shown in Fig. 5. Due to the larger device size of the Ma in Fig. 5, the ESD current didn't destroy it during MM ESD stress. On the other hand, the failure spots were also found in two transistors of interface circuits after Pin-B ND-mode MM ESD stress, as shown in Figs. 6(a) and 6(b). ND-mode MM ESD currents were discharged by two mainly current paths, as the dashed lines shown in Fig. 7. These two paths provided the current paths to distributively discharge ESD current. The

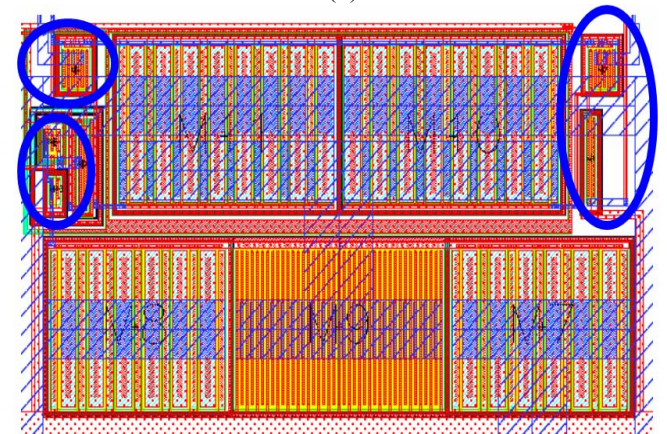
corresponding failure photos on the interface devices Mb and M3 are shown in Figs. 6(a) and 6(b), respectively.



(a)



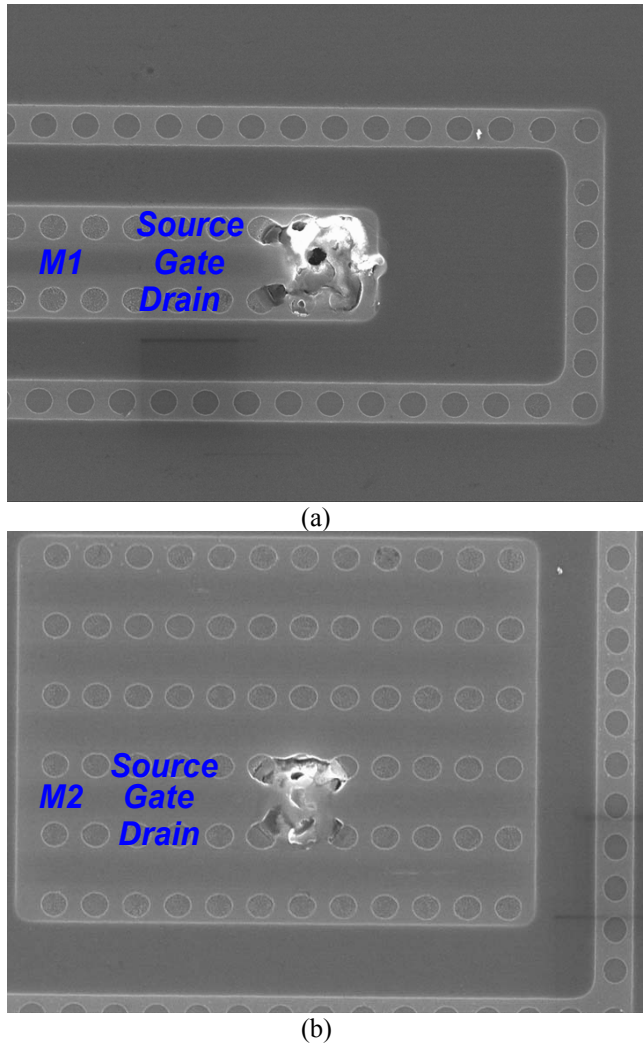
(b)



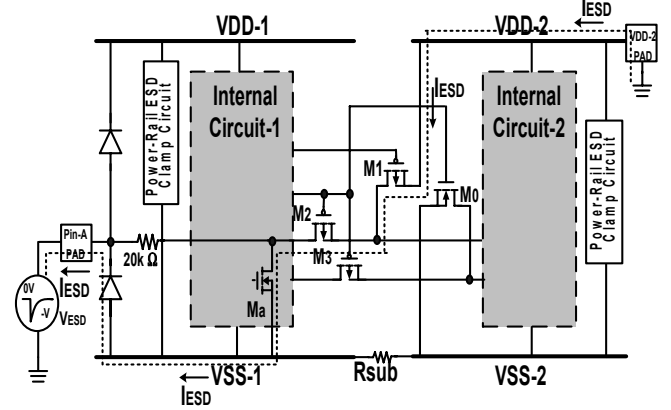
(c)

**Fig. 3:** Abnormal EMMI hot spots were found at the interface circuits (see the circled area) under (a) Pin-A ND-mode MM ESD stress, (b) Pin-B ND-mode MM ESD stress conditions. (c) The corresponding layout of the interface circuits indicated the failure spots shown in (a) and (b).

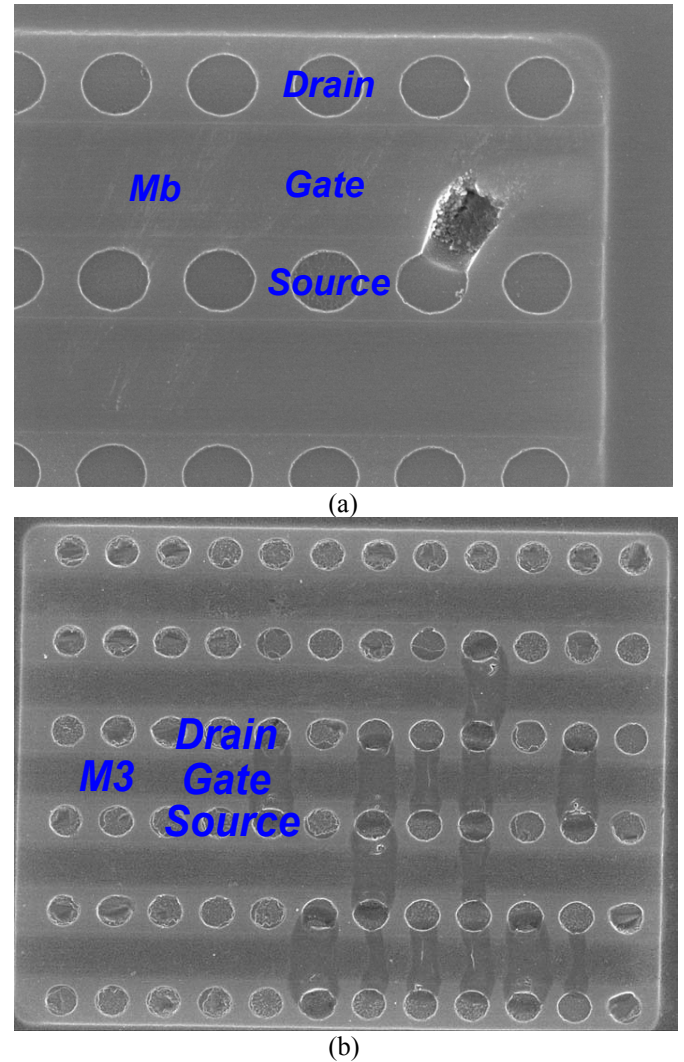
To overcome this ESD failure at the interface circuits, adding the suitable blocking resistors ( $R_{block}$ ) to the interface devices and installing the ground-connection ESD cell in original ESD protection scheme were proposed in Fig. 8. Two extra blocking resistors are added at the source terminal of the M1 and the gate terminal of the Mb, respectively. The ground-connection ESD cell used to connect the separated ground lines is implemented by using bi-directional diode strings [9]. The diode number in the ground-connection ESD cell was optimized to prevent substrate noise coupling issue and leakage issue. To further provide higher substrate noise isolation, the bi-directional silicon-controlled rectifier (SCR) [10] with ESD-detection circuit can be used to replace the series diodes between the separated power lines. By using the proposed ESD protection solution, the ESD current will be effectively discharged along ground lines under ND-mode MM ESD stress. Therefore, the abnormal internal ESD damages can be overcome in this IC product with separated power lines.



**Fig. 4:** After Pin-A ND-mode MM ESD stress, the SEM photos of failure spots were located at (a) PMOS transistor (M1) and (b) the other PMOS transistor (M2).

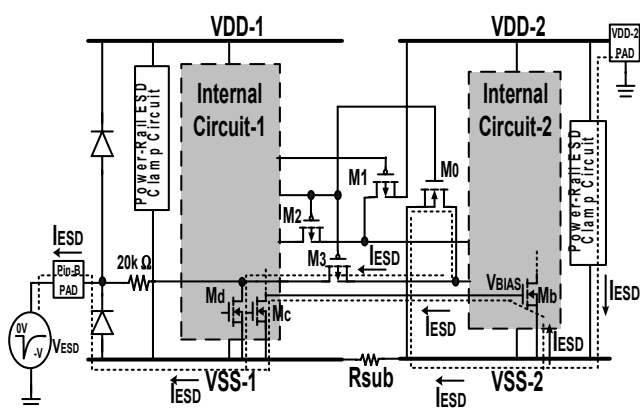


**Fig. 5:** The ESD current could be discharged through the circuitous path to cause ESD damages on the M1 and M2 during Pin-A ND-mode MM ESD stress.

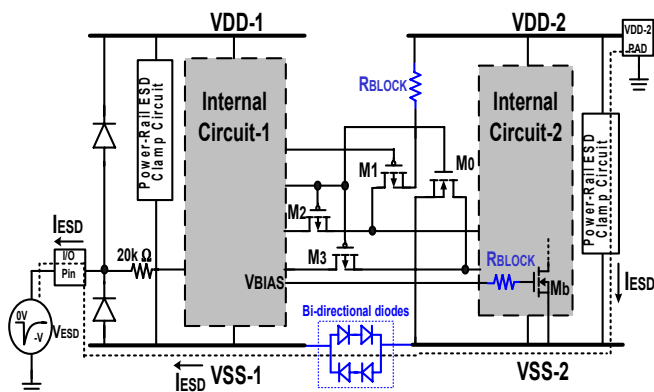


**Fig. 6:** SEM photos for (a) NMOS transistor (Mb) and (b) PMOS transistor (M3) of interface circuits after Pin-B ND-mode MM ESD stress, respectively.





**Fig. 7: ESD discharging paths under Pin-B ND-mode MM ESD stress. The Mb and M3 of interface circuits are damaged during such ESD stress.**



**Fig. 8: Final version of ESD protection scheme in this IC product with separated power lines.**

## 4. Conclusion

Due to the circuit performance considerations, the IC product has two separated power domains to cause ESD failure in interface circuits between different power domains. MM ESD currents is discharged through some unexpected paths in the interface circuits during ND-mode ESD stress. Each failure mechanism of Pin-A and Pin-B has been clearly analyzed and illustrated by the failure spot images and ESD current discharge paths. The effective solutions have been proposed to overcome abnormal internal ESD damage by means of adding the blocking resistors to the interface devices and installing the suitable power connection cells between the separated power lines. The optimum modifications have been proven in the new version IC product to sustain MM ESD level of greater than 200V.

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