Transient-Induced Latchup in CMOS Integrated Circuits due to Electrical Fast Transient (EFT) Test

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Abstract

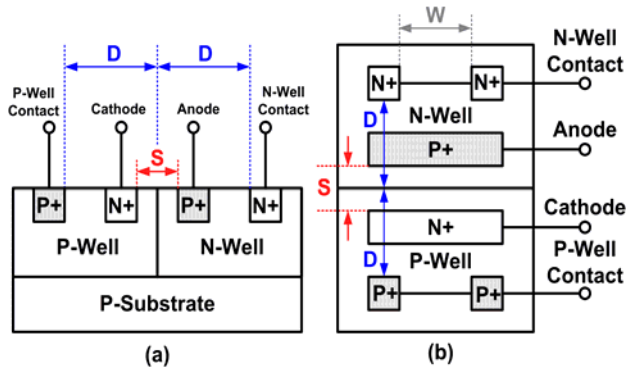
The transient-induced latchup (TLU) in CMOS ICs under electrical fast transient (EFT) test has been investigated by experimental verification. With positive and negative voltage pulses under EFT test, the TLU can be triggered on in CMOS ICs with the parasitic pnpn structure. The physical mechanism of TLU in CMOS ICs has been developed with experimental verification in time domain. All the experimental evaluations have been verified with the silicon-controlled rectifier (SCR) test structure fabricated in a 0.18-μm CMOS technology.

1. Introduction

Recently, the electromagnetic compatibility (EMC) of integrated circuits (ICs) has attracted more attentions than before in microelectronic products. This tendency is caused by several reasons. First, there are much more complicated implementations of ICs, such as mixed-signal, multiple power supplies, system-on-chip (SoC), etc. The environment where these CMOS devices are located will suffer from considerable noises coming from both interior and exterior of CMOS ICs. Second, more and more ICs are susceptible to the strict requirement of reliability regulation, such as electrical fast transient (EFT) test for EMC [1]. During the EFT test, the EFT-generated transient voltage is quite large (with an amplitude of several hundreds volts) and fast (with a pulse duration of several tens nanoseconds), which can couple into power pins or I/O pins of the ICs. Third, aggressive scaling of both device feature size, as well as the clearance between PMOS and NMOS devices, leads the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs to exhibit weak latchup immunity [2]-[5]. It has been reported that the transient noise on power and ground lines (pins) of CMOS ICs can easily trigger on the transient-induced latchup (TLU) [6]-[8], even though such TLU-sensitive CMOS ICs have already met the requirements of the quasi-static latchup test standard [9]. Therefore, engineers have to deal with the lower immunity to TLU failures due to electromagnetic interferences in microelectronic products. Since the susceptibility of a final microelectronic product may only depend on just one single chip (such as SoC), the characterization of EMC susceptibility at the IC level is getting more important.

2. Test Structure

An SCR device is used as the test structure for TLU measurement under EFT test because the occurrence of latchup results from the parasitic SCR in CMOS ICs. The device cross-sectional view and layout top view of SCR in CMOS ICs are sketched in Figs. 1(a) and 1(b), respectively. The geometric parameters such as D, S, and W represent the distances between well edge and well contact, anode and cathode, and the adjacent well contacts, respectively. In CMOS ICs, the P+ anode (source of PMOS) and N+ well contact are connected to V_{DD}, whereas the N+ cathode (source of NMOS) and the P+ well contact are connected to ground. Once latchup occurs inside the SCR structure, huge current will be generated through a mechanism of positive-feedback regeneration [10]. The SCR structure used in this paper is fabricated in a 0.18-μm CMOS technology with layout parameters of D=9.7μm, S=3.64μm, and W=0.28μm.



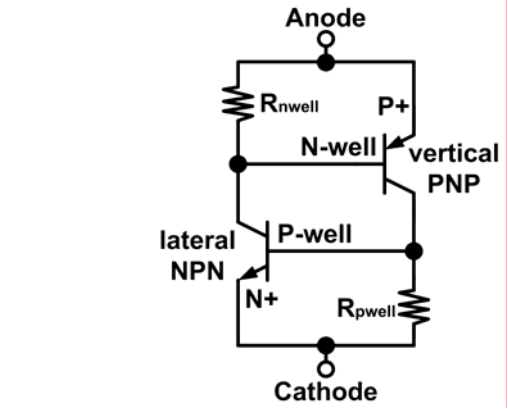
(a)

Fig. 1. (a) The device cross-sectional view, and (b) layout top view, of the SCR structure in CMOS ICs.

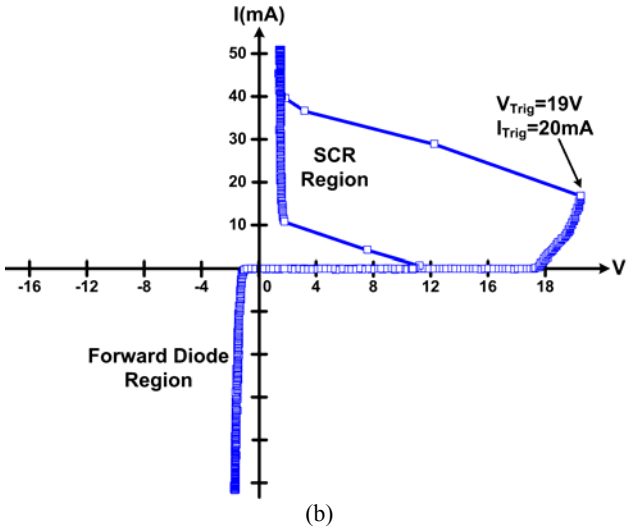
The equivalent circuit schematic of the SCR structure is shown in Fig. 2(a). The SCR structure consists of a lateral NPN and a vertical PNP bipolar transistor to form 2-terminal/4-layer PNPN (P+/N-well/P-well/N+) structure. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of the N-well/P-well junction, which could be as high as 22V in a 0.25-μm CMOS process, or ~19V in a 0.18-μm CMOS process. When the positive voltage applied to the anode of SCR is greater than the breakdown voltage with its cathode relatively grounded, the hole and electron current will be generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to P+ diffusion connected to ground, whereas the electron current will flow the N-well to N+ diffusion connected to the anode of SCR. As long as the voltage drop across the P-well resistor (R_{pwell}) (N-well resistor (R_{nwell})) is greater than 0.7V, the NPN (PNP) transistor will be turned on to inject the electron (hole) current to further bias the PNP (NPN) transistor, which initiates the SCR latching action. Finally, the SCR will be fully triggered into its latching state with the

positive-feedback regenerative mechanism [10].

The DC I-V characteristic of the SCR device is shown in Fig. 2(b). Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistor on can be generated through the positive-feedback mechanism of latchup without involving the avalanche breakdown mechanism again. So, the SCR has a lower holding voltage (V_{hold}) of typically ~1.5V in bulk CMOS processes. If the negative voltage is applied on the anode terminal of the SCR, the parasitic diode (N-well/P-well junction) inherent in the SCR structure will be forward biased to clamp the negative voltage at a lower voltage level of ~1V (cut-in voltage of a diode). Whatever the ESD energy is positive or negative, the SCR device can clamp ESD overstresses to a lower voltage level. Thus, the SCR device can sustain the highest ESD robustness within a smaller layout area in CMOS ICs.



(a)



(b)

Fig. 2. (a) Equivalent circuit schematic of a SCR device. (b) I-V characteristics of SCR device in a 0.18-μm CMOS process under positive and negative voltage biases.

3. Measurement Setup

The measurement setup for EFT test [1] is shown in Fig. 3. A supply voltage of 1.8V is used as V_{DD} and the EFT generator is directly connected to the device under test (DUT) in this work. The voltage and current waveforms on the DUT (at V_{DD} node) during/after EFT test are monitored by the digital oscilloscope. The repetitive EFT test is a test with bursts consisting of a number of fast pulses. The standard of IEC 61000-4-4 defines immunity requirements and test methods for electronic equipment to repetitive fast transients such as those originating from interruption of inductive loads or relay contact bounce. The standard also defines the test voltage waveforms of these fast transients with the repetition frequency of 5kHz and 100kHz. The use of 5kHz repetition rate is traditional EFT test and 100kHz is closer to reality. For both repetition rates, the burst repeats every 300ms and the application time is not less than 1 minute. The minimum start value of the pulse peak is ±200V. For EFT pulse with the repetition frequency of 5kHz, the general voltage waveforms are shown in Figs 4(a) and 4(b). In Fig. 4(a), the burst duration is 15ms. In Fig. 4(b), the waveform of a single pulse has a rise time of about 5ns and the pulse duration (full width at half maximum) of 50ns.

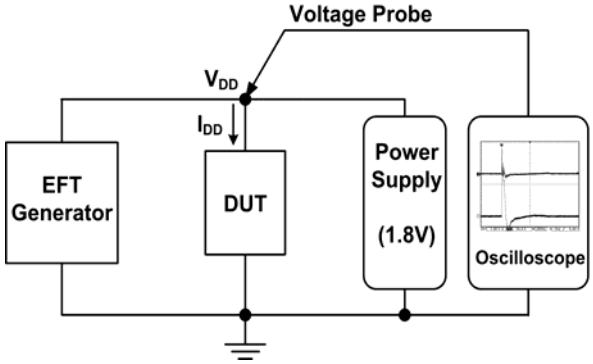
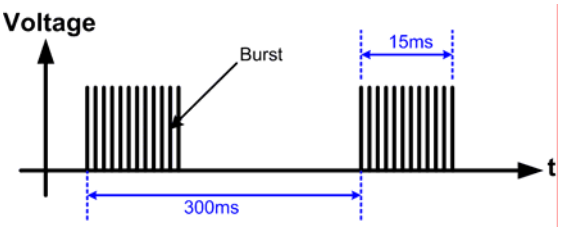
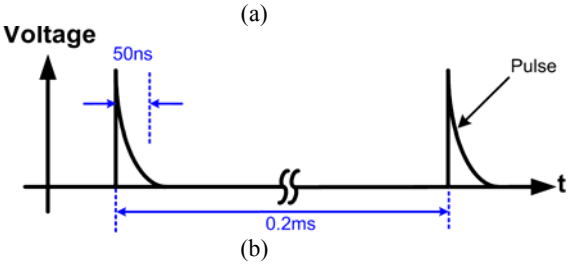


Fig. 3. Measurement setup for electrical fast transient (EFT) test with the power supply of 1.8V to DUT.



(a)



(b)

Fig. 4. Specified EFT transient waveforms of (a) burst, and (b) each pulse, according to the standard of IEC 61000-4-4.

4. Experimental Results

With the measurement setup shown in Fig. 3, the minimum EFT level to induce TLU in the SCR can be determined. With both positive and negative EFT voltage pulse, the measured V_{DD} (I_{DD}) transient response will be

recorded through the voltage (current) probe to display on the oscilloscope. This will clearly indicate whether the TLU occurs (I_{DD} significantly increases) after the EFT test with positive or negative EFT voltage pulse. Here the TLU level is defined as the minimum positive (negative) voltage provided by the EFT generator to trigger on TLU in the SCR. The specified SCR structure with layout parameters of D=9.7m, S=3.64m, and W=0.28m fabricated in a 0.18-μm CMOS technology is used for all the TLU measurements in this work.

With a negative EFT voltage level of -200V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Fig. 5. Obviously, I_{DD} current appears due to the forward-biased N-well/P-well junction when V_{DD} decreases below 0V during EFT test. When V_{DD} increases from $-V_{peak}$ to its normal operating voltage (+1.8V), the N-well/P-well junction will rapidly change from the forward-biased state to its original reverse-biased state. Meanwhile, inside the N-well (P-well) region, larger number of stored minority holes (electrons) offered by the forward peak current, will be instantaneously "swept-back" to the P-well (N-well) region where they originally come from. Thus, such "swept-back" current, I_{sb}, will produce a localized voltage drop while flowing through the parasitic P-well or N-well resistance. Once this localized voltage drop approaches to some critical value, the emitter-base junction of either vertical PNP or lateral NPN BJT in SCR structure will be forward biased to further trigger on latchup. Afterwards, I_{DD} will greatly increase while V_{DD} returns to above 0V, which indicates the occurrence of latchup. Finally, V_{DD} (I_{DD}) waveform is locked at a low voltage (high current) latchup state after this transition.

With a positive EFT voltage level of +200V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Fig. 6. V_{DD} begins to increase rapidly from the normal operating voltage (+1.8V) to a positive peak voltage of above +100V. Meanwhile, the N-well/P-well junction is reverse biased, and thus large transient displacement current (I_{DS}) can be generated within the SCR due to large increasing rate ($\equiv +V_{peak}-1.8V$/rise time) of V_{DD} [11]. In Fig. 6, the V_{DD} waveform is oscillatory after the positive EFT voltage pulse. Afterwards, once large enough swept-back current (I_{sb}) is produced when V_{DD} increases from negative voltage back to the normal operating voltage, TLU can be triggered on with significantly increased I_{DD}.

The SCR structure in bulk CMOS processes is susceptible to TLU (absolute values of both positive and negative TLU levels are all 200V) unless the SCR is latchup-free (latchup holding voltage of SCR is larger than the normal operating voltage of +1.8V). Due to such weak immunity against TLU, latchup prevention skills should be necessary to improve TLU immunity for core circuitry.

5. Discussion

With the positive EFT pulse, the N-well/P-well junction is reverse biased, and thus transient displacement current caused by N-well / P-well junction can be found within the

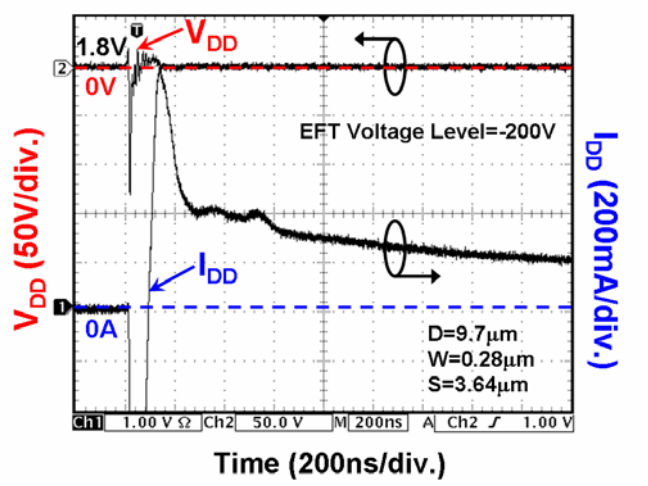


Fig. 5. Measured V_{DD} and I_{DD} transient waveforms on the SCR structure in CMOS ICs under the EFT test with a negative voltage level of -200V.

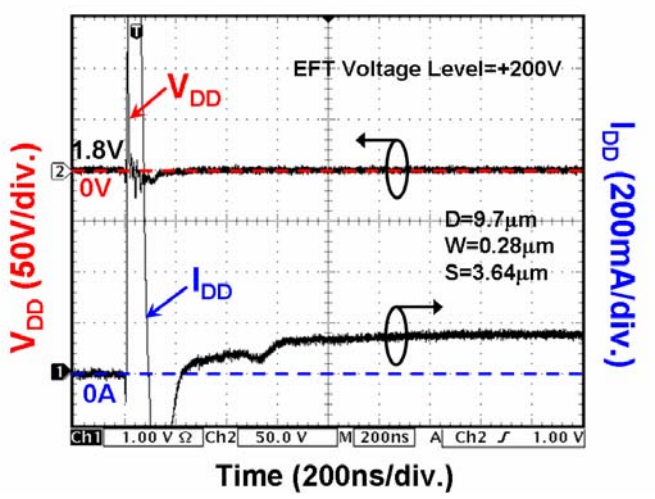


Fig. 6. Measured V_{DD} and I_{DD} transient waveforms on the SCR structure in CMOS ICs under the EFT test with a positive voltage level of +200V.

SCR. In Fig. 6, the V_{DD} waveform is oscillatory after the positive EFT voltage pulse. Meanwhile, V_{DD} decreases from its positive peak voltage to negative voltage value. Within this duration, the N-well/P-well junction changes from the revise-biased state to the forward-biased state, while more and more minority electrons (holes) are injected into the P-well (N-well) region. Once these minority carriers are subsequently swept back to N-well (P-well) regions where they originally come from, it has been reported that TLU can be triggered on due to such large enough swept-back current (I_{sb}) [12]. As a result, TLU occurs because the huge I_{DD} can be found after EFT test.

Under the EFT test with the negative voltage pulse, it has been proved that the swept-back current, I_{sb}, caused by the minority carrier stored within the parasitic pnpn structure of CMOS ICs is the major cause of the TLU. For simplicity,

two reasonable assumptions are given. First, the N-well/P-well junction is treated as an ideal 1-D diode with step junction profile, as the inset figure shown in Fig. 7. Second, the storage time of minority carriers is assumed to be negligible because I_{DD} can rapidly follow the polarity variation of V_{DD}. Therefore, from the assumptions, Q_{stored} inside the N-well region can be expressed as

$$Q_{stored} \equiv \int_{X_n}^{X_{n'}} \left[P_n(x,t)\Big|_{t=t_B} - P_n(x,t)\Big|_{t=t_A} \right] dx , \qquad (1)$$

where t_A (t_B) is the initial (final) timing point of a specific duration when I_{sb} exists. Q_{stored} represents the total stored minority carriers (holes) causing I_{sb} ($t_A \le t \le t_B$) inside the N-well region. Compared with the quasi-static latchup test, the specific duration ($t_A \le t \le t_B$) in EFT test is much shorter than that in quasi-static latchup test because the EFT pulse duration is only several tens nanoseconds. The rise time (fall) time for quasi-static latchup test is much longer (~μs) than that for EFT test. Thus, once these Q_{stored} are swept back to the regions where they come from, the averaged I_{sb} can be expressed as

$$I_{sb} \equiv \frac{Q_{stored}}{t_B - t_A} . \qquad (2)$$

In both TLU and quasi-static latchup conditions, if the initial ($t=t_A$) and the final ($t=t_B$) voltages during $t_A \le t \le t_B$ are equal (i.e. with the same amount Q_{stored}), the averaged I_{sb} in TLU case will be about 10^3~10^6 times larger than that in the quasi-static latchup case. The averaged I_{sb} is rather small and hard to trigger on latchup in quasi-static latchup test. Thus, the averaged I_{sb} is large enough to easily trigger on latchup in the SCR structure under EFT test.

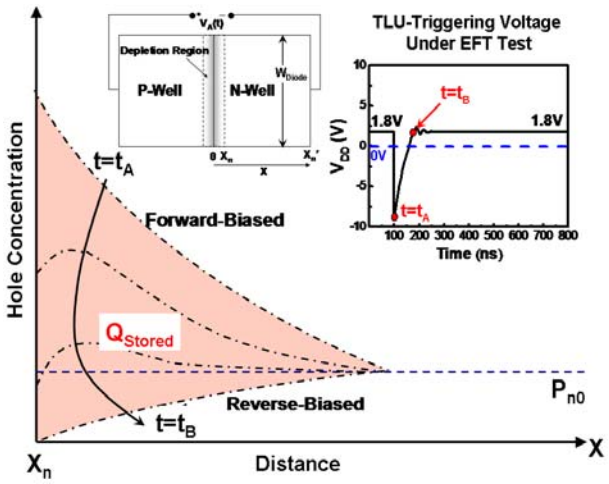


Fig. 7. Total stored minority carriers, Q_{stored}, causing I_{sb} ($t_A \le t \le t_B$) inside the N-well region. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged I_{sb}.

6. Conclusion

The positive and negative EFT voltage pulses have been clarified as the realistic TLU-triggering stimulus under the EFT test. From experimental measurements, the specific "swept-back" current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been proved to be the cause of TLU. Thus, TLU reliability may still exist in qualified CMOS IC products through quasi-static latchup test. Because TLU reliability issue potentially exists within the whole circuitry of CMOS ICs, latchup prevention skills such as layout optimization, the special advanced process technologies, or circuit technique should be necessary to improve TLU immunity for core circuitry under EFT test. With understanding on the physical mechanism and experimental verification on TLU, safe design/layout rules or circuit techniques in CMOS ICs can be developed against TLU events under EFT test.

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References

[1] IEC 61000-4-4 International Standard, "*EMC – Part 4-4: Testing and Measurement Techniques – Electrostatic Fast Transient/Burst Immunity Test*," International Electrotechnical Commision, 2004.

[2] S. Voldman, "Latch-up – Its back," in *Threshold Newsletter*: ESD Association, Sep./Oct. 2003.

[3] S. Voldman, E. Gebreselasic, M. Zierak, D. Hershberger, D. Collins, N. Feilchenfeld, S. St. Onge, and J. Dunn, "Latchup in merged triple well structure," in *Proc. IEEE Int. Reliability Physics Symp. (IRPS)*, 2005, pp. 129-136.

[4] C. Duvvury and G. Boselli, "ESD and latch-up reliability for nanometer CMOS technologies," in *IEDM Tech. Dig.*, 2004, pp. 933-936.

[5] G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: A scaling perspective," in *Proc. IEEE Int. Reliability Physics Symp. (IRPS)*, 2005, pp. 137-144.

[6] S. Bargstatd-Franke, W. Stadler, K. Esmark, M. Streibl, K. Domanski, H. Gieser, H. Wolf, and W. Bala, "Transient latch-up: Experimental analysis and device simulation," in *Proc. EOS/ESD Symp.*, 2003, pp. 80-87.

[7] J. T. Mechler, C. Brennan, J. Massucco, R. Rossi, and L. Wissel, "Contention-induced latchup," in *Proc. IEEE Int. Reliability Physics Symp. (IRPS)*, 2004, pp. 126-129.

[8] ESD Association Draft Standard Practice, "*ANSI/ESD SP5.4-2004: Transient Latch-up Testing – Component Level Supply Transient Simulation*," ESD Association, 2004.

[9] EIA/JEDEC Standard No. 78, "*IC Latch-up Test*," Electronic Industries Association, 1997.

[10] M.-D. Ker, and C.-Y. Wu, "Modeling the positive-feedback regenerative process of CMOS latchup by a positive transient pole method – Part I: Theoretical derivation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1141-1148, Jun. 1995.

[11] R. R. Troutman and H. P. Zappe, "A transient analysis of latchup in bulk CMOS," *IEEE Tran. Electron Devices*, vol. ED-30, no. 2, pp. 170-179, Feb. 1983.

[12] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.