Optimization of PMOS-Triggered SCR Devices for On-Chip ESD Protection in a 0.18-μm CMOS Technology

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Abstract

PMOS-triggered SCR devices with initial-on function have been proposed to achieve an efficient ESD protection in deep-submicron CMOS technology. The channel length of the embedded PMOS transistor in the PMOS-triggered SCR device dominates the trigger mechanism to govern the trigger voltage, holding voltage, turned-on resistance, second breakdown current, turn-on efficiency, and ESD robustness of the PMOS-triggered SCR device. The channel lengths of the embedded PMOS transistors in the PMOS-triggered SCR devices should be optimized to achieve the most efficient ESD protection design in deep-submicron or nanoscale CMOS technology.

1. Introduction

Due to the low breakdown voltage of the thinner gate oxide, the on-chip ESD protection circuit must be designed to rapidly and efficiently clamp the overstress voltage across the gate oxide of the internal circuits in deep-submicron CMOS technology [1]-[3]. The ESD specifications of the commercial IC products are generally required to be higher than 2 kV in human-body-model (HBM) and 200 V in machine-model (MM) ESD stresses. However, when the internal circuits are realized with a much thinner gate oxide in a deep-submicron CMOS technology, the general ESD protection designs cannot effectively protect the internal circuits. A new on-chip ESD protection concept with the initial-on ESD protection devices had been proposed [4]-[6]. The ESD clamp device is initially on, when the IC is floating with no any power bias. When the pad of IC is zapped by ESD stress, the ESD clamp device standing in the already-on status can rapidly discharge ESD current from the pad to ground. In order to enhance the applications of SCR devices for deep-submicron CMOS technology, a PMOS-triggered SCR device with initial-on function had been proposed to achieve the lower trigger voltage and the higher turn-on efficiency for efficient ESD protection in deep-submicron CMOS technology [6].

In this work, the PMOS-triggered SCR devices with different channel lengths (L) of the embedded PMOS transistors have been implemented in a 0.18-μm 1.8-V CMOS technology to optimize the device characteristics for efficiency applications in ESD protection. The channel lengths of the embedded PMOS transistors can significantly affect the characteristics, such as trigger voltage (Vt1), holding voltage (Vh), turn-on resistance (Ron), second breakdown current (It2), turn-on efficiency, and ESD robustness, for ESD protection design in deep-submicron CMOS technology. The optimization of the PMOS-triggered SCR devices can provide a higher efficiency of ESD protection to solve this main reliability issue on CMOS integrated circuits.

2. Implementations of PMOS-Triggered SCR Devices with Different Channel Lengths

The PMOS-triggered SCR device consists of embedded PMOS transistor, SCR structure, p-triggered node, n-triggered node, and RC-based ESD transient detection circuit, as shown in Fig. 1 [6]. The PMOS transistor is directly embedded into the SCR structure to achieve the initial-on function for ESD protection. The source and drain terminals of embedded PMOS transistors are respectively connected to the n-triggered and p-triggered nodes to synchronously generate double trigger currents into n-well and p-well of the SCR structure. The gate terminal of embedded PMOS transistor is tied to a RC-based ESD transient detection circuit. The RC-based ESD transient detection circuit is used to distinguish the ESD-stress conditions from the normal circuit operation conditions [7].

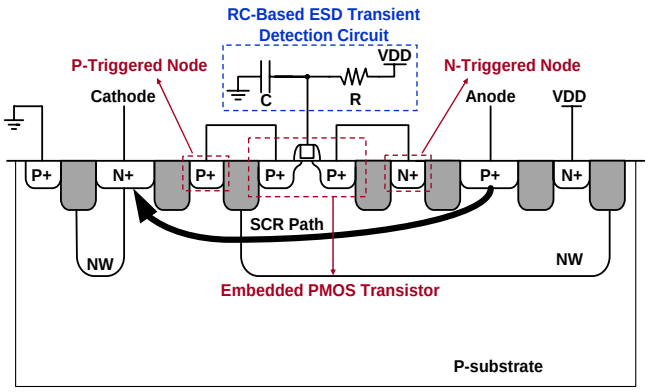


Fig. 1: The cross-sectional view of the PMOS-triggered SCR device with RC-based ESD transient detection circuit.

There are three different channel lengths (L), which are 0.3 μm, 0.5 μm, and 0.75 μm, of the embedded PMOS transistors in the PMOS-triggered SCR devices in our testchips. The illustrated layout top view of the PMOS-triggered SCR devices is shown in Fig. 2. Due to the different channel lengths in the embedded PMOS transistors, the anode-to-cathode spacings are also different in these three PMOS-triggered SCR devices. They are 6.8 μm, 7.0 μm, and 7.25 μm in the PMOS-triggered SCR devices with embedded PMOS transistors of 0.3-μm, 0.5-μm, and 0.75-μm channel lengths, respectively. In addition, the device width of each PMOS-triggered SCR device is only 50 μm.

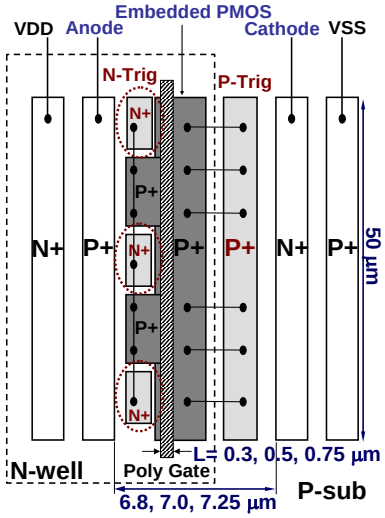


Fig. 2: The layout top view of PMOS-triggered SCR device with different channel lengths of the embedded PMOS transistor in a 0.18-μm CMOS process.

3. Influence of Channel Lengths on Device Characteristics of PMOS-Triggered SCR

The anode of the PMOS-triggered SCR device was connected to the RC-based ESD transient detection circuit, such as a power-rail ESD clamp circuit. The illustrated scheme is shown in Fig. 3. When the VDD pad is zapped by ESD stresses, the gate voltage of the embedded PMOS transistor is kept at 0 V by the RC-time delay. The embedded PMOS transistor is on to conduct the ESD current from the anode of the SCR or pickup of n-well, and then inject into the p-well of the SCR, as the dashed lines illustrated in Fig. 3 [6]. The channel lengths of the embedded PMOS transistors dominate the trigger current to affect the trigger voltage (Vt1), holding voltage (Vh), turn-on resistance (Ron), second breakdown current (It2), turn-on efficiency, and the ESD robustness of the PMOS-triggered SCR devices.

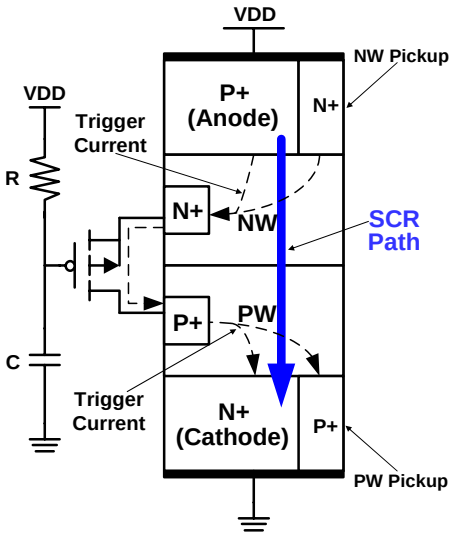
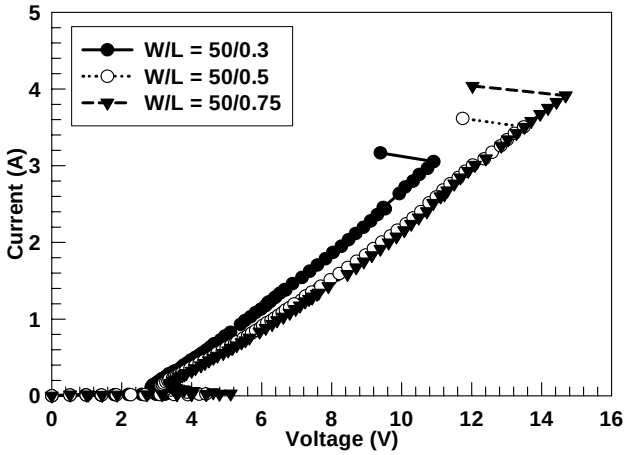
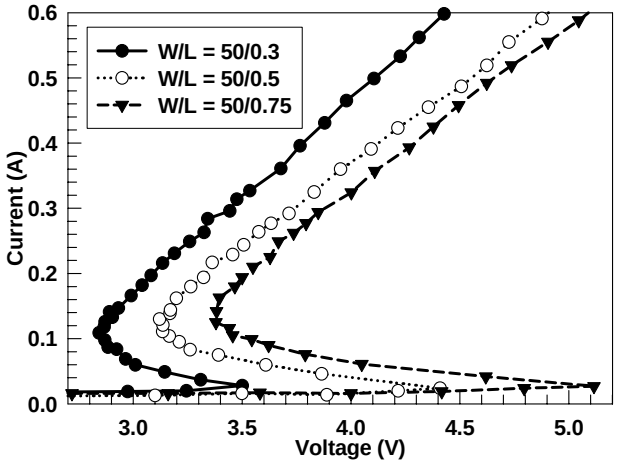


Fig. 3: The operation of the initial-on SCR design for power-rail ESD clamp circuit.

The TLP I-V curves of the PMOS-triggered SCR devices with different channel lengths in embedded PMOS transistors are shown in Figs. 4(a) and 4(b). The trigger voltages of the PMOS-triggered SCR devices are decreased from ~5.12 V to ~3.45 V in the embedded PMOS transistors of 0.75-μm to 0.3-μm channel lengths. The holding voltages are also decreased from ~3.40 V to ~2.82 V in the embedded PMOS transistors of 0.75-μm to 0.3-μm channel lengths. The measured results of the triggered voltages (Vt1) and holding voltages (Vh) are presented in Fig. 5. The turn-on resistances (Ron) of the PMOS-triggered SCR devices with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths in the embedded PMOS transistors are 2.71 Ω, 3.28 Ω, and 3.31 Ω, respectively, as shown in Table I.



(a)



(b)

Fig. 4: (a) TLP-measured I-V curves of the PMOS-triggered SCR devices with different channel lengths of the embedded PMOS transistors. (b) The zoomed-in view of (a) around the low current region.

The shorter channel lengths of the embedded PMOS transistors can generate the higher trigger currents to reduce the trigger voltage of the PMOS-triggered SCR devices. However, holding voltages and turn-on resistances of the

PMOS-triggered SCR devices also can be reduced, due to the shorter anode-to-cathode spacing and the lower parallel channel resistance in the embedded PMOS transistor. However, the second breakdown currents are increased from ~3.05 A to ~3.92 A by increasing the channel lengths of the embedded PMOS transistors. In addition, the HBM/MM ESD robustness of the PMOS-triggered SCR devices with 0.3-μm, 0.5-μm, and 0.75-μm channel lengths in the embedded PMOS transistors are respectively 5.0 kV/200 V, 6.5 kV/250 V, and 6.5 kV/300 V, as shown in Table II.

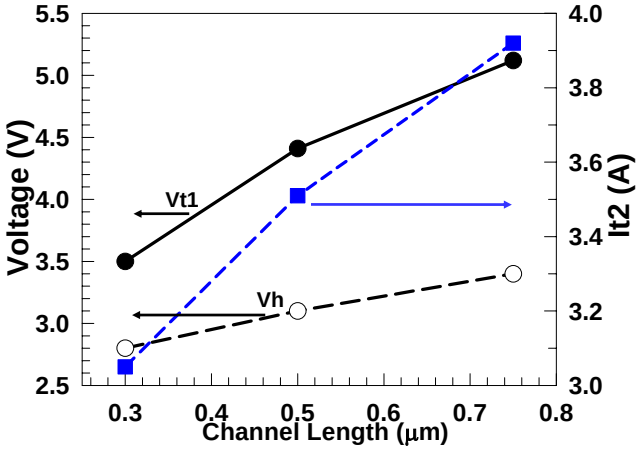


Fig. 5: Trigger voltages (Vt1), holding voltages (Vh), and second breakdown currents (It2) of the PMOS-triggered SCR devices with different channel lengths in the embedded PMOS transistors

Table I: Turn-on resistances (Ron) and second breakdown currents (It2) of the PMOS-triggered SCR devices with different channel lengths in the embedded PMOS transistors

Lengths	0.3 μm	0.5 μm	0.75 μm
It2 (A)	3.05	3.51	3.92
Ron (Ω)	2.71	3.28	3.31

Table II: HBM/MM ESD robustness of the PMOS-triggered SCR devices with different channel lengths in the embedded PMOS transistors

ESD Tests		L=0.3 μm	L=0.5 μm	L=0.75 μm
HBM	(+)	5000 V	6500 V	6500 V
	(-)	7000 V	> 8000 V	6500 V
MM	(+)	200 V	250 V	300 V
	(-)	500 V	550 V	650 V

In order to observe the turn-on efficiency of the PMOS-triggered SCR devices with different channel lengths in the embedded PMOS transistors, 5-V ESD-like voltage pluses with rise time of 2 ns were applied on the anodes of PMOS-triggered SCR devices with different channel lengths in embedded PMOS transistors. The rise time of Human Body Model (HBM) ESD event is about 2 ns to 10 ns [8]. The clamped voltage waveforms are compared in Fig. 6. The PMOS-triggered SCR device with 0.3-μm channel length in the embedded PMOS transistor can efficiently clamp the overshooting ESD voltage pulse to a lower voltage level. The measured voltage waveforms clearly prove that the higher turn-on efficiency of shorter channel lengths in the embedded PMOS transistors.

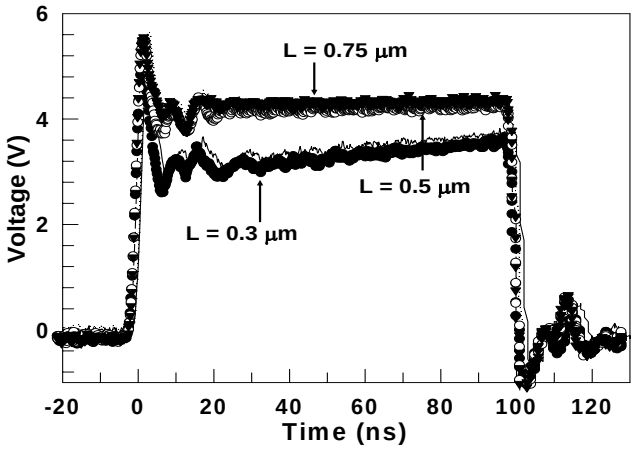
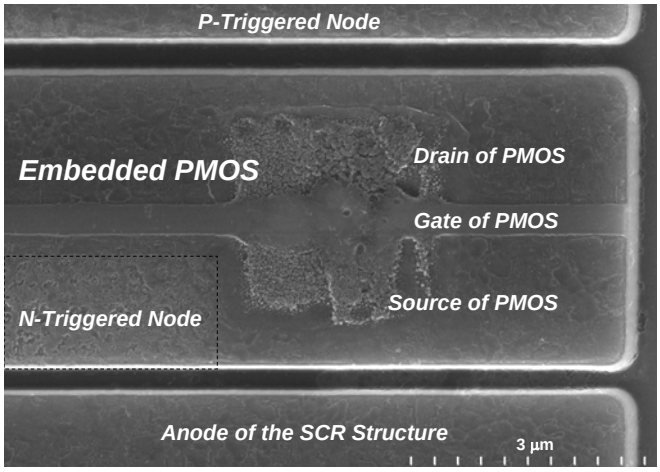


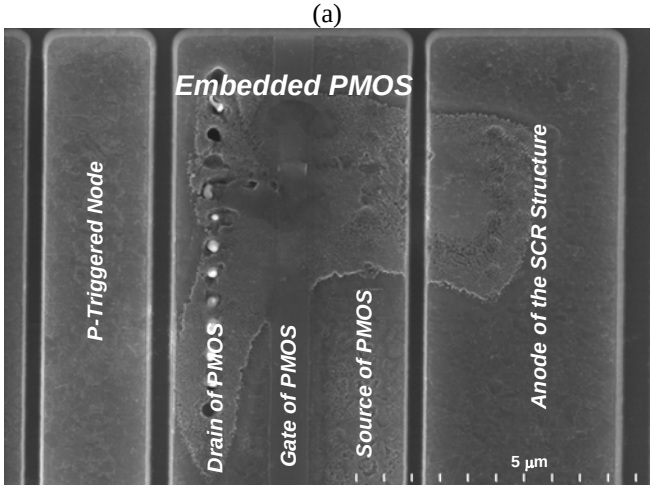
Fig. 6: The 5-V ESD-like voltage pulses were applied to the anodes of the PMOS-triggered SCR devices with different channel lengths in embedded PMOS transistors.

4. Influence of Channel Lengths on Failure Mechanisms of PMOS-Triggered SCR

The PMOS-triggered SCR device with 0.3-μm channel length in embedded PMOS transistor has a lower trigger voltage, lower holding voltage, and higher turn-on efficiency. However, the second breakdown currents and ESD robustness of PMOS-triggered SCR device with 0.3-μm channel length in embedded PMOS transistor is obviously lower than that with 0.5-μm or 0.75-μm channel length in embedded PMOS transistor. The shorter channel lengths in the embedded PMOS transistors cause the crowding of ESD currents nearby the embedded PMOS transistors, and generated the local joule heats too high to destroy the embedded PMOS transistors. In addition, the shorter channel lengths in the embedded PMOS transistors have the lower channel resistance to produce the huge ESD current discharging through the surface channel of PMOS transistors to cause the ESD damages. The failure analyses by SEM images are shown in Figs. 7(a), 7(b), and 7(c). The failure spots are located at the embedded PMOS transistors in the PMOS-triggered SCR device with 0.3-μm channel length in the embedded PMOS transistor, as presented in Fig. 7(a). Then, the failure spots are located at the anode diffusion to embedded PMOS transistor in the PMOS-triggered SCR devices with 0.5-μm and 0.75-μm channel lengths in the embedded PMOS transistors, as shown in Figs. 7(b) and 7(c).



(a)



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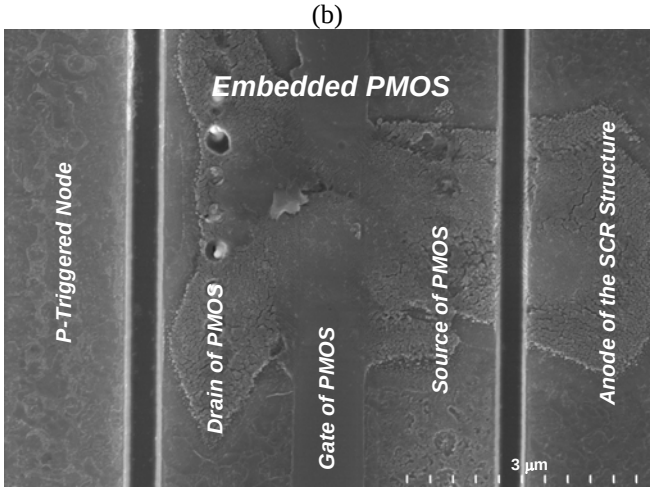

(c)

Fig. 7: (a) The failure spot is located at the embedded PMOS transistor in the PMOS-triggered SCR device with 0.3-μm channel length. (b) and (c) The failure spot is located at the anode to embedded PMOS transistor in the PMOS-triggered SCR devices with 0.5-μm and 0.75-μm channel lengths.

5. Conclusion

The channel lengths in the embedded PMOS transistors of the PMOS-triggered SCR devices significantly affect the devices characteristics, such as trigger voltage (Vt1), holding voltage (Vh), turn-on resistance (Ron), second breakdown current (It2), turn-on efficiency, ESD robustness, and failure mechanism of the PMOS-triggered SCR devices. The Vt1, Vh, and Ron of the PMOS-triggered SCR devices are decreased by decreasing the channel lengths in the embedded PMOS transistors. The channel lengths of the embedded PMOS transistors in the PMOS-triggered SCR devices should be optimized to achieve the most efficient ESD protection design in deep-submicron or nanoscale CMOS technology.

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