The Impact of N-Drift Implant on ESD Robustness of High-Voltage NMOS with Embedded SCR Structure in 40-V CMOS Process

Wei-Jen Chang[1], Ming-Dou Ker[1], Tai-Xiang Lai[2], Tien-Hao Tang[2], and Kuan-Cheng Su[2]

[1]Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
[2]United Microelectronics Corp., Science-based Industrial Park, Taiwan

Abstract

The ESD robustness on different device structures and layout parameters of high-voltage (HV) NMOS has been investigated in 40-V CMOS process with silicon verification. It was demonstrated that a specific structure of HV n-type silicon controlled rectifier (HVNSCR) embedded into HV NMOS without N-drift implant in the drain region has the best ESD robustness. Moreover, due to the different current distributions in HV NMOS and HVNSCR, the trends of the TLP-measured It2 under different spacings from the drain diffusion to polygate are different.

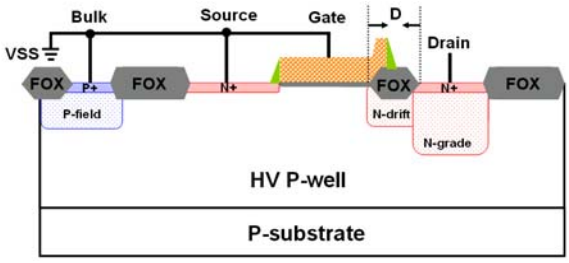
1. Introduction

High-voltage (HV) NMOS in the smart-power technology has been widely used in LCD driver circuits, telecommunication, power switch, motor control systems, etc [1]. In the smart-power technology, HV NMOS was often used as both of output driver and ESD protection device simultaneously. With an ultra-high operating voltage, the ESD robustness of high-voltage MOSFET is quite weaker than that of low-voltage MOSFET [2]–[10]. To increase ESD robustness, the conventional design with large device dimension still suffers the non-uniform current distribution among the device. The HV NMOS has the extremely strong snapback phenomenon during ESD stress, which often results in non-uniform turn-on variation among the multi-fingers of HV NMOS [11]. To overcome the problem of non-uniform turn-on phenomenon, the gate-coupling technique was applied to the HV NMOS [3], [4]. However, the gate of HV NMOS must be in series with a large resistor, which occupies a large layout area. Hence, how to improve the ESD robustness of HV NMOS with a reasonable silicon area is indeed an important reliability issue in HV CMOS technology.

In this paper, to improve ESD robustness in a limit layout area, a specific structure of HV n-type SCR (HVNSCR) can be built in the HV NMOS by replacing part of the drain region with P+ diffusion. ESD robustness of HV NMOS and HVNSCR are investigated with or without the N-drift implant in the drain region. In addition, the layout spacing from the drain diffusion to polygate is also split to find its dependence on ESD robustness. All test chips have been fabricated in a 0.35-μm 40-V CMOS technology.

2. Device Structure of HV NMOS with Embedded SCR

The device cross-sectional views of HV NMOS with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 1(a) and 1(b), respectively. The HV NMOS is fabricated in the HV P-well, where the P-field implant is used as isolation ring to isolate the device from the other. The N-grade implant is used to increase the breakdown voltage of the drain region in the HV NMOS. Moreover, the HV NMOS has lightly doped N-drift implant below the field oxide in the drain region, and utilizes the field oxide between the gate and the drain contact to minimize the peak electric field around the corner of the drain region, which can avoid the hot carrier effect in the N-channel.



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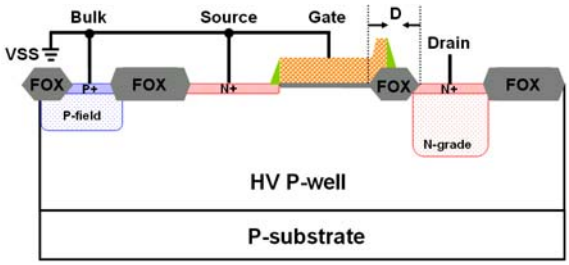


(b)

Fig. 1. The cross-sectional views of HV NMOS (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.

The trigger voltage of the HV NMOS device is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the parasitic lateral n-p-n BJT in HV NMOS will be triggered on to discharge ESD current.

It has been well known that SCR has a good ESD protection capability. Hence, to improve the ESD robustness of HV NMOS, the part of drain region in HV NMOS was replaced by P+ diffusion to form a SCR structure in the device, where the P+ diffusion is conjunction with N+ diffusion in the drain region. The device cross-sectional views of HVNSCR with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 2(a) and 2(b), respectively. The SCR path in the HV NMOS was composed by P+ diffusion in the drain region, N-grade, HV P-well, N+ diffusion in the source region. Here, no extra layout area is needed to realize this HVNSCR structure in HV NMOS.

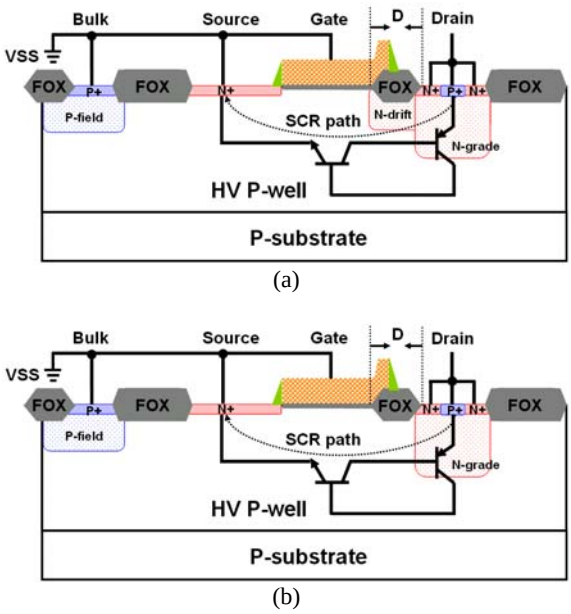


Fig. 2. The cross-sectional views of HVNSCR (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.

The HVNSCR device is composed of a lateral n-p-n BJT and a vertical p-n-p BJT to form a 2-terminal/4-layer PNPN (P+/N-grade/HV P-well/N+) structure. The trigger voltage of the HVNSCR device is the same as that of the HV NMOS, which is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the HV NMOS will be first triggered on by the ESD transient pulse, and then the embedded HVNSCR will be triggered on to discharge ESD current.

The equivalent circuit of the HVNSCR device embedded into HV NMOS is shown in Fig. 3. When the magnitude of the applied voltage is greater than the drain breakdown voltage of HV NMOS, the hole and electron currents will be generated through the avalanche breakdown mechanism. The hole current will flow through the HV P-well to P+ diffusion connected to the P-field ring of HV NMOS, which will increase the voltage level of the HV P-well. As long as the voltage drop across the HV P-well resistor ($R_{HV\ P\text{-}well}$) is greater than the cut-in voltage of lateral n-p-n BJT, the lateral n-p-n BJT will be triggered on to keep HV NMOS into its breakdown region. While the lateral n-p-n BJT is turned on, the electron current will be injected through the N-grade into N+ diffusion in the drain of HV NMOS to lower the voltage level of N-grade. As the injected electron current is larger than some critical value, the voltage drop across the N-grade resistor ($R_{N\text{-}grade}$) will be greater than the cut-in voltage of the vertical p-n-p BJT. The vertical p-n-p BJT will be turned on to inject the hole current through the HV P-well into P+ diffusion to further bias the lateral n-p-n BJT. Such positive feedback regeneration physical mechanism [12] will initiate the latching action in the HVNSCR. Finally, the HVNSCR will be successfully triggered into its latching state by the positive-feedback regenerative mechanism [12]. Once the HVNSCR is triggered on, the required holding current to keep the n-p-n and p-n-p BJTs on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism again.

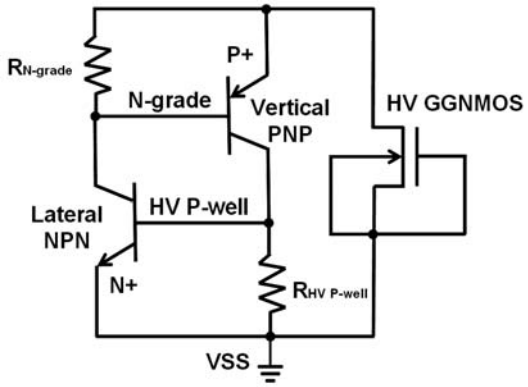


Fig. 3. The equivalent circuit of the HVNSCR embedded into HV GGNMOS.

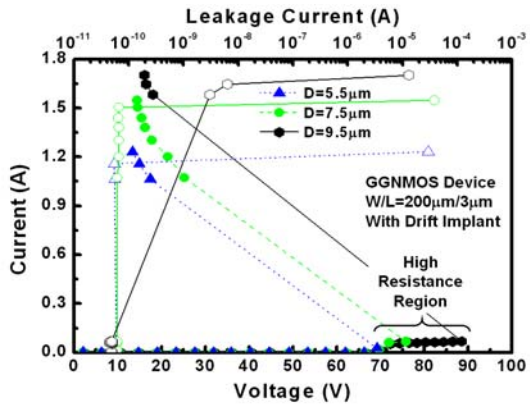
3. Experimental Results

To simulate the human-body-model (HBM) [13] ESD event, the transmission line pulsing generator (TLPG) [14] is designed to generate the stable and consistent pulses of very high current in a very short period of time. To investigate the device behavior during HBM ESD stress, the TLP with a pulse width of 100ns and a rise time of 10ns has been widely used to measure the secondary breakdown current (It2) of ESD devices. In the test chip, the device dimension (W/L) of HV NMOS was 200μm/3μm, where the minimum device lengths (L) of HV NMOS is 3μm in the given 0.35-μm 40-V CMOS process. The device dimension (W/L) of HVNSCR is also kept the same as that of HV NMOS.

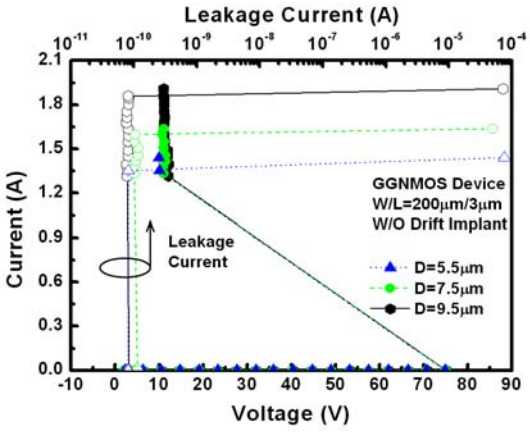
Generally, the ESD robustness is highly dependent on the ESD current discharging path among HV MOSFETs. In HV MOSFETs, the location of ESD damage is usually occurred at the drain region. Therefore, in this test chip, the drift implant in the drain region and the layout spacing (D) from the drain diffusion to polygate were split to see its

impact on ESD performance.

The TLP-measured I-V curves of HV gate-grounded NMOS (GGNMOS) with or without N-drift implant in the drain region are shown in Fig. 4, where the layout spacing from the drain diffusion to polygate (D, as shown in Fig. 1) is split to find the dependence on TLP-measured It2. The breakdown voltage of HV GGNMOS with or without N-drift implant is about 70V~75V, which is higher than the operation voltage of 40V. When the parasitic n-p-n BJT in HV GGNMOS is turned on, it will snap back with a low holding voltage.



(a)

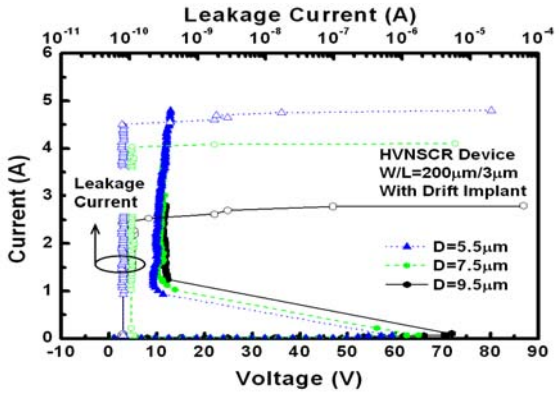


(b)

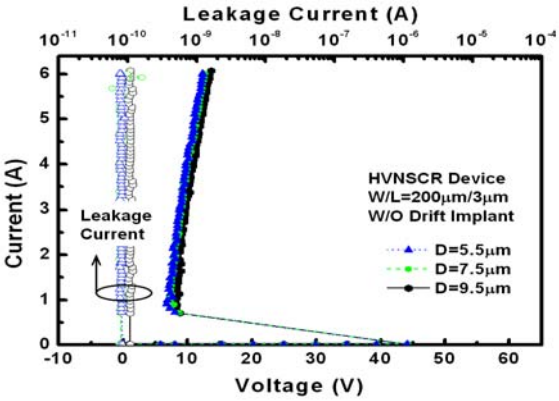
Fig. 4. The TLP-measured I-V curves of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region under different spacings D.

In Fig. 4(a), with N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.1A, 1.5A, and 1.7A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, respectively. The trigger voltage and holding voltage will be increased when the spacing D is increased. In Fig. 4(b), without N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.3A, 1.6A, and 1.9A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, where the It2 and the holding voltage are obviously increased as the parameter D is increased. The trigger voltage is 75V which is independent to the spacing D.

The TLP-measured I-V curves of HVNSCR with or without N-drift implant in the drain region under different layout spacings D are shown in Fig. 5. Though the measured trigger voltage of HVNSCR is lower than that of HV GGNMOS, it is still higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. After the HVNSCR is triggered on into its snapback region, it will keep at the lower holding voltage.



(a)



(b)

Fig. 5. The TLP-measured I-V curves of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region under different spacings D.

In Fig. 5(a), with N-drift implant, the TLP-measured It2 of HVNSCR are 4.9A, 4A, and 2.4A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, where the It2 is obviously increased as the spacing D is decreased. While the spacing D is increased, the distance from anode to cathode of SCR path is increased, which results in the increase of the holding voltage [15]. In Fig. 5(b), without N-drift implant, the TLP-measured It2 of HVNSCR are all over 6A for the spacing D of 5.5μm, 7.5μm, and 9.5μm. Comparing Fig. 5(a) and Fig. 5(b), under the same spacing of D, the HVNSCR without N-drift implant in the drain region also has a higher It2 than that with N-drift implant in the drain region. Moreover, HVNSCR without N-drift implant in the drain region has a lower trigger voltage, which can be triggered on into its snapback region earlier.

Table I. TLP-It2 of HV GGNMOS and HVNSCR with or without drift implant under different spacings D.

Spacing D in Layout	5.5μm	7.5μm	9.5μm
TLP-It2 of HV GGNMOS (With N-Drift Implant)	1.1A	1.5A	0.1A
TLP-It2 of HV GGNMOS (Without N-Drift Implant)	1.3A	1.6A	1.9A
TLP-It2 of HV GDPMOS (With P-Drift Implant)	0.01A	0.01A	0.06A
TLP-It2 of HV GDPMOS (Without P-Drift Implant)	0.13A	0.1A	0.14A

Table I summarizes the dependence of TLP-measured It2 of HV GGNMOS and HVNSCR with or without N-drift implant under different spacings D. With the same spacing of D, both HV GGNMOS and HVNSCR without N-drift implant have higher TLP-measured It2 than those with N-drift implant. The ESD current in the devices will flow more deeply into the HV P-well to avoid the current crowding at the channel surface without N-drift implant, which in turn can sustain higher ESD stress. In HV GGNMOS, only the drain avalanche breakdown current can be generated to the HV P-well to turn on the parasitic lateral n-p-n BJT. In HVNSCR, the parasitic vertical p-n-p BJT can be turned on because part of the current can flow from P+ diffusion of the drain region to HV P-well. The parasitic vertical p-n-p BJT can also provide a current to trigger on the parasitic lateral n-p-n BJT. Furthermore, with the turned on vertical p-n-p BJT, the current in HVNSCR flows more deeply into the HV P-well as compared to HV GGNMOS, which can make the current more uniform distribution among the HVNSCR to sustain higher ESD stress. Due to the different current distributions in HV GGNMOS and HVNSCR, the dependences of TLP-measured It2 on the spacing of D are different.

4. Conclusion

The N-drift implant in the drain region and layout spacing (D) from the drain diffusion to polygate have been spilt to verify the ESD robustness of HV NMOS and HVNSCR in a given 40-V CMOS process. It has been found that the devices without N-drift implant have higher TLP-measured It2 than those with N-drift implant. For HVNSCR, the TLP-measured It2 can be improved over 6A by removing N-drift in the drain region. Due to the different current distributions in HV GGNMOS and HVNSCR, the dependences of TLP-measured It2 on the spacing of D are different.

Acknowledgment

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