EVALUATION ON EFFICIENT MEASUREMENT SETUP FOR TRANSIENT-INDUCED LATCHUP WITH BI-POLAR TRIGGER

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ABSTRACT

An efficient measurement setup for transient-induced latchup (TLU) with bi-polar trigger is evaluated in this paper. The influences of the current-blocking diode and the current-limiting resistance on TLU immunity are investigated with the silicon controlled rectifier (SCR) fabricated in a 0.25-μm CMOS technology. The measurement setup without a current-blocking diode but with a small current-limiting resistance is recommended to evaluate TLU immunity of CMOS ICs. This recommended measurement setup not only can accurately judge the TLU level of CMOS ICs without over estimation, but also is beneficial to avoid electrical over-stress (EOS) damage on device under test (DUT). To further prove the utility of this recommended TLU measurement in the real circuits, a ring oscillator fabricated by 0.25-μm CMOS technology is used as the test circuit for verification.

INTRODUCTION

Quasi-static latchup, a primary reliability issue in CMOS ICs, was first found in applications of space radiation environments in the 1960's [1]. Once quasi-static latchup is triggered on due to the parasitic SCR located within CMOS ICs, a destructive high-current latchup state often leads to chip or system failure [2]. With the developed solutions against quasi-static latchup such as epitaxial layer [3], guard ring [4], retrograde well [5], shallow trench isolation (STI) [5], P^+ substrate [6], double [7] or triple well [8] technology, etc, the latchup concerns in CMOS ICs were once thought never a reliability issue again. However, due to the continually scaling down of device feature size and the growth of complicated circuitry such as SOC, mixed-signal, RF, multiple power supply systems, BiCMOS SiGe technologies [9], etc, it is still difficult to achieve the purpose of latchup-free in modern CMOS technology [10]. In particular, transient-induced latchup (TLU) under the strict-demanded system-level ESD test is an increasing reliability issue in state-of-the-art CMOS IC products [10]-[12].

In quasi-static latchup, it is usually considered that whether latchup failures will occur in the chip due to the overshooting or undershooting transient triggering at I/O pins because of impedance mismatch between I/O pins and printed circuit board (PCB) interface. In TLU, however, noises coming from external electromagnetic interference (EMI) or internal circuitry itself can cause a rapid power-to-ground voltage transition to initiate latctup in core circuitry. Some customer-returned CMOS ICs which had passed the quasi-static latchup test [13] still probably suffer from TLU failures in core circuitry. As a result, an efficient measurement setup which can accurately evaluate the TLU immunity of CMOS ICs is important to IC industry.

Several measurement setups to evaluate TLU immunity of CMOS ICs have been developed [11], [12], [14]. In particular, an underdamped bi-polar trigger was found to initiate TLU with a much lower trigger voltage than the overdamped uni-polar trigger does [12]. More importantly, the underdamped bi-polar trigger can reflect the real voltage waveform of EMI-generated noises under the system-level electrostatic discharge (ESD) test [15].

In this work, based on the TLU measurement setup with an underdamped bi-polar trigger [12], the current-blocking diode used to prevent capacitor-discharged current from flowing into the power supply [11], [12], is proved to be with an adverse effect on producing the intended underdamped bi-polar trigger. To clarify this issue, measurement setups combing two types of current-blocking diodes, fast recovery diode (PR1507) and general purpose diode (1N4007), with various current-limiting resistances are performed to investigate their dependences on bi-polar trigger waveforms. Moreover, two different physical mechanisms causing TLU between overdamped uni-polar trigger and underdamped bi-polar trigger are discussed through experimental results. Finally, a measurement setup without a current-blocking diode but with a small current-limiting resistance is recommended to evaluate TLU immunity of CMOS ICs. This recommended measurement setup for TLU has been well verified through the SCR test structures and the ring oscillator fabricated by 0.25-μm CMOS technology.

TEST STRUCTURE

An SCR structure is used as the test structure for TLU measurement because the occurrence of latchup results from the parasitic SCR in CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 1(a) and 1(b), respectively. The geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent contacts, respectively. All the SCR structures are fabricated by 0.25-μm salicided CMOS technology.

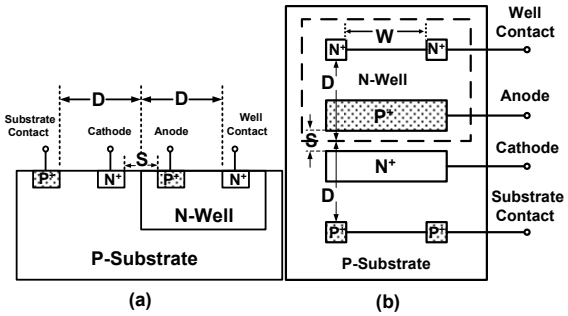

FIGURE 1. (A) DEVICE CROSS-SECTIONAL VIEW, AND (B) LAYOUT TOP VIEW, OF THE SCR STRUCTURE FOR TLU MEASUREMENTS.

MEASUREMENT SETUP

Fig. 2 sketches a typical measurement setup for TLU using underdamped bi-polar trigger [12]. The SCR structure shown in Fig.

1 is used as the DUT where the P^+ anode and the N^+ well contact are connected together to V_{DD}, whereas the N^+ cathode and the P^+ substrate contact are connected to ground.

The current-blocking diode used to prevent capacitor-discharged current from flowing into the power supply [11], [12] is considered to evaluate its dependences on TLU immunity of the SCR structures. The current-limiting resistance is used to avoid the EOS damage to DUT under a high-current latchup state. An electrostatic discharge (ESD) simulator is used to generate the underdamped bi-polar trigger source, V_{Charge}. In addition, a capacitor with capacitance of 200pF used in the machine model (MM) ESD test is employed as the charged capacitor. Compared with the former case [12] where the charged capacitor with capacitance of 100nF is used, the influence of a smaller charged capacitance (200pF) in Fig. 2 on the bi-polar trigger waveform is its damping frequency and damping factor. For example, the damping frequency in [12] is 500kHz, but it is found to be about 8MHz in this work. In practical measurement results of system-level ESD test where the damping frequency is about several tens of megahertz [16], TLU measurement setup in this work seems to be able to better simulate the system-level ESD test in the real field applications.

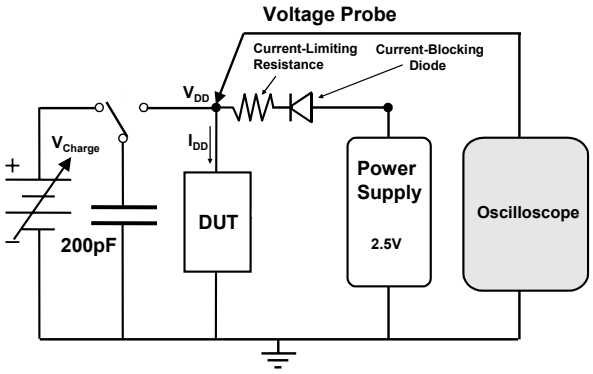

FIGURE 2. THE TYPICAL MEASUREMENT SETUP FOR TLU USING BI-POLAR TRIGGER [12].

EXPERIMENTAL RESULTS

A. Dependences of Current-Blocking Diode and Current-Limiting Resistance on Bi-Polar Trigger Waveforms

The SCR structure in Fig. 1 drawn with layout parameters of D=16.6μm, S=20μm, and W=22.5μm is used to investigate the influences of current-blocking diode and current-limiting resistance on the underdamped bi-polar trigger waveform. Furthermore, the underdamped bi-polar trigger source (V_{Charge}) is kept as small as +15V for positive V_{Charge} and -5V for negative V_{Charge} to prevent the occurrence of TLU, so that the bi-polar trigger waveform can be clearly observed.

With a positive V_{Charge} of +15V, when there is neither current-blocking diode nor current-limiting resistance in the measurement setup of Fig. 2, the transient V_{DD} and I_{DD} waveforms are shown in Fig. 3. The V_{DD} waveform reveals the intended positive-going underdamped bi-polar trigger with damping frequency of about 8 MHz. Afterwards, when a current-limiting resistance of 20Ω is added to the measurement setup in Fig. 2 but still without the current-blocking diode, the damping factor of V_{DD} waveform obviously increases, as shown in Fig. 4. This can be found in Fig. 3 where the initial positive peak value of V_{DD} must take about 2μsec to fully decay, but only 0.8μsec in Fig. 4. Furthermore, when a current-blocking diode (PR1507) is added to the measurement setup but without the current-limiting resistance, the V_{DD} waveform no longer reveals an underdamped bi-polar waveform, but an overdamped uni-polar waveform instead, as shown in Fig. 5. When the initially-stored positive charges in the charged capacitor (200pF) are discharged through the switch into the power supply or DUT, these positive charges are blocked by the current-blocking diode from flowing into the power supply, so the current-blocking diode is the equivalent of a large resistance (open circuit) to these positive charges. Similarly, the DUT, SCR structure, is also the equivalent of a large resistance to these positive charges because a large energy barrier built by the N-well/P-substrate junction is seen as a reverse-biased diode by the positive charges, therefore to block the positive charges from flowing into the DUT. This fact is true unless TLU or reverse junction breakdown occurs in the SCR structure. As shown in Fig. 4, a current-limiting resistance of 20Ω in series with the power supply increases the damping factor of the V_{DD} waveform, so the equivalent large resistance of the current-blocking diode tremendously increases the damping factor of the V_{DD} waveform to result in an overdamped uni-polar waveform, as shown in Fig. 5.

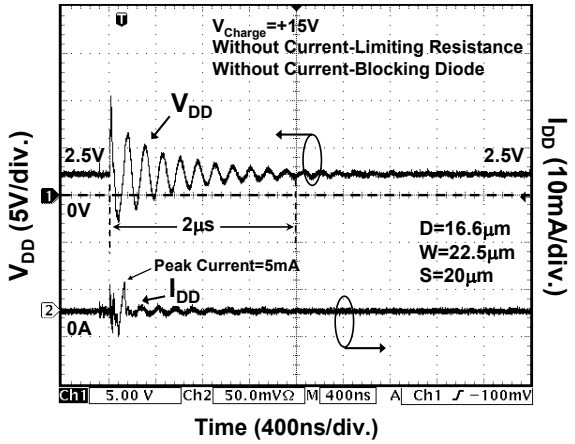

FIGURE 3. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A POSITIVE V_{Charge} OF +15V. NEITHER CURRENT-BLOCKING DIODE NOR CURRENT-LIMITING RESISTANCE IS USED IN THE TLU MEASUREMENT SETUP.

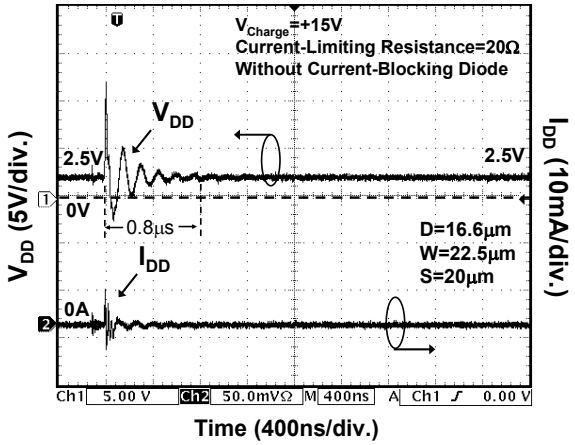

FIGURE 4. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A POSITIVE V_{Charge} OF +15V. A CURRENT-LIMITING RESISTANCE OF 20Ω BUT WITHOUT A CURRENT-BLOCKING DIODE IS USED IN THE TLU MEASUREMENT SETUP.

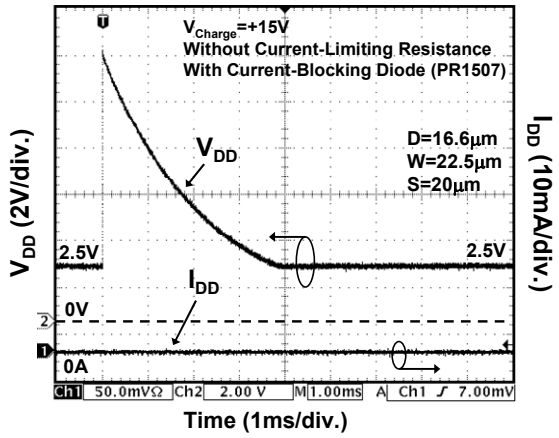

FIGURE 5. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A POSITIVE V_{Charge} OF +15V. A CURRENT-BLOCKING DIODE (PR1507) BUT WITHOUT A CURRENT-LIMITING RESISTANCE IS USED IN THE TLU MEASUREMENT SETUP.

With a negative V_{Charge} of -5V, when there is neither current-blocking diode nor current-limiting resistance in measurement setup, the transient V_{DD} and I_{DD} waveforms are shown in Fig. 6. The V_{DD} waveform reveals the intended negative-going underdamped bi-polar trigger waveform with the same damping frequency, 8 MHz, as that observed in Fig. 3. When a current-limiting resistance of 20Ω is further added to the measurement setup but still without the current-blocking diode, the damping factor of V_{DD} waveform obviously increases, as shown in Fig. 7. This can be found in Fig. 6 where the initial negative peak value of V_{DD} must take about 2µsec to fully decay, but only 0.8µsec in Fig. 7. Moreover, when a current-blocking diode (PR1507) is added to the measurement setup but without the current-limiting resistance, the transient V_{DD} and I_{DD} waveforms with a negative V_{Charge} of -5V are shown in Fig. 8. Unlike the same measurement setup with a positive V_{Charge} of +15V, where the V_{DD} waveform is an overdamped uni-polar waveform, the V_{DD} waveform is still an underdamped bi-polar waveform. The reason for this phenomenon is that when the initially-stored negative charges in the charged capacitor (200pF) are discharged through the switch into the power supply or DUT, the current-blocking diode is seen as a forward-biased diode by these negative charges, so the current-blocking diode is the equivalent of a small resistance (short circuit) to these negative charges. However, the DUT, SCR structure, is still the equivalent of a large resistance to these negative charges because a large energy barrier built by the P^+-anode/N-well junction is seen as a reversed-biased diode to these negative charges, thus to block the negative charges from flowing into the DUT. As shown in Fig. 7, a current-limiting resistance of 20Ω in series with the power supply increases the damping factor of the V_{DD} waveform, so the equivalent small resistance of the current-blocking diode slightly increases the damping factor of the V_{DD} waveform, as shown in Fig. 8.

B. Dependences of Current-Blocking Diode and Current-Limiting Resistance on TLU Level

The influences of current-blocking diode and current-limiting resistance on TLU level are considered by combing two types of current-blocking diodes, fast recovery diode (PR1507) and general purpose diode (1N4007), with various current-limiting resistances (0Ω, 5Ω, 10Ω, 20Ω, and 30Ω) in the TLU measurement setup. The TLU level is defined as the minimum value of V_{Charge} which can trigger on TLU. Furthermore, layout dependence on TLU level is also evaluated by using two SCR structures with the same D (16.6µm) and W (22.5µm) but different S of 1.2µm and 20µm fabricated in a 0.25-µm salicided CMOS process.

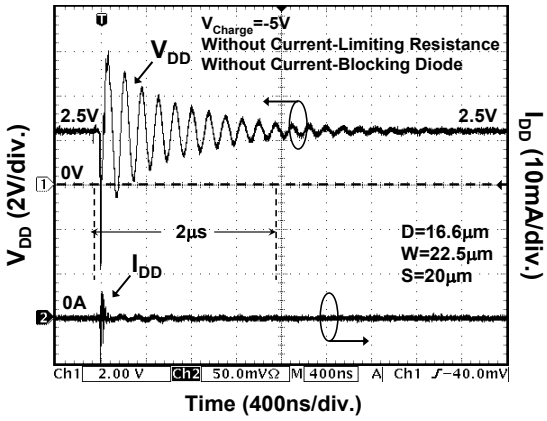

FIGURE 6. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A NEGATIVE V_{Charge} OF -5V. NEITHER CURRENT-BLOCKING DIODE NOR CURRENT-LIMITING RESISTANCE IS USED IN THE TLU MEASUREMENT SETUP.

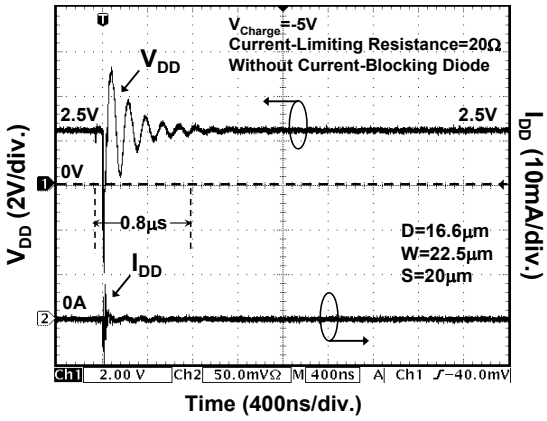

FIGURE 7. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A NEGATIVE V_{Charge} OF -5V. A CURRENT-LIMITING RESISTANCE OF 20Ω BUT WITHOUT A CURRENT-BLOCKING DIODE IS USED IN THE TLU MEASUREMENT SETUP.

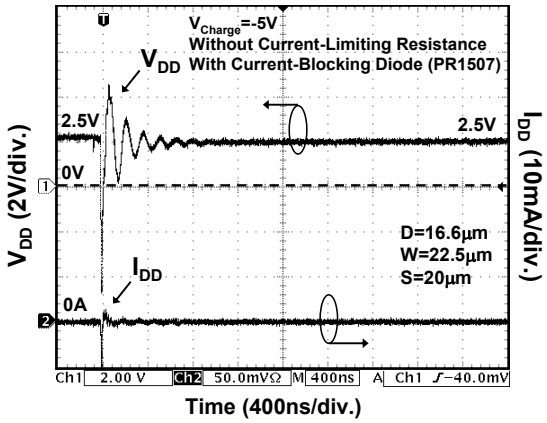

FIGURE 8. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A NEGATIVE V_{Charge} OF -5V. A CURRENT-BLOCKING DIODE (PR1507) BUT WITHOUT A CURRENT-LIMITING RESISTANCE IS USED IN THE TLU MEASUREMENT SETUP.

The experimentally measured latchup DC I-V characteristics for two SCR structures with the same D (16.6μm) and W (22.5μm) but different S of 1.2μm and 20μm are shown in Fig. 9. The SCR structure with S=20μm (S=1.2μm) has the trigger voltage (V_{Trig}) and the trigger current (I_{Trig}) of 21V (19.5V) and 4mA (2mA), respectively. Once latchup occurs in the SCR structure, a low-impedance path will exist from V_{DD} to ground, resulting in huge current conducting through this low-impedance path. As shown in the inset figure in Fig. 9, the SCR structure with S=20μm (S=1.2μm) has the holding voltage (V_{Hold}) and the holding current (I_{Hold}) of 1.5V (1V) and 16mA (10mA), respectively.

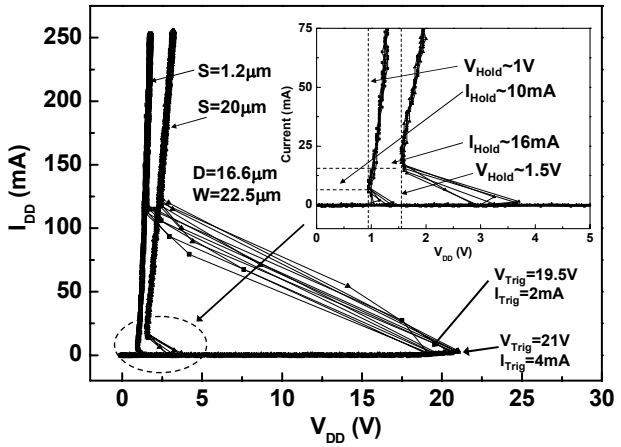

FIGURE 9. THE MEASURED LATCHUP DC I-V CHARACTERISTICS OF TWO SCR STRUCTURES WITH THE SAME D (16.6μm) AND W (22.5μm) BUT DIFFERENT S OF 1.2μm AND 20μm.

For the SCR structure with layout parameters of D=16.6μm, S=1.2μm, and W=22.5μm, Fig. 10 shows the relations between positive TLU level and current-limiting resistances under different current-blocking diodes. For measurement setup without current-blocking diode, the TLU level is smaller than that for the measurement setup with general purpose (1N4007) or fast recovery (PR1507) current-blocking diode. For measurement setup with current-blocking diode, the TLU-triggering current is the transient displacement current caused by the large reverse-biased P-substrate/N-well junction when the uni-polar trigger rapidly increases from 0V to its positive peak voltage, as shown in Fig. 5. However, for measurement setup without current-blocking diode, the TLU-triggering current is the "sweep-back" current (I_{Sb}) [17] caused by the stored minority carries when the N-well/P-substrate junction of the SCR structure quickly changes from the forward-biased state (V_{DD}<0) to the normal reversed-biased state (V_{DD}>0). Such unique I_{Sb} does exist under an underdapmed bi-polar trigger, as shown in Figs. 3 and 6. The bi-polar trigger has the ability to evaluate a lower TLU level of CMOS ICs than the uni-polar trigger does. Thus, the measurement setup without a current-blocking diode, whose TLU-triggering source is the bi-polar trigger, can evaluate a lower TLU level of CMOS ICs than that with a current-blocking diode, whose TLU-triggering source is the uni-polar trigger.

The influences of current-limiting resistance on positive TLU level are also shown in Fig. 10. For measurement setup with a current-blocking diode, TLU level is almost independent to current-limiting resistance. However, for measurement setup without current-blocking diode, the TLU level linearly increases with the increasing current-limiting resistance. The reason for such tendency is that a larger current-limiting resistance leads a smaller I_{Sb} [17] due to a larger damping factor of V_{DD} waveform, as shown in Fig. 4. However, the current-limiting resistance does not obviously affect the reverse displacement current, that is, the damping factor of V_{DD} waveform shown in Fig. 5. The equivalent large resistance of current-limiting diode in series with a small current-limiting resistance (<30Ω) makes the effect of current-limiting resistance negligible. Therefore, although current-limiting resistance can avoid EOS damage to DUT, it over estimates the TLU level of CMOS ICs when a bi-polar trigger is used.

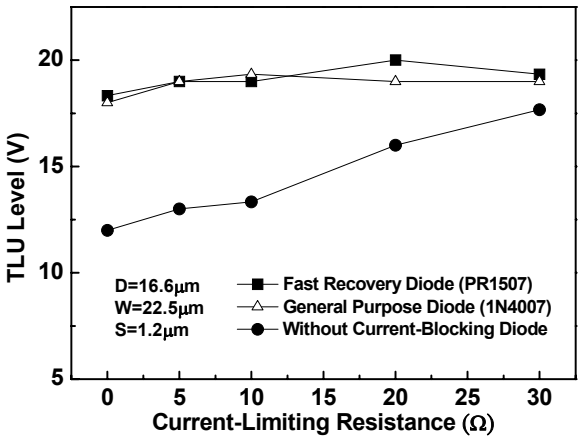

FIGURE 10. THE RELATIONS BETWEEN POSITIVE TLU LEVEL AND CURRENT-LIMITING RESISTANCES UNDER DIFFERENT CURRENT-BLOCKING DIODES. THE SCR STRUCTURE HAS THE LAYOUT PARAMETERS OF D=16.6μm, S=1.2μm, AND W=22.5μm.

For the SCR structure with layout parameters of D=16.6μm, S=20μm, and W=22.5μm, Fig. 11 shows the relations between positive TLU level and current-limiting resistances under different current-blocking diodes. Compared with the TLU dependences in Fig. 10, the more obvious difference is that the TLU level greatly increases to exceed +100V when the current-limiting resistance is larger than 20Ω for the measurement setup with a current-blocking diode. In fact, TLU does not occur in these cases due to one of the following two reasons. First, larger current-limiting resistance leads I_{DD} lower than the latchup holding current. Second, larger voltage drop across larger current-limiting resistance makes V_{DD} lower than the latchup holding voltage. No matter which happens, TLU does not occur. For example,

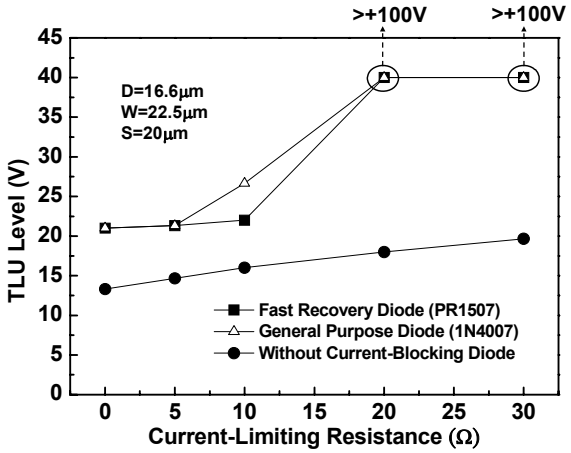

FIGURE 11. THE RELATIONS BETWEEN POSITIVE TLU LEVEL AND CURRENT-LIMITING RESISTANCES UNDER DIFFERENT CURRENT-BLOCKING DIODES. THE SCR STRUCTURE HAS THE LAYOUT PARAMETERS OF D=16.6μm, S=20μm, AND W=22.5μm.

with a positive V_{Charge} of +35V, Fig. 12 shows the transient V_{DD} and I_{DD} waveforms for measurement setup with a current-blocking diode (PR1507) and a current-limiting resistance of 20Ω. It seems that TLU initially occurs but eventually fails to be maintained because V_{DD} is pulled down to about 1V, which is lower than the latchup holding voltage (~1.5V). Thus, an additional voltage drop across the current-blocking diode or larger current-limiting resistance leads the V_{DD} (I_{DD}) lower than the holding voltage (holding current) of the SCR structure, where the SCR structure has layout parameters of D=16.6μm, S=20μm, and W=22.5μm.

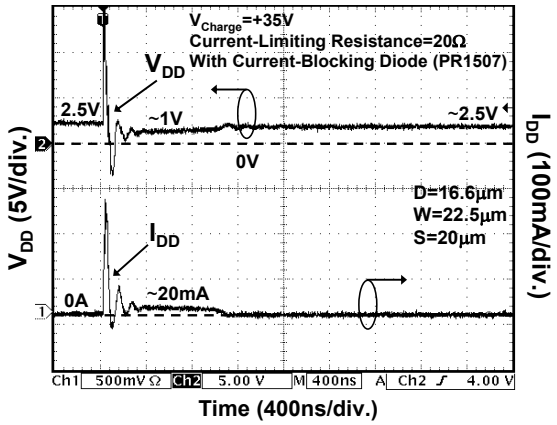

FIGURE 12. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS WITH A POSITIVE V_{Charge} OF +35V. A CURRENT-BLOCKING DIODE (PR1507) AND A CURRENT-LIMITING RESISTANCE OF 20Ω ARE USED IN THE TLU MEASUREMENT SETUP.

For SCR structure with layout parameters of D=16.6μm, W=22.5μm, and S=1.2μm (20μm), Fig. 13 (Fig. 14) shows the relations between negative TLU level and current-limiting resistances under different current-blocking diodes. Compared with the same measurement setup for positive TLU level test in Fig. 10 (Fig. 11), an obvious difference is the absolute value of negative TLU level is smaller than that of positive TLU level. The reason is that the TLU-triggering source is always a negative-going underdamped bi-polar trigger for a negative V_{Charge}, as shown in Figs. 6, 7, and 8. For both positive and negative V_{Charge} with the same absolute value, the negative V_{Charge} has a larger value of the average I_{Sb} due to a larger V_{DD} negative peak voltage [17]. Thus, the absolute value of negative TLU level evaluated by the negative-going bi-polar trigger is smaller than that of positive TLU level evaluated by either positive-going bi-polar trigger or uni-polar trigger.

Through evaluating the influences of current-blocking diode and current-limiting resistance on TLU level in Figs. 10, 11, 13, and 14, the measurement setup without the current-blocking diode is recommended to efficiently evaluate the TLU immunity of CMOS ICs. In addition, a larger current-limiting resistance (>20Ω) has been proved to lead TLU not occurring in the SCR structure with a higher holding voltage (1.5V), i.e. a larger S (20μm), in Figs. 11 and 14. Thereby, a small current-limiting resistance of 5Ω is recommended to be used. This current-limiting resistance of 5Ω can accurately evaluate the TLU level of CMOS ICs without over estimation, and also avoid the EOS damage to DUT during TLU test.

DISCUSSION

The transient displacement current and sweep-back current (I_{Sb}) have been clarified as the TLU-triggering current within CMOS ICs

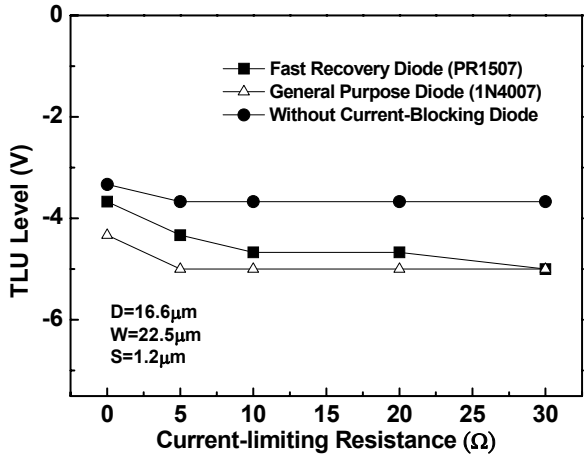

FIGURE 13. THE RELATIONS BETWEEN NEGATIVE TLU LEVEL AND CURRENT-LIMITING RESISTANCES UNDER DIFFERENT CURRENT-BLOCKING DIODES. THE SCR STRUCTURE HAS THE LAYOUT PARAMETERS OF D=16.6μm, S=1.2μm, AND W=22.5μm.

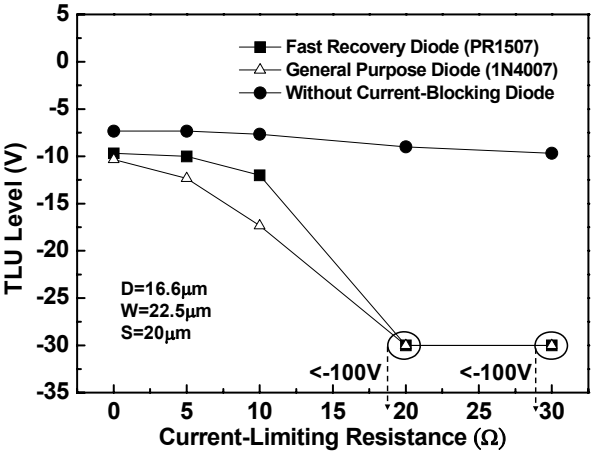

FIGURE 14. THE RELATIONS BETWEEN NEGATIVE TLU LEVEL AND CURRENT-LIMITING RESISTANCES UNDER DIFFERENT CURRENT-BLOCKING DIODES. THE SCR STRUCTURE HAS THE LAYOUT PARAMETERS OF D=16.6μm, S=20μm, AND W=22.5μm.

for uni-polar and bi-polar triggers, respectively [17]. From the TLU level dependences shown in Figs. 10, 11, 13, and 14, TLU is more susceptible to I_{Sb} caused by the bi-polar trigger. This can be further illustrated that V_{DD} and I_{DD} transient responses of TLU are different between uni-polar and bi-polar triggers. Figs. 15 and 16 show the V_{DD} and I_{DD} transient responses of TLU for uni-polar trigger (with current-blocking diode) and for bi-polar trigger (without current-blocking diode), respectively. Both cases use the same current-limiting resistance (5Ω) as well as the same SCR structure with layout parameters of D=16.6μm, W=22.5μm, and S=20μm. In Fig. 15, for uni-polar trigger with a positive V_{Charge} of +22V, TLU begins with the rapid-increasing I_{DD} while the V_{DD} initially increases (induce displacement current). In Fig. 16, for bi-polar trigger with a positive V_{Charge} of +14V, however, TLU begins with the rapid-increasing I_{DD} while the V_{DD} returns from its initial negative peak voltage to a normal positive voltage (induce I_{Sb}). Thus, by observing the V_{DD} and I_{DD} transient responses in time domain, it can be proved once again that TLU level is dependent on different types of TLU-triggering currents and the chosen TLU-triggering sources.

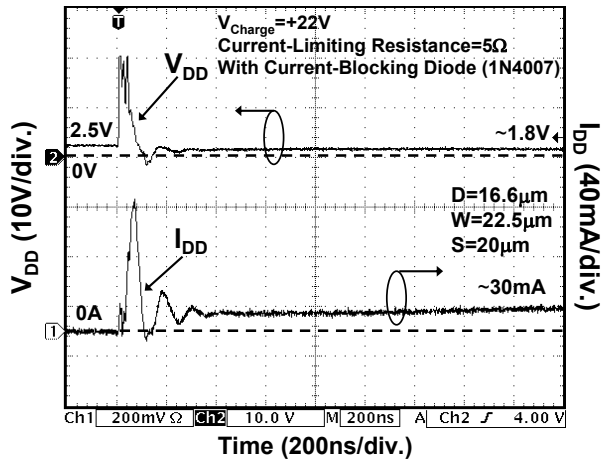

FIGURE 15. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS OF TLU FOR UNI-POLAR TRIGGER WITH A POSITIVE V_{Charge} OF +22V. A CURRENT-BLOCKING DIODE (1N4007) AND A CURRENT-LIMITING RESISTANCE OF 5Ω ARE USED IN THE TLU MEASUREMENT SETUP.

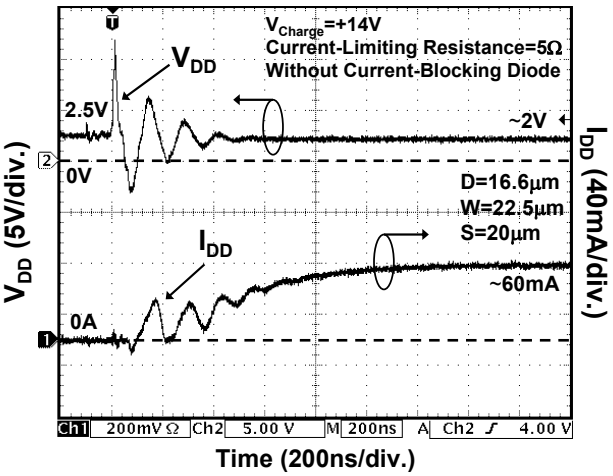

FIGURE 16. THE MEASURED V_{DD} AND I_{DD} TRANSIENT WAVEFORMS OF TLU FOR BI-POLAR TRIGGER WITH A POSITIVE V_{Charge} OF +14V. A CURRENT-LIMITING RESISTANCE OF 5Ω BUT WITHOUT A CURRENT-BLOCKING DIODE IS USED IN THE TLU MEASUREMENT SETUP.

VERIFICATION ON REAL CIRCUITS

A 100-MHz ring oscillator with 101-stage inverter chain and 7-stage taper buffer fabricated in a 0.25-μm CMOS technology is used as a real circuit to verify the TLU level by using the recommended measurement setup. The schematic diagram and layout top view of the ring oscillator are shown in Figs. 17(a) and 17(b), respectively. The geometrical parameters such as X, Y, and Z represent the distances between well-edge and well (substrate) contact, source (drain) regions of PMOS and NMOS, and the adjacent well (substrate) contacts, respectively. The TLU measurement setup shown in Fig. 2 with a 5Ω current-limiting resistance but without the current-blocking diode is employed as the recommended measurement setup to evaluate the TLU level of the ring oscillator. The ring oscillator is treated as the DUT in Fig. 2, where the N^+ well contact and the P^+ source of PMOS are connected together to V_{DD1}, but the P^+ substrate contact and the N^+ source of NMOS are connected to ground. It is noted that the layout

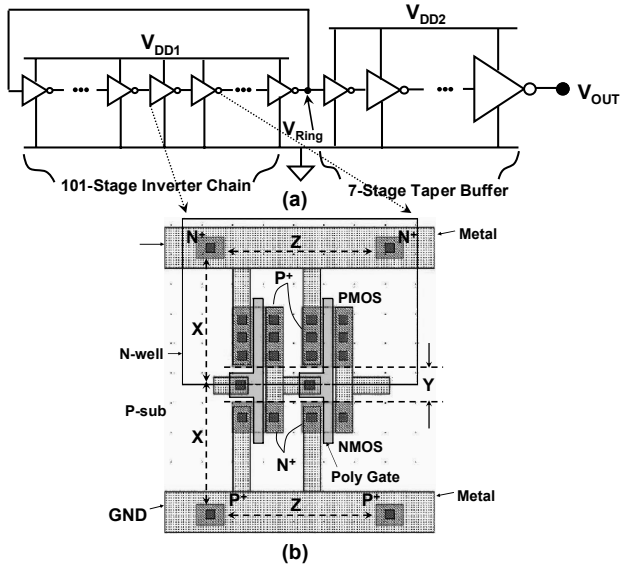

FIGURE 17. (A) SCHEMATIC DIAGRAM, AND (B) LAYOUT TOP VIEW, OF THE RING OSCILLATOR. THE GEOMETRICAL PARAMETERS SUCH AS X, Y, AND Z REPRESENT THE DISTANCES BETWEEN WELL-EDGE AND WELL (SUBSTRATE) CONTACT, SOURCE (DRAIN) REGIONS OF PMOS AND NMOS, AND THE ADJACENT WELL (SUBSTRATE) CONTACTS, RESPECTIVELY.

parameters of all the taper buffers are fixed, and the power line of the taper buffer (V_{DD2}) with a +2.5V power supply voltage is separated from the power line of the inverter chain (V_{DD1}) to evaluate the TLU level of the inverter chain but not the taper buffer. In fact, the parasitic SCR structure within the ring oscillator is composed of the P^+ source of PMOS (anode), N-well, P-substrate, and the N^+ source of NMOS (cathode). Once TLU is triggered on by a positive or negative V_{Charge} within the ring oscillator, rapid-increasing current will be conducted through a low-impedance path between V_{DD1} and ground, eventually probably burning out the chip due to over heating. For the ring oscillator in Fig. 17 with layout parameters of X=11.7μm, Y=1.2μm, and Z=10.5μm, Figs. 18 and 19 show the V_{DD1}, I_{DD1}, and V_{OUT} transient responses for TLU with a V_{Charge} of +20V and -10V, respectively. In both cases, TLU is triggered on due to large enough I_{Sb} while V_{DD1} increases from its negative peak voltage to its normal operating voltage, +2.5V. Meanwhile, large-increasing I_{DD1} accompanies the pull-down V_{DD1} due to a low-impedance path between V_{DD1} and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator, V_{Ring}, to be pulled down to ground, so V_{OUT} is kept at +2.5V after the 7-stage taper buffer.

Four measurement setups with two different types of current-blocking diodes (PR1507 and 1N4007) and current-limiting resistances (5Ω and 20Ω) are used to verify whether the recommended measurement setup has the lowest TLU level as those shown in Figs. 10, 11, 13, and 14. Moreover, two ring oscillators with layout parameters of X=16.6μm, Y=1.2μm, and Z=22.5μm and X=16.6μm, Y=10μm, and Z=0.3μm are also used to investigate the layout dependences on TLU level. Table I lists the TLU levels measured by these four different TLU measurement setups for the ring oscillator with layout parameters of X=16.6μm, Y=1.2μm, and Z=22.5μm. Clearly, both positive and negative TLU levels measured by the recommended TLU measurement setup (Type A) are lower than those measured by the other three measurement setups (Type B, C, and D).

Similarly, Table II lists the TLU levels for the ring oscillator with layout parameters of X=16.6μm, Y=10μm, and Z=0.3μm. In addition to the recommended measurement setup (Type A), the other three measurement setups are not capable of evaluating the TLU level. The additional voltage drop across the current-blocking diode or larger current-limiting resistance leads the V_{DD} (I_{DD}) lower than the holding voltage (holding current) of the parasitic SCR in the ring oscillator, where the ring oscillator has layout parameters of X=16.6μm, Y=10μm, and Z=0.3μm. Thus, it's proved once again the recommended measurement setup, where there is no current-blocking diode but a small current-limiting resistance (5Ω), can evaluate TLU level of CMOS ICs without over estimation, and also has the advantage to avoid the EOS damage to DUT during TLU test. In addition, comparing with the TLU levels in Tables I and II, TLU level of the ring oscillator with layout parameters of X=16.6μm, Y=10μm, and Z=0.3μm is higher than that of the ring oscillator with layout parameters of X=16.6μm, Y=1.2μm, and Z=22.5μm.

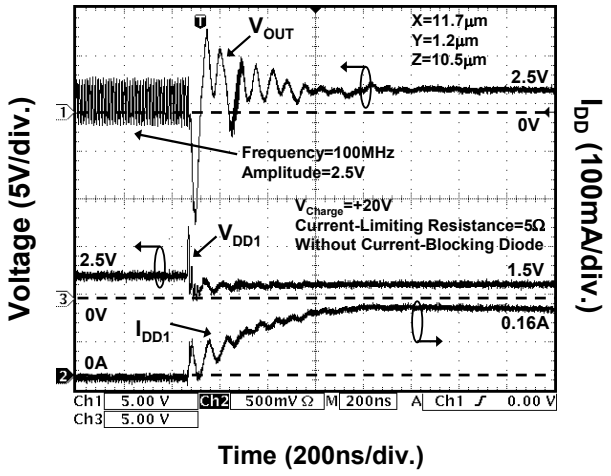

FIGURE 18. THE MEASURED V_{DD1}, I_{DD1}, AND V_{OUT} TRANSIENT WAVEFORMS OF THE RING OSCILLATOR WITH A POSITIVE V_{Charge} OF +20V. A CURRENT-LIMITING RESISTANCE OF 5Ω BUT WITHOUT A CURRENT-BLOCKING DIODE IS USED IN THE TLU MEASUREMENT SETUP.

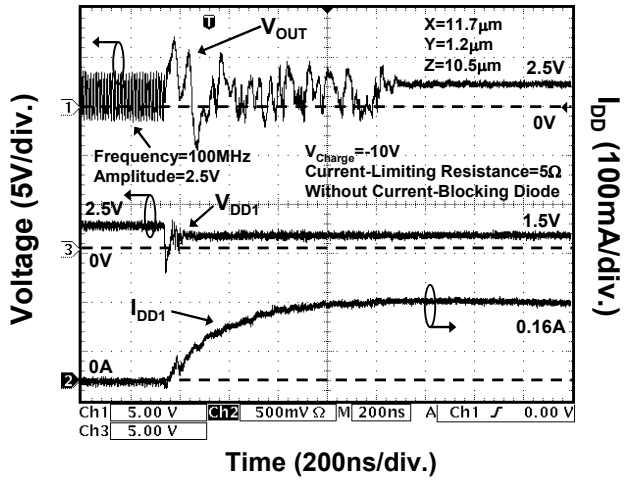

FIGURE 19. THE MEASURED V_{DD1}, I_{DD1}, AND V_{OUT} TRANSIENT WAVEFORMS OF THE RING OSCILLATOR WITH A NEGATIVE V_{Charge} OF -10V. A CURRENT-LIMITING RESISTANCE OF 5Ω BUT WITHOUT A CURRENT-BLOCKING DIODE IS USED IN THE TLU MEASUREMENT SETUP.

TABLE I
THE RELATIONS BETWEEN TLU LEVEL AND FOUR DIFFERENT TLU MEASUREMENT SETUPS FOR THE RING OSCILLATOR WITH LAYOUT PARAMETERS OF X=16.6μm, Y=1.2μm, and Z=22.5μm

Measurement Setups	Type A	Type B	Type C	Type D
Current-Blocking Diode	None	PR1507	None	1N4007
Current-Limiting Resistance	5Ω	5Ω	20Ω	20Ω
Positive TLU Level	+7V	+15V	+10V	+15V
Negative TLU Level	-5V	-9V	-7V	-10V

TABLE II
THE RELATIONS BETWEEN TLU LEVEL AND FOUR DIFFERENT TLU MEASUREMENT SETUPS FOR THE RING OSCILLATOR WITH LAYOUT PARAMETERS OF X=16.6μm, Y=10μm, and Z=0.3μm

Measurement Setups	Type A	Type B	Type C	Type D
Current-Blocking Diode	None	PR1507	None	1N4007
Current-Limiting Resistance	5Ω	5Ω	20Ω	20Ω
Positive TLU Level	+26V	TLU Does Not Occur	TLU Does Not Occur	TLU Does Not Occur
Negative TLU Level	-11V	TLU Does Not Occur	TLU Does Not Occur	TLU Does Not Occur

CONCLUSION

An efficient measurement setup which is capable of accurately judging the TLU level of CMOS ICs without over estimation has been proposed and verified with silicon chips. In particular, measurement setup with an underdamped bi-polar trigger has been proved to have a lower TLU level than the overdamped uni-polar trigger does. Through investigating the influences of current-blocking diode on bi-polar trigger waveform, it has been found that the intended positive-going bi-polar trigger waveform can not be produced, but a positive-going uni-polar trigger waveform instead. The reason is that the current-blocking diode serves as a large resistance to the discharged positive charges and largely increases the damping factor of V_{DD}. In addition, although the intended negative-going bi-polar trigger waveform can be produced, its damping factor slightly increases because the current-blocking diode serves as a small resistance to the discharged negative charges. Through evaluating the influences of current-limiting

resistance on bi-polar trigger waveform, a current-limiting resistance increases the damping factor of V_{DD} and over estimates the TLU level of CMOS ICs. However, a low current-limiting resistance does not have an apparent impact on evaluating the TLU level. Thus, the TLU measurement setup without a current-blocking diode but with a small current-limiting resistance of 5Ω is recommended. This recommended measurement setup can precisely evaluate the TLU level of CMOS ICs without over estimation, which is beneficial to avoid EOS damage to DUT during TLU test. This recommended TLU measurement setup has been used to evaluate the TLU immunity of the SCR test structure and the ring oscillator in silicon chips with different layout parameters.

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REFERENCES

[1] K. Kinoshito, C. T. Kleiner, and E. D. Johnson, "Radiation induced regeneration through the P-N junction isolation in monolithic IC's," *IEEE Trans. Nuclear Science*, vol. 12, pp. 83–90, Oct. 1965.

[2] R. Troutman, "*Latchup in CMOS Technology: The Problem and the Cure*," Kluwer Publications, New York, 1986.

[3] D. B. Estreich, A. Ochoa, and R. W. Dutton, "Analysis of latchup prevention in CMOS IC's using epitaxial buried layer process," in *IEDM Tech. Dig.*, 1978, pp. 230–234.

[4] R. Troutman, "Epitaxial layer enhancement of N-well guard rings for CMOS circuits," *IEEE Electron Device Lett.*, vol. 4, pp. 438–440, Dec. 1983.

[5] S. Voldman, M. Marceau, A. Baker, E. Adler, S. Geissler, J. Slinkman, J. Johnson, and M. Paggi, " Retrograde well and epitaxial thickness optimization for shallow- and deep-trench collar merged isolation and node trench SPT cell and CMOS logic technology," in *IEDM Tech. Dig.*, 1992, pp. 811–815.

[6] M. Hargrove, S. Voldman, J. Brown, K. Duncan, and W. Craig, "Latchup in CMOS," in *Proc. IRPS*, 1998, pp. 269–278.

[7] G. Goto, H. Takahashi, and T. Nakamura, "Latchup immunity against noise pulses in a CMOS double well structure," in *IEDM Tech. Dig.*, 1983, pp. 168–171.

[8] S. Voldman, E. G. Gebreselasie, D. Hershberger, D. S. Collins, N. B. Feilchenfeld, S. A. St. Onge, A. Joseph, and J. Dunn, "Latchup in merged triple well technology," in *Proc. IRPS*, 2005, *in press*.

[9] S. Voldman, and A. Watson, "The influence of deep trench and substrate resistance on the latchup robustness in a BiCMOS silicon germanium technology," in *Proc. IRPS*, 2004, pp. 135–142.

[10] S. Voldman, "Latch-up – it's back," in *Threshold Newsletter*, ESD Association, Sep./Oct., 2003.

[11] M. Kelly, L. Henry, J. Barth, G. Weiss, M. Chaine, H. Gieser, D. Bonfert, T. Meuse, V. Gross, C. Hatchard, and I. Morgan, "Developing a transient induced latch-up standard for testing integrated circuits," in *Proc. EOS/ESD Symp*., 1999, pp. 178–189.

[12] I. Morgan, C. Hatchard, and M. Mahanpour, "Transient latch-up using an improved bi-polar trigger," in *Proc. EOS/ESD Symp*., 1999, pp. 190–202.

[13] EIA/JEDEC Standard No. 78, "*IC Latch-up Test*," Electronic Industries Association, 1997.

[14] ESD Association Standard Practice, "*ANSI/ESD SP5.4-2004: Transient Latch-up Testing – Component Level Supply Transient Stimulation*," ESD Association, 2004.

[15] IEC 61000-4-2 International Standard, "*EMC – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*," IEC, 2001.

[16] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in an 8-bits microcontroller to solve the system-level ESD issue on keyboard," in *Proc. EOS/ESD Symp*., 1999, pp. 352–360.

[17] M.-D. Ker and S.-F. Hsu, "Transient-induced latchup in CMOS technology: physical mechanism and device simulation," in *IEDM Tech. Dig.*, 2004, pp. 937–940.